

Automated Critical Device Identification for Configurable Analogue Transistors

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Abstract—A novel approach is proposed for analogue circuits that identifies which devices should be replaced with configurable analogue transistors (CATs) to maximise post fabrication yield. Both performance sensitivity and adjustment independence are considered when identifying these critical devices, giving a combined weighted sensitivity. The results from an operational amplifier case study are presented where it is demonstrated that variation in key circuit performances can be reduced by an average of 78.8% with the use of only three CATs. These results confirm that the proposed critical device selection method with optimal performance driven CAT sizing can lead to significant improvement in overall performance and yield.

Keywords—configurable analogue transistor; optimal sizing; device variability; sensitivity analysis, post fabrication calibration

I. INTRODUCTION

A. CMOS Scaling

Maintaining production yield at smaller process nodes raises significant challenges due to device variability [1][2]. In analogue and mixed-signal circuits, the resulting performance degradation can be so severe that some form of post-silicon adjustment is necessary [3]. Early approaches concentrate solely on the adjustment of a single device to improve circuit performance [4]. This is often impractical in more complex systems that require multiple adjustment points or a higher level of integration [5]. In contrast, electronic trimming methods such as the use of floating gates [6][7] or substrate biasing [8] to alter the transfer characteristics of MOS transistors allow higher integration at lower cost. Furthermore, a wide range of simple digital trimming techniques exist, e.g. configurable arrays of MOS devices [9] or capacitors [10].

System-level digital methods have also been proposed, where circuit errors are corrected in software [11] or in the analogue domain by reconfiguration, e.g. switching-sequence post adjustment for data converters (SSPA) [12].

B. The Configurable Analogue Transistor (CAT)

The calibration methods described in the previous section tend to be targeted at either fairly specific circuit applications or effects (e.g. floating gates). The choice of which devices to make adjustable is conventionally made early in the design stage and is based on the type of circuit, the technology available and the anticipated main sources of variability. The configurable analogue transistor (CAT) introduced in [13] provides a calibration platform that is independent of the target circuit and the specific mechanisms of variation. This is

achieved by considering system-level performance and replacing specific transistors in the circuit with CATs. The number of CATs represents a trade-off between increased circuit complexity and yield improvement. The structure of a CAT is shown in Figure 1. There is a main device M_0 and n calibration devices M_1 to M_n , selected through n digital control lines, B_1 to B_n , resulting in a total of 2^n discrete widths. In contrast to previous digitally adjustable analogue circuits, the CAT methodology includes a unique optimal sizing process [13]. The CAT configuration can be altered at any time after fabrication either as a one-time post-fabrication process, or to dynamically calibrate circuits to compensate for environmental effects or ageing [14].

C. Critical Device Identification

In principle, any transistor in a given circuit could be replaced by a CAT. A designer could manually identify devices that would benefit from calibration based on experience and their understanding of the operation of the circuit, however this becomes more difficult as the circuit complexity increases.

In order to facilitate optimal performance gain from the application of CATs, an automated method of Critical Device Identification (CDI) is an integral part of the approach. The task of CDI is to identify a number of transistors, which when adjusted allow the performances to be tuned after fabrication. This paper proposes a novel approach to critical device identification which is fully automated and independent of circuit type. In addition, the proposed method also optimally sizes the CATs to minimise performance variation.

D. Paper Structure

The remainder of this paper is structured as follows: Section II describes the proposed technique for critical device identification. Section III presents the results from applying the approach to an operational amplifier case study. Concluding remarks are given in Section IV.

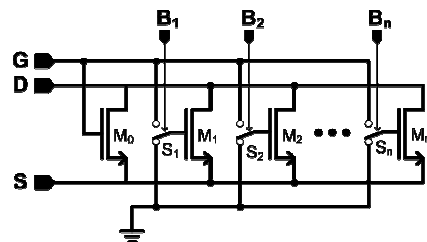


Figure 1: Structure of the configurable analogue transistor.

II. PROPOSED METHOD

A. Overview

The proposed process of CDI and its application to a circuit is illustrated in Figure 2 and comprises of five steps as follows.

Step 1: A conventional sensitivity analysis is performed in simulation. The dependence of circuit performance to changes in individual devices is recorded in a sensitivity table.

Step 2: The sensitivity information is used to perform CDI, resulting in a list of transistors that are most suitable.

Step 3: A Monte Carlo (MC) simulation of the circuit is used to adjust the critical devices in an ideal manner to minimise performance variability.

Step 4: The critical devices are replaced by CATs with a finite number of calibration transistors (optimal sizing from step 3).

Step 5: In the last step, a MC simulation is performed and the required adjustment for each critical device is calculated.

To illustrate the proposed process, Figure 3 shows the circuit of an operational amplifier. The circuit consists of a differential input stage, MP4 and MP5, gain stage, MN8, and an output buffer, MN6. MN9 and the capacitor form the internal compensation network and MP0-MP1, MN0-MN3 and the resistor form the bias circuit.

The performance characteristics that are considered are DC voltage gain, open-loop bandwidth and common-mode rejection ratio. The operational amplifier is designed in a standard $0.35\mu\text{m}$ CMOS process at 3.3V , with active and passive component values as listed in Table I.

B. Sensitivity Analysis and Critical Device Identification

The sensitivity of each performance to a change in each transistor's width is normalised as a relative change to its nominal value, as defined in Equation 1:

$$S_{A,n} = \frac{A|_{w_n=nom+5\%} - A|_{w_n=nom-5\%}}{A|_{w_n=nom}} \quad (1)$$

where A is a circuit performance (e.g. gain) evaluated with the

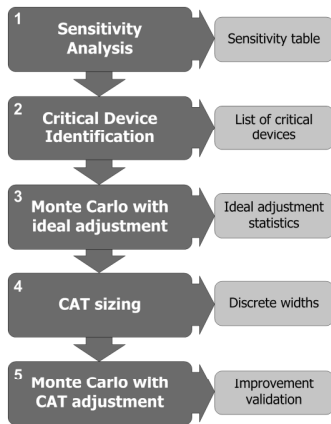


Figure 3: Process flow of critical device identification and CAT replacement

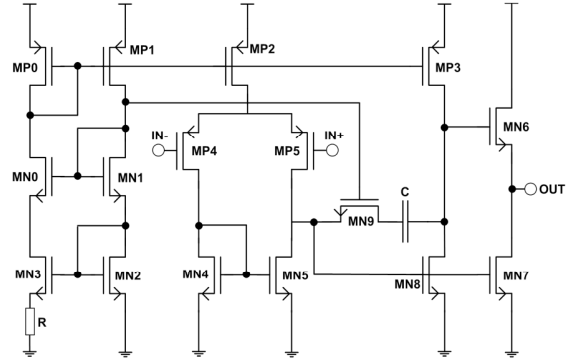


Figure 2: Circuit diagram of the operational amplifier

width of transistor n , w_n , at different values, resulting in the sensitivity of performance A on transistor n , $s_{A,n}$. The sensitivities obtained for the operational amplifier when applying the above sensitivity analysis for all performance-transistor combinations are shown on the left of Table II. The assumption in Table II is that there is a linear relationship between the performance and transistor width within the range of interest and that the circuit is a linear system within this range and therefore superposition applies. In practice these assumptions have been found to be valid and their implications are discussed later in this paper. In the proposed method for CDI, the two goals of high sensitivity and high independence are combined. First, a normalised measure for independence is derived by calculating the ratio of a particular sensitivity to all the sensitivities associated with that particular transistor, as per Equation 2:

$$w_{A,n} = \frac{|s_{A,n}|}{\sum |s_n|} \quad (2)$$

Where A represents a certain performance, n a certain transistor and $w_{A,n}$ the relative amount of transistor n 's total impact on performance. The weighting table that was obtained for the operational amplifier case study is shown in the centre section of Table II. Secondly, element-wise multiplication of the original sensitivity table and the weighting table is performed as per Equation 3:

$$s'_{A,n} = s_{A,n} \cdot w_{A,n} \quad (3)$$

which results in a sensitivity table, $s'_{A,n}$, that considers both absolute sensitivity and independence. The weighted sensitivity table for the operational amplifier is shown on the right of

TABLE I. DEVICE SIZES AND COMPONENT VALUES

Device	Dimensions	Device	Dimensions
MP0	$8.75\mu\text{m} / 0.35\mu\text{m}$	MN2	$35\mu\text{m} / 0.35\mu\text{m}$
MP1	$8.75\mu\text{m} / 0.35\mu\text{m}$	MN3	$35\mu\text{m} / 0.35\mu\text{m}$
MP2	$105\mu\text{m} / 0.35\mu\text{m}$	MN4	$52.5\mu\text{m} / 0.35\mu\text{m}$
MP3	$105\mu\text{m} / 0.35\mu\text{m}$	MN5	$52.5\mu\text{m} / 0.35\mu\text{m}$
MP4	$105\mu\text{m} / 0.35\mu\text{m}$	MN6	$175\mu\text{m} / 0.35\mu\text{m}$
MP5	$105\mu\text{m} / 0.35\mu\text{m}$	MN7	$175\mu\text{m} / 0.35\mu\text{m}$
MN0	$8.75\mu\text{m} / 0.35\mu\text{m}$	MN8	$98\mu\text{m} / 0.35\mu\text{m}$
MN1	$8.75\mu\text{m} / 0.35\mu\text{m}$	MN9	$50\mu\text{m} / 0.35\mu\text{m}$
Component	Value	Component	Value
R	$823\text{k}\Omega$	C	623fF

Table II. For the purpose of this work, one critical device is chosen for each performance by selecting the transistors with greatest weighted sensitivity. In this case, the critical devices are therefore MP0 for bandwidth, MP3 for gain and MN7 for CMRR. Although MP0 significantly affects both gain and bandwidth it is still chosen as a critical device for bandwidth due to its very high absolute sensitivity to this performance.

C. Calculation of Ideal Transistor Adjustment

From the sensitivity information obtained in the previous section, the resulting change in circuit performance from adjusting the widths of the critical devices can be described by a system of linear equations:

$$\begin{aligned}\Delta A &= s_{A1}\Delta w_1 + s_{A2}\Delta w_2 + \dots + s_{AN}\Delta w_N \\ \Delta B &= s_{B1}\Delta w_1 + s_{B2}\Delta w_2 + \dots + s_{BN}\Delta w_N \\ \Delta C &= s_{C1}\Delta w_1 + s_{C2}\Delta w_2 + \dots + s_{CN}\Delta w_N\end{aligned}\quad (4)$$

where ΔA is the change in performance A (e.g. bandwidth) from adjusting the width of transistor 1 (e.g. MP0) by Δw_1 , defined by the sensitivity of parameter A to a change in transistor 1, s_{A1} . Note that this sensitivity is not the same numerical value as found in Table II, which is a dimensionless value normalised to the nominal performance and to a $\pm 5\%$ change in transistor width. In order to evaluate the above equations, the sensitivity has to be de-normalised in both dimensions, resulting in a gradient with units, e.g. Hz/ μm .

Before the CAT technique can be applied to a circuit, the necessary ideal adjustment is computed first from a MC simulation of device parameter variation. The deviation of performances from their nominal values is used to solve Equation 4 for the necessary adjustment in transistor widths. The simulation is then repeated with the MC variables unaltered but the critical devices adjusted.

D. Application of Optimally Sized CATs

While the adjustment technique of Section II.C shows a significant improvement in performance, it is unrealistic because it assumes infinite granularity in the adjustment devices. In reality, a CAT consists of a finite number of calibration transistors. The optimal sizing algorithm for CAT [15] operates on statistical information of transistor width.

TABLE III - OPTIMAL SIZING OF THE CONFIGURABLE ANALOGUE TRANSISTORS

	MP3	MP0	MN7	
<i>Nominal width</i>	105.0 μm	8.75 μm	175.0 μm	
<i>CAT width step</i>	11.64 μm	0.743 μm	10.20 μm	
<i>CAT device</i>	<i>Main</i>	64.26 μm	6.150 μm	139.3 μm
	<i>1st</i>	11.64 μm	0.743 μm	10.20 μm
	<i>2nd</i>	23.28 μm	1.486 μm	20.40 μm
	<i>3rd</i>	46.56 μm	2.972 μm	40.80 μm

Each CAT is optimally sized by considering the distribution of required width adjustments shown in Figure 4. This results in an optimised final performance distribution because the distribution of width adjustment is directly related to circuit performance. Using the optimal sizing algorithm for CAT and assuming three calibration transistors in each critical device, the transistor sizes in Table IV have been calculated. To allow adjustment in both positive and negative direction, the nominal width of the main transistor M_0 is reduced and the three calibration transistors are sized to give eight evenly spaced selectable values centred on the original nominal width. After obtaining these transistor sizes, a further MC simulation is performed. Instead of adjusting devices with infinite granularity, the CAT configuration is used to constrain the adjustment to the eight selectable widths. This is equivalent to tuning the CATs on a chip after fabrication. The results of this therefore represent the performance obtained following post manufacture adjustment with optimally sized CATs.

III. RESULTS

In the case-study circuit, which is shown in Figure 3, MP0, MP3 and MN7 have been replaced with CATs, each with three calibration transistors sized according to Table IV. Figure 5 shows the histograms of the performances before and after application of the CATs. Clearly, the spread in all three performances is reduced significantly, resulting in a lower standard deviation and greater yield. Table V compares the standard deviations of the performances before and after application of the three CAT devices. The standard deviations are improved by 76.2%, 80.2% and 79.9% for gain, bandwidth and CMRR, respectively.

Table III-PERFORMANCE SENSITIVITY TO VARIATION IN TRANSISTORS

Device	Sensitivity (s)			Weighting (w)			Weighted Sensitivity (s')		
	Bandwidth	Gain	CMRR	Bandwidth	Gain	CMRR	Bandwidth	Gain	CMRR
MP5	0.0280	0.0159	0.0001	0.6361	0.3617	0.0022	0.0178	0.0058	0.0000
MP4	0.0057	0.0045	-0.0006	0.5297	0.4180	0.0523	0.0030	0.0019	0.0000
MP3	-0.0014	-0.0466	0.0000	0.0288	0.9712	0.0000	0.0000	-0.0452	0.0000
MP2	0.0634	-0.0128	0.0005	0.8263	0.1674	0.0063	0.0524	-0.0021	0.0000
MP1	0.0671	-0.0506	0.0003	0.5685	0.4285	0.0029	0.0381	-0.0217	0.0000
MP0	-0.1287	0.0996	-0.0007	0.5620	0.4351	0.0030	-0.0723	0.0433	0.0000
MN9	0.0001	0.0000	0.0000	1.0000	0.0000	0.0000	0.0001	0.0000	0.0000
MN8	0.0021	0.0468	0.0000	0.0422	0.9578	0.0000	-0.0002	0.0448	0.0000
MN7	-0.0048	-0.0019	0.0970	0.0467	0.0185	0.9348	-0.0007	0.0011	0.0907
MN6	-0.0015	0.0019	0.0000	0.4422	0.5577	0.0001	0.0292	-0.0019	0.0000
MN5	0.0370	-0.0095	-0.0004	0.7891	0.2031	0.0078	-0.0345	0.0001	0.0000
MN4	-0.0366	0.0019	0.0003	0.9429	0.0482	0.0089	0.0242	-0.0143	0.0000
MN3	0.0430	-0.0331	0.0002	0.5634	0.4336	0.0030	-0.0350	0.0202	0.0000
MN2	-0.0618	0.0470	-0.0003	0.5663	0.4307	0.0029	0.0005	0.0000	0.0000
MN1	-0.0006	-0.0001	0.0000	0.8699	0.1291	0.0010	0.0001	0.0000	0.0000
MN0	0.0001	-0.0001	0.0000	0.5648	0.4314	0.0038	0.0001	-0.0001	0.0000

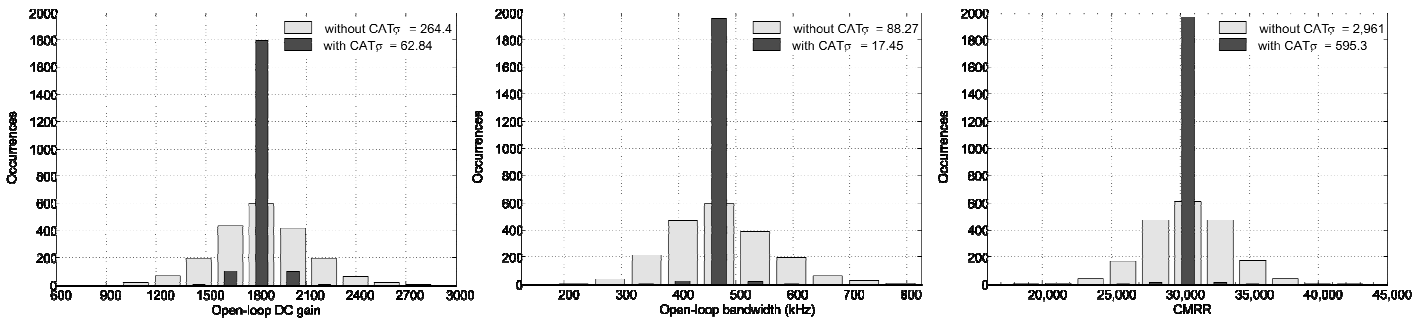


Figure 1. Histograms of circuit performances.

Table IV also shows the best theoretical improvement by applying the optimal CAT sizing algorithm in [15]. The theoretical maximum is almost impossible to achieve in practice because the relationship between CAT width and the performance it adjusts is unlikely to be perfectly linear. The results using CAT are remarkably close to the theoretical maximum improvement, indicating that the assumption of linear sensitivity is adequate for this particular combination of circuit, parameters and spread.

IV. CONCLUSIONS

The CAT technique provides a calibration platform that is independent of the target circuit and the mechanisms of performance variation. In this paper a novel automated method is proposed that determines which transistors in a circuit should be replaced with CAT devices in order to achieve maximum post fabrication yield improvement. It is demonstrated that both the performance sensitivity and the adjustment independence should be taken into account, giving a combined weighted sensitivity. In the case study, three critical devices were identified and replaced which led to an average of 78.8% improvement in the variability of key circuit performances. These results demonstrate that the proposed CDI methodology and performance driven CAT sizing can form a successful approach to improve analogue circuit yield.

TABLE IV- CIRCUIT PERFORMANCE AFTER APPLYING CAT

Condition	Performance			
		gain	BW	CMRR
Nominal	Mean	1.83×10^3	471×10^3	30.5×10^3
	Standard deviation	264	88.3×10^3	2.96×10^3
Adjustment with CAT	Mean	1.83×10^3	471×10^3	30.5×10^3
	Standard deviation	62.8	17.5×10^3	595
	Standard deviation improvement	76.2%	80.2%	79.9%
	Maximum standard deviation improvement	80.7%	80.8%	80.3%

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