A Complexity Adaptive Channel Estimator for Low Power

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***Abstract*—This paper presents a complexity adaptive channel estimator for low power. Channel estimation (CE) is one of the most computation intensive tasks in a software-defined radio (SDR) based OFDM demodulator. Complementary to the conventional low-power design methodology on processor architectures or circuits, we propose to reduce power also at the algorithm level. The idea is to dynamically scale the processing load of the channel estimator according to the run-time estimated channel quality. In this work, with a case study on China Mobile Multimedia Broadcasting (CMMB) standard, three practical CE algorithms are adopted to form a complexity scalable algorithm set, and signal noise ratio (SNR) is chosen to be the channel quality parameter for CE algorithm switching. In order to accurately estimate the SNR in the run-time, we also propose a noise variance estimation algorithm which is robust against fast-fading channels and introduces small computation overheads. Simulation shows that, under a pre-defined scenario for our targeting SDR demodulator, more than 50% run-time load reduction can be achieved compared with a fixed worst case channel estimator, while still fulfilling the mean square error requirement, resulting in about 25% of power reduction for the total demodulator. In addition, complexity adaption enables dynamical voltage and frequency scaling (DVFS) in a SDR demodulator which can lead to furthermore power reduction.**

I. INTRODUCTION

Software-defined radio (SDR) nowadays becomes attractive because of its high flexibility to be able to support multiple radio standards and multiple modes within one radio standard using the same hardware. A typical SDR receiver platform is shown in Figure 1, where the gray scale of a block shows the programmable flexibility. In this platform, the tuner receives radio frequency (RF) signals and applies frequency down-conversion. The digital front-end (DFE) samples the analog waveform into bits, performs pre-filtering and then sends the bits to a demodulator for baseband processing. The demodulated soft-bits are sent to a codec for de-interleaving and channel decoding. Eventually, the decoded bits are sent out as standard transport stream. Among the four blocks, the demodulator is typically realized by a vector DSP [1], which provides the highest programmable flexibility.

Compared with traditional ASIC solutions, the SDR based demodulator is more flexible but less power-efficient. Currently, most of the low-power SDR demodulator design focus on efficient processor architectures [2] [3] or low-power circuits, while the baseband processing algorithms in the demodulator are fixed and designed only for the worst case wireless channel condition.

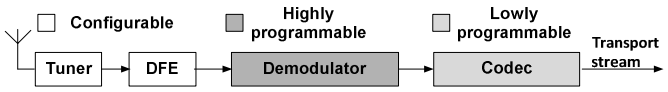

Figure 1. A typical SDR receiver platform

Complementary to the conventional low-power design methodology on processor architectures or circuits, we propose to dynamically adapt the computation complexity of the baseband processing algorithms according to the fluctuating wireless channel qualities: when the channel quality is high, light loaded baseband processing algorithms are adopted for power saving. When the channel quality is poor, heavy loaded baseband processing algorithms are adopted to guarantee the reception quality. Benefited from the nature of SDR, switching among a set of baseband processing algorithms only introduce the increment of the code size, but the computation hardware cost keeps unchanged. The concept of complexity adaption is inspired from the complexity scalable motion estimation (ME) algorithms in resource-limited and low-power video processing systems [4] [5] which play trade-offs between video quality and algorithm complexity. The major difference in our case is that we exploit the dynamics of the wireless channel quality so that there is no sacrifice for the reception quality.

In this work, based on the assumption that power consumption is proportional to the computation load, we propose a complexity adaptive channel estimator for the low-power demodulator design at the algorithm level. To enable complexity adaptation, we also propose a run-time noise variance estimation algorithm which introduces little computation overhead and can accurately estimate the channel quality even for fast fading channels. We evaluate the performance of our run-time complexity adaptive channel estimator by simulation under a pre-defined scenario. The simulation shows that more than 50% run-time load reduction can be achieved compared with a fixed worst case channel estimator, resulting about 25% power reduction for our targeting SDR demodulator. The work targets at the CMMB standard, a digital TV broadcast standard in China, and focuses

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978-3-9810801-8-6/DATE12/©2012 EDAA

on channel estimation (CE), one of the most computation intensive tasks in a CMMB demodulator. For generalization, the concept can also be applied to other OFDM systems (e.g. 802.11n) and other baseband processing tasks (e.g. the equalizer) for the low-power demodulator design.

The remaining parts are organized as follows: In Sec. II the system model is presented. In Sec. III the architecture and algorithms of our complexity adaptive channel estimator for CMMB are presented. In Sec. IV the performance of our complexity adaptive channel estimator is evaluated. Finally in Sec.V conclusions and future research work are discussed.

II. SYSTEM MODEL

A. CMMB Standard

CMMB is a digital TV broadcast standard in China. It adopts OFDM as the modulation scheme at the physical layer [6]. The CMMB data stream is organized by frames. Each frame lasts for 1s and consists of 40 time slots (TS). Each TS lasts for 25ms, which is headed with a preamble and then followed by 53 OFDM data blocks. Each CMMB preamble contains two synchronization signals, which are modulated through inverse fast Fourier transform (IFFT) by 2 identical PN sequences with the unit power. The CMMB frame structure is shown in Figure 2. The CMMB spectrum structure is shown in Figure 3, where the usable-subcarriers are guarded by null-subcarriers at two side bands. In order to enable channel estimation, the unit-valued scattered pilots (SP), are inserted within the useable-subcarrier band, which subsample the frequency domain channel transfer function (CTF). The interlaced pattern of SPs is shown in Figure 4.

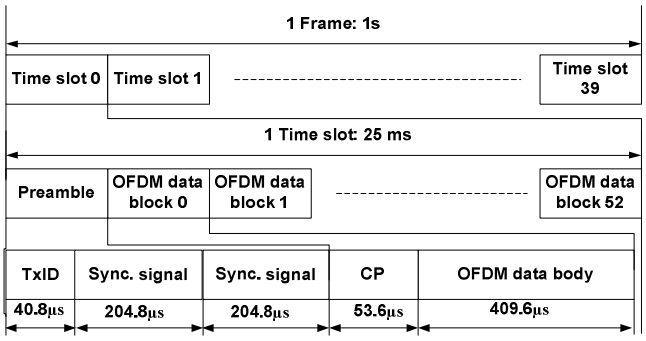

Figure 2. CMMB frame structure

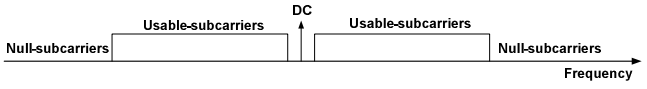

Figure 3. CMMB spectrum structure

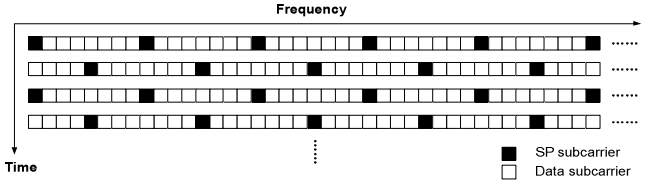

Figure 4. SP pattern within the usable-subcarrier band

B. Baseband Model

The baseband model for CMMB is similar to many OFDM systems such as DVB-T and 802.11n, shown in Figure 5, and can be divided into three parts: the transmitter, the fading channel with additive noise, and the receiver.

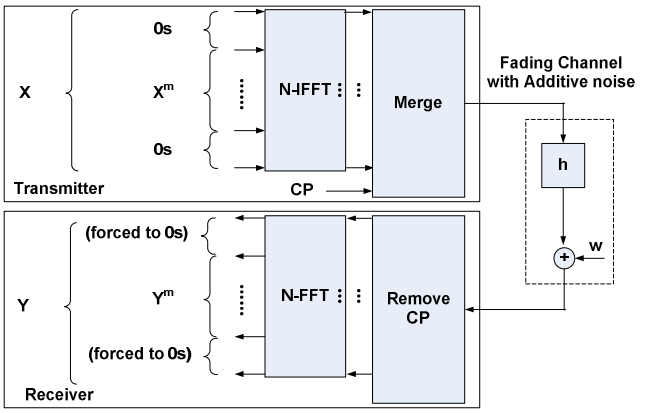

Figure 5. CMMB baseband model

In the transmitter, $\mathbf{X}^{\mathbf{m}}$ is the data sequence to be transmitted, with the length of N_m. It's guarded with null-subcarriers on its two sides for band protection. The total sequence $\mathbf{X}$ is called the frequency domain signal and has the length of N. $\mathbf{X}$ is transformed into the time domain by N-point IFFT. After insertion of cyclic prefix (CP), a time domain OFDM block is generated. During the transmission, it's further faded with a multi-path channel $\mathbf{h}$ and added with additive Gaussian white noise $\mathbf{w}$. In the receiver, CP is removed and the received OFDM block is transformed back into the frequency domain by N-point fast Fourier transform (FFT). Assume that the synchronization is perfect and that the delay spread of the multi-path channel is shorter than CP length: G, then the received useable-subcarrier sequence $\mathbf{Y}^{\mathbf{m}}$ can be expressed as:

$$\mathbf{Y}^{\mathbf{m}}(k) = \mathbf{H}^{\mathbf{m}}(k) \cdot \mathbf{X}^{\mathbf{m}}(k) + \mathbf{W}^{\mathbf{m}}(k) \tag{1}$$

where $k \in [0, N_m - 1]$, and $\mathbf{H}^{\mathbf{m}}$ is the CTF within the useable-subcarrier band.

In particular, the received SPs can be expressed as:

$$\mathbf{Y}^{\mathbf{m}}(\mathbf{P}(k)) = \mathbf{H}^{\mathbf{m}}(\mathbf{P}(k)) + \mathbf{W}^{\mathbf{m}}(\mathbf{P}(k)) \tag{2}$$

where $\mathbf{P}$ is the pattern vector storing SP indexes.

For the CMMB preamble, the received synchronization signals after FFT can be expressed in the following form:

$$\begin{aligned} \mathbf{Y}_1^{\mathbf{m}}(k) &= \mathbf{H}_1^{\mathbf{m}}(k) \cdot \mathbf{X}_{PN}^{\mathbf{m}}(k) + \mathbf{W}_1^{\mathbf{m}}(k) \\ \mathbf{Y}_2^{\mathbf{m}}(k) &= \mathbf{H}_2^{\mathbf{m}}(k) \cdot \mathbf{X}_{PN}^{\mathbf{m}}(k) + \mathbf{W}_2^{\mathbf{m}}(k) \end{aligned} \tag{3}$$

where $k \in [0, N_m - 1]$ and $\mathbf{X}_{PN}^{\mathbf{m}}$ is the pre-defined PN sequence.

In the system model, one further assumption is that, the SNR stays constant within one CMMB TS (25ms). The

assumption is reasonable because the change of SNR is normally caused by the change of environment temperature, or due to physical movement. Within 25ms, those changes can be seen negligible.

III. The Architecture and Algorithms

A. System Architecture

The system architecture of our complexity adaptive channel estimator is shown in Figure 6, which is in a feed-forward form. In this architecture, the preamble of each CMMB TS is reused for channel quality estimation (CQE). A typical channel quality parameter is SNR, which is chosen in our design. According to the estimated SNR, one CE algorithm is selected for channel estimation for the subsequent 53 OFDM blocks in the current TS.

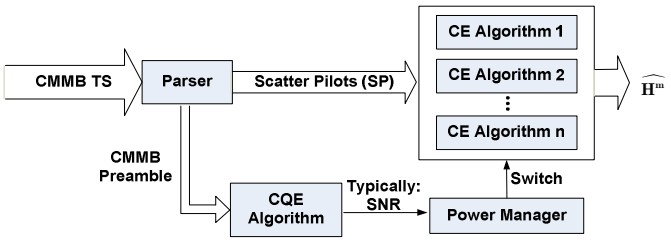

Figure 6. System architecture in a feed-forward form

As an alternative, the complexity adaptive channel estimator can also be designed in the feedback architecture which directly uses the measured bit error rate (BER) at the channel decoder output to indicate the channel quality. However, a large data set is required to measure a very small BER (For CMMB with $BER \le 3\times10^{-6}$, it means more than 0.33 mega payload bits should be evaluated which last for more than 10 CMMB time slots). Therefore, the estimated BER does not indicate an immediate channel quality for the current TS but only an average channel quality during a past time interval. The length of the interval is determined by the interleaving depth and the size of BER measurement data set, and is much longer than one CMMB TS. Compared with the feedback architecture, the feed-forward architecture can rapidly track the fluctuating channel quality so that it's more suitable in our run-time scenario and no history data needs to be buffered. To enable the feed-forward architecture in Figure 6, a set of CE algorithms with scalable load and scalable estimation accuracies are required. Also an efficient CQE algorithm is required which can accurately estimate the SNR in the run-time and should introduce small computation overhead. They are described in the following two subsections respectively.

B. Scalable CE Algorithms

To explore the scalability, three CE algorithms are chosen: linear interpolating estimation (LI) [7], mismatched Wiener filtering estimation (MWF) [8], and time domain least square estimation (TD-LS) [9]: LI is the simplest method to estimate the CTF using received SPs. This is done by making weighted summation of two nearest SPs, where the weights are inversely proportional to the distance; MWF is a low-pass finite impulse response (FIR) filter. The filtering coefficients are offline determined by a mismatched channel impulse response (CIR), which has uniform gain on each channel tap within a pre-defined maximal delay spread; TD-LS aims to compute a LS estimate of time domain CIR and then transform the estimated CIR back into the frequency domain. The computation of the CIR estimate involves with a multiplication of an ill-conditioned decorrelation matrix [9]. This problem is solved by applying truncated singular value decomposition (TSVD) on the ill-conditioned decorrelation matrix, so that a suboptimal lower-rank matrix approximation with a far smaller condition number is obtained [10]. These three CE algorithms are chosen because of their scalability in both performance and computation complexity, and also because of their practicability: the main operations are multiply-additions, FIR filtering, FFT and IFFT, which are easy to be vectorized and realized in a programmable vector DSP.

To analyze the performance scalability, the mean square error (MSE) under different SNRs for different CE algorithms is shown in Figure 7. In this comparison, typical urban 6-tap channel (TU6) is used with Doppler frequency at 10Hz. TU6 is specified by commission of the European Communities [11] and is adopted as the reference channel model in the CMMB standard. We see that the performance gap between TD-LS and 6-tap MWF is about 3dB and the gap between MWF and LI is also about 3 dB. Also in the Figure 7, the thresholds for CE algorithms can be obtained under a given MSE requirement. In this case, the MSE requirement is set to be 0.018, which is an experimental value below which the decoded video provides satisfactory reception quality. By examining the intersection points, the thresholds for CE algorithm selection can be derived: when the SNR is smaller than 12.6dB, TD-LS must be selected in order to guarantee the MSE requirement; when the SNR is between 12.6dB and 15.6dB, MWF is selected to fulfill the MSE requirement; and when the SNR is higher than 15.6dB, LI is sufficient. In real implementations, the SNR thresholds can also be right-shifted so as to avoid optimistic decisions caused by SNR estimation errors, which is a tradeoff between the power saving factor and the robustness.

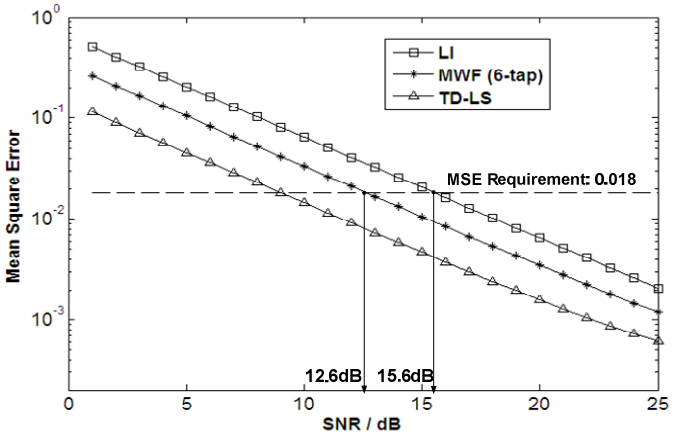

Figure 7. Performance scalability of CE algorithms

To analyze the computation complexity scalability, the number of arithmetic operations per OFDM block in CMMB 1K mode for the three CE algorithms is shown in Table I. We

see that they scale well. For example, the number of complex additions of LI is only 2% of that of TD-LS. And the number of complex additions of 6-tap MWF is about 19% of that of TD-LS.

TABLE I. PROFILINGS OF THREE CE ALGORITHMS

Algorithms	Complex Additions	Complex Multiplications
LI	472	472
MWF (6-tap)	3984	3984
TD-LS	21504	8704

Based on above analysis, the selected three CE algorithms scale well in both performance and computation complexity.

C. The CQE Algorithm

The CQE algorithm aims to estimate the SNR using the CMMB preamble in (3). A key step to estimate SNR is to estimate the noise variance. Noise variance estimation suffers from the fading of CTF. Many existing noise variance estimation approaches need the estimate of channel statistics as a prerequisite [12] [13], which are computation intensive and the performance depends on the accuracy of channel statistics estimates. [14] proposes a noise variance estimation approach by using cyclic prefix (CP). It needs no channel statistics, but the estimate needs thousands of OFDM blocks to be accurate, therefore not applicable for our run-time scenario. [15] proposes an approach by making difference of the two identical adjacent OFDM blocks in the synchronization preamble. It is robust against frequency selective channel but is only applicable when the channel is time-invariant. When the channel is fast fading, however, the estimated noise variance is enlarged. [16] proposes another approach, taking the fact that the maximal delay of channel taps stays within the length of cyclic prefix (CP), so that the noise subspace and the channel subspace can be decoupled by IFFT. However, in the null-subcarrier modulated OFDM systems as CMMB, the reconstructed CIR has the energy leaked into the delay paths longer than the CP length [17]. As a result, the estimated noise variance is again enlarged.

The proposed approach combines the ideas in [15] and [16], so as to resolve the problems introduced by both of them. Consider the preamble structure in (3), the two training OFDM blocks are first multiplied by the conjugated version of the unit-power PN sequence $\mathbf{X}_{PN}^{\mathbf{m}}$, in the following form:

$$\begin{aligned}\mathbf{Y}^{\mathbf{m}\prime}(k) &= \mathbf{Y}_n^{\mathbf{m}}(k)\cdot\mathbf{X}_{PN}^{\mathbf{m}}(k)^* \\ &= \mathbf{H}_n^{\mathbf{m}}(k)\cdot|\,\mathbf{X}_{PN}^{\mathbf{m}}(k)\,|^2 + \mathbf{W}_n^{\mathbf{m}}(k)\cdot\mathbf{X}_{PN}^{\mathbf{m}}(k)^* \\ &= \mathbf{H}_n^{\mathbf{m}}(k) + \mathbf{W}_n^{\mathbf{m}\prime}(k) \\ &0\le k\le N_m-1;\ n=1\ or\ 2.\end{aligned} \tag{4}$$

where $\mathbf{W}_n^{\mathbf{m}\prime}$ is still white noise with the same variance as $\mathbf{W}_n^{\mathbf{m}}$.

Then, $\mathbf{Y}_1^{\mathbf{m}\prime}$ and $\mathbf{Y}_2^{\mathbf{m}\prime}$ are both transformed into the time domain by N-point IFFT as:

$$\mathbf{y}_n^{\mathbf{m}\prime} = IFFT(\mathbf{Y}_n^{\mathbf{m}\prime}, N) = \mathbf{h}_n^{\mathbf{m}} + \mathbf{w}_n^{\mathbf{m}\prime},\ n=1\ or\ 2 \tag{5}$$

In order to remove the leaked channel taps, we further make difference of the long delay paths of $\mathbf{y}_1^{\mathbf{m}\prime}$ and $\mathbf{y}_2^{\mathbf{m}\prime}$ in the following form:

$$\Delta\mathbf{y}(k) = \mathbf{y}_1^{\mathbf{m}\prime}(k) - \mathbf{y}_2^{\mathbf{m}\prime}(k),\ G\le k\le N-G-1 \tag{6}$$

In (6), the long delay paths of $\mathbf{y}_1^{\mathbf{m}\prime}$ and $\mathbf{y}_2^{\mathbf{m}\prime}$ consist of two parts: the leaked channel taps and the noise. And such differencing operation in the time domain long delay paths has the following effects:

- For the part of the leaked channel taps: when the channel taps of adjacent OFDM blocks are time-invariant, the leaked energy can be totally removed by differencing; when the multi-path channel is fast fading, there is extra energy which is introduced by the channel difference. However, IFFT migrates the majority of such extra energy into the low delay paths so that the effect of fast-fading is greatly reduced. Also, the channel leakage energy in long delay paths is inhibited because the channel taps in adjacent OFDM blocks are still correlated.
- For part of the noise: based on the fact that differencing two Gaussian variables results in a new Gaussian variable with twice of variance, the noise energy is magnified, which also helps to improve the estimation precision.

Therefore, the noise variance can be estimated as:

$$\widehat{\sigma_W^2} = \frac{1}{2}\sigma^2(\Delta\mathbf{y}) = \frac{N}{2N_m(N-2G)}\sum_{k=G}^{N-G-1}(|\,\mathbf{y}_1^{\mathbf{m}\prime}(k)-\mathbf{y}_2^{\mathbf{m}\prime}(k)\,|^2) \tag{7}$$

Using the estimated noise variance, the SNR estimate can be immediately computed as:

$$\widehat{SNR} = 10\lg\frac{\sigma^2(\mathbf{Y}_n^{\mathbf{m}})-\widehat{\sigma_W^2}}{\widehat{\sigma_W^2}},\ n=1\ or\ 2 \tag{8}$$

IV. RESULTS AND DISCUSSIONS

A. Performance Evaluation of the CQE Algorithm

The proposed noise variance and SNR estimation algorithm is evaluated by comparing with the approaches in [15] and [16]. The simulation is run under TU6 channel in two modes: the slow fading mode with the Doppler frequency at 1Hz, and the fast fading mode with the Doppler frequency at 250Hz. Figures 8 and 9 show the relationships between the actual SNR and the estimated SNR in the two modes: the ideal curve should be a line with slope of 45°, which is the solid line. The curve labeled with "FD-Diff" stands for the frequency domain differencing approach in [15]; The curve labeled with "TD-Naive" stands for the time domain de-coupling approach in [16]; And the curve labeled with "TD-Diff" stands for the proposed approach by time domain differencing.

In the slow fading mode, we see that the both TD-Diff and FD-Diff coincide with the ideal curve, while TD-Naive falls below the ideal curve. That's because in the slow fading mode, the CTF during the adjacent two OFDM blocks is constant and the differencing in time domain and frequency domain can both remove the total channel energy. For TD-Naive, however, the leaked channel energy into the noise subspace enlarges the estimated noise variance; In the fast fading mode, we see that TD-Naive is still below the ideal curve because the leaked channel energy still exists which enlarges the estimated noise variance. However, we also see that FD-Diff drops even lower, that is because when fast fading, the difference between CTFs in adjacent OFDM blocks enlarges the estimated noise variance. We can also see that the proposed TD-Diff still keeps close to the ideal curve, showing the robustness against fast fading channels.

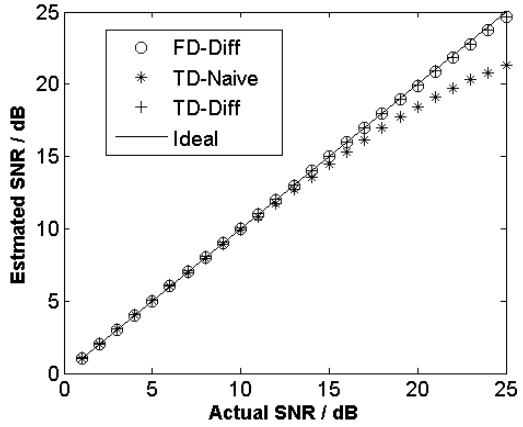

Figure 8. SNR estimation results under slow fading channel

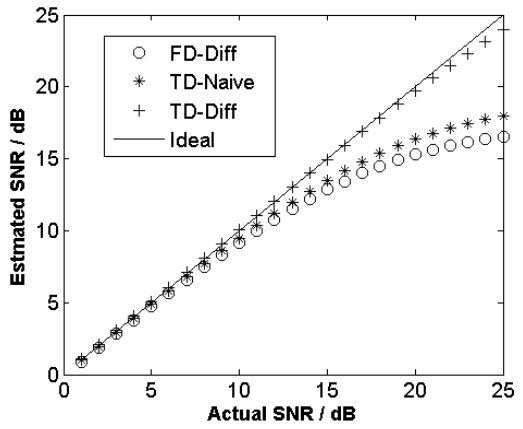

Figure 9. SNR estimation results under fast fading channel

B. *Load Profile*

To verify the complexity scalability in a real SDR demodulator, the derived CE algorithms and CQE algorithm are mapped onto the VectraLx digital signal processor (VDSP) [18] in our targeting SDR receiver platform. VDSP is a programmable vector processor which combines the very long instruction word (VLIW) and single instruction multiple data (SIMD) to explore the both instruction-level parallelism and the data-level parallelism. For algorithm mapping, the main contributors to the number of computation cycles are FFT, IFFT and FIR filtering. For TD-LS, the FFT and the IFFT are separately reused once. For MWF, a 6-tap FIR filtering is reused for four times. For the SNR estimation, the IFFT is reused twice.

The normalized cycle numbers obtained from the VDSP simulator for each algorithm module are showed in Figure 10, including the computation overheads for SNR estimation and the power manager. Note that the cycle number of the computation overheads is further normalized by a factor of 1/53. That is because the execution frequency of CQE algorithm is 1/53 of that of CE algorithm.

In Figure 10 we see that the loads of three CE algorithms in VDSP scale as expected. The processing load of 6-tap MWF is roughly 33% of that of TD-LS. And the processing load of LI is roughly 8% of TD-LS. These two ratios are higher than the theoretical estimated ratios (19% and 2%), meaning that TD-LS better fits VDSP. That is because, benefited from the hardware function unit of radix-4 FFT butterfly within the VDSP core, FFT and IFFT computations are more efficient. In Figure 10 we can also see that the computation overheads introduced by the CQE algorithm and the power manager is only 1.78% of TD-LS, which is almost negligible.

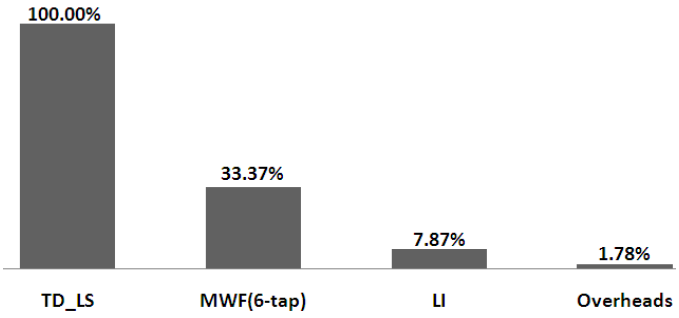

Figure 10. Load profile of CQE and CE algorithms in VDSP

The algorithm modules of our complex adaptive channel estimator are integrated into a *Matlab* test bench and the obtained load profile for the algorithm modules is inserted into the test bench for integrated simulation. The simulation scenario is specified in Table II.

TABLE II. SCENARIO FOR INTEGRATGED SIMULATION

Parameters	Settings
Channel model:	TU6 channel
Doppler frequency:	10Hz
FFT size:	1024 (CMMB 1K mode)
Equalizer type:	Zero-forcing Equalizer
Mapping scheme:	4-QAM
MSE requirement:	≤ 0.018
SNR assumption:	Constant within 25ms
SNR distribution:	Uniform distribution (11dB~20dB)

The simulation is performed over a sample set of 2000 CMMB time slots. Figure 11 shows the normalized average cycle counts per TS in 4 different CE algorithm configurations, where the grey scale proportions in each column reflect the cycle contribution of different algorithm modules, including the computation overheads. We see that, under the simulation scenario, compared with a fixed worse case channel estimator (TD-LS), the maximal run-time load reduction factor is 55 % (100% - 45% = 55 %). Furthermore, the power saving for the total CMMB demodulator can be estimated: in our implementation, the worst case channel estimator (TD-LS) takes about 50% of the total load for baseband processing in VDSP (the other 50% loads include the processing tasks for FFT, frequency and time tracking, zero-forcing equalization and soft-bits de-mapping). And therefore our complexity adaptive channel estimator can achieve about 25% power saving for the VDSP demodulator. This saving factor is under the fixed supply voltage and can be even larger when the load reduction is further exploited by reducing the supply voltage using dynamical voltage and frequency scaling (DVFS) [19].

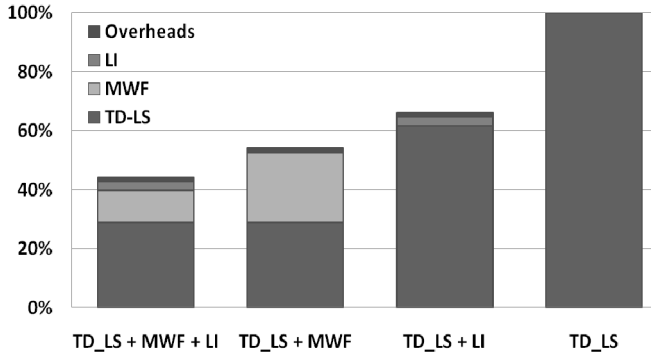

Figure 11. Normalized average cycle number per CMMB TS

CONCLUSION AND FURTHER WORK

In this paper, we present a complexity adaptive channel estimator for low power SDR demodulators. The idea is to run-time scale the processing load of the channel estimator according to the run-time estimated SNR, so as for the run-time load reduction and power saving. We proposed a feed-forward architecture in order to rapidly track the fluctuating channel quality. We adopted 3 practical CE algorithms to form a scalable algorithm set. With a case study on CMMB, we analyzed and verified the scalability of the algorithm set on our targeting SDR platform. We also proposed a noise variance and SNR estimation algorithm by differencing two synchronization signals of CMMB preamble in the time domain long delay paths. It can accurately estimate the SNR even under fast fading channels and introduces small computation overheads. We verified the idea by simulation under a pre-defined scenario for our targeting SDR platform. The simulation shows that more than 50% run-time load reduction can be achieved compared with a fixed worse case channel estimator, while still fulfilling the MSE requirement. It leads to about 25% of power-saving of the whole demodulator. This results in a longer battery life in high SNR channels while maintaining satisfactory reception quality in poor SNR channels.

Currently we are working on combining the complexity adaptive architecture with DVFS in VDSP, to exploit the load reduction for further power reduction.

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