Asymmetry of MTJ Switching and Its Implication to STT-RAM Designs

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***Abstract*—As one promising candidate for next-generation nonvolatile memory technologies, spin-transfer torque random access memory (STT-RAM) has demonstrated many attractive features, such as nanosecond access time, high integration density, non-volatility, and good CMOS process compatibility. In this paper, we reveal an important fact that has been neglected in STT-RAM designs for long: the write operation of a STT-RAM cell is asymmetric based on the switching direction of the MTJ (magnetic tunneling junction) device: the mean and the deviation of the write latency for the switching from low- to high-resistance state is much longer or larger than that of the opposite switching. Some special design concerns, e.g., the write-pattern-dependent write reliability, are raised by this observation. We systematically analyze the root reasons to form the asymmetric switching of the MTJ and study their impacts on STT-RAM write operations. These factors include the thermal-induced statistical MTJ magnetization process, asymmetric biasing conditions of NMOS transistors, and both NMOS and MTJ device variations. We also explore the design space of different design methodologies on capturing the switching asymmetry of different STT-RAM cell structures. Our experiment results proved the importance of full statistical design method in STT-RAM designs for design pessimism minimization.**

I. Introduction

Conventional memory technologies, i.e., SRAM, DRAM, and Flash, have achieved a remarkable success in modern electronic industry. As the semiconductor fabrication technology approaches 20nm range, the disadvantages of those technologies has become more and more prominent, i.e., the high leakage power of SRAM and DRAM, the poor endurance performance of NAND Flash, and the generally degraded device reliability. Hence, the research on emerging memory technologies have been triggered to look for alternative process scaling paths. As a promising candidate, spin-transfer torque random access memory (STT-RAM) aims the embedded memory and on-chip cache applications [7], [10], [11]. In an STT-RAM cell, data is stored as the resistance states of a magnetic tunneling junction (MTJ) device [2]. Compared to other competing technologies such as Phase-Change RAM (PCRAM), Resistive RAM (RRAM) and Ferromagnetic RAM (FeRAM), STT-RAM offers faster (nanoseconds) read access time, better CMOS process compatibility, as well as the common properties such as zero standby power, small memory cell size, and good scalability etc. [6].

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A well-known issue in STT-RAM designs is the high write cost: a long write pulse width, i.e., 10ns or longer, is required to flip the MTJ resistance [4]. Many circuit design and architecture level solutions have been proposed to alleviate this issue, including increasing the size of driving transistors [9], overdriving the word-line voltage [1], adding the write buffers [10] and hybrid memory design with both SRAM and STT-RAM [3].

Some studies have been performed to analyze the impacts of process variation effects: Wang, et al. has discussed the thermal fluctuation on MTJ devices [8]; Xu, et al. has analyzed the effects of proccess variations of CMOS transistor in STT-RAM [9]; and Sumllen et al. developed a thermal noise model to evaluate the thermal fluctuations during the MTJ resistance switching process [5].

In this work, we reveal an important fact that has not received enough attentions in STT-RAM designs and applications: the write mechanism of STT-RAM cells is highly asymmetric at different switching directions, i.e., 0→1 and 1→0. Specifically, the switching of 0→1 takes longer time than 1→0 at the same switching current while suffering from the larger variations. This asymmetry can be further aggravated by the different biasing conditions of the driving NMOS transistor at different switching directions, and the device variations of both MTJ and NMOS transistors. The existing works either do not consider the asymmetric thermal fluctuation induced switching variations, or the impact of thermal fluctuations on the asymmetric switching behavior of STT-RAM cell.

Therefore, we systematically analyze the asymmetry of STT-RAM cell write operations and its implication to the performance and reliability of memory cell write operations. We also investigate the possibility to minimize the design space pessimism that required to tolerate the asymmetry and the variations of STT-RAM write operations, by optimizing the design methodologies. Compare to previous works, we not only discussed the asymmetry of the variation of thermal fluctuation, but also evaluation the asymmetry of thermal fluctuation and process variation in a STT-RAM cell where both MTJ and CMOS variations are taken into account.

The rest of the paper is organized as follows: Section II gives the preliminary on STT-RAM basics; Section II investigates the contributors to the asymmetric STT-RAM write operations and write error rates at different switching directions

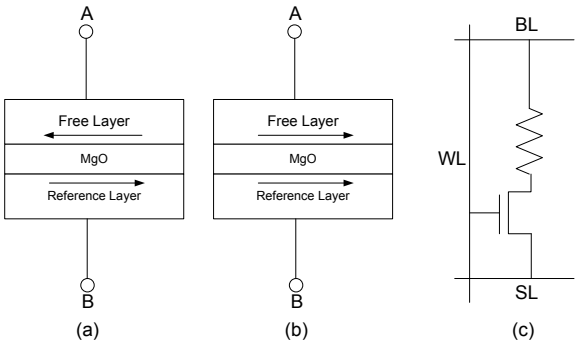


Fig. 1. MTJ Structure (a) Anti-parallel (high resistance state). (b) Parallel (low resistance state). (c) 1T1J STT-RAM cell structure.

by considering the thermal fluctuations and device variations; Section IV compares the design outcomes of different design flows and analyzes the impacts of the statistical switching property of STT-RAM cell on the write reliability; Section V discusses the write operations of "bottom-to-tup" STT-RAM cell structure; Section VI concludes our work.

II. Preliminary

A. STT-RAM Basics

Spin-transfer torque random access memory (STT-MRAM) uses magnetic tunneling junction (MTJ) devices to store the information. A MTJ has two ferromagnetic layers (FL) and one oxide barrier layer (BL). The resistance of MTJ depends on the relative magnetization directions (MDs) of the two FLs. When their MDs are parallel or anti-parallel, the MTJ is in its low or high resistance state, as illustrated in Fig. 1. R_h and R_l are usually used to denote the high and the low MTJ resistance, respectively. Tunneling magneto-resistance (TMR) is defined as $(R_h - R_l)/R_l$, which presents the distinction between the two resistance states.

In a MTJ, the MD of one FL (reference layer) is pinned while the one of the other FL (free layer) can be flipped by applying a polarized write current though the MTJ. For example, the switching from low resistance state ('0') to high resistance state ('1') can be realized by applying a current from B to A, as shown in Fig. 1. A larger write current can shorten the MTJ switching time by paying the additional memory cell area overhead: In the popular "1T1J" (one-transistor-one-MTJ) cell structure (see Fig. 1(c)), the MTJ write current is supplied by the NMOS transistor. Increasing the write current requires a larger NMOS transistor. Also, the increased write current raises the breakdown possibility of the MTJ device.

B. Asymmetry of STT-RAM Write Operations

The asymmetry of STT-RAM write operations mainly comes from two sources: the asymmetric MTJ switching property and NMOS transistor driving ability at two switching directions.

1) Asymmetry of MTJ switching: The asymmetry of MTJ switching at two switching directions, i.e., 0→1 and 1→0, is mainly due to the different spin-transfer efficiency η at the both sides of the oxide barrier. For example, when the MTJ works at a long switching time region (>10ns), the MTJ switching threshold current density can be calculated as [6]:

$$J_{C0} = (\frac{2e}{\hbar})(\frac{\alpha}{\eta})(t_F M_s)(H_k \pm H_{ext} + 2\pi M_s) \quad (1)$$

Here, J_{C0} is the minimal current density that causes the MTJ resistance flipping in the absence of any external magnetic field at 0K. e is the electron charge. α is the damping constant, M_s is the saturation magnetization, t_F is the thickness of the free layer, $\hbar$ is the reduced planck's constant, H_k is the effective anisotropy field including magneto crystalline anisotropy and shape anisotropy, H_{ext} is the external field.

We note that the spin-transfer efficiency η is determined by the relative MDs of two FLs as:

$$\eta = (P/2)/(1 + P^2 cos\theta). \quad (2)$$

Here P is the tunneling spin polarization. θ is the angle between the MDs of two FLs. Combining Eq. (1) and (2), we have:

$$\frac{J_{C0}^{0\to1}}{J_{C0}^{1\to0}} = \frac{1+P^2}{1-P^2}, \quad (3)$$

where $J_{C0}^{0\to1}$ and $J_{C0}^{1\to0}$ denotes the MTJ switching threshold current density at the switching of 0→1 and 1→0, respectively.

2) Asymmetry of transistor driving ability: The driving ability of NMOS transistor is also asymmetric due to the different bias conditions at two STT-RAM cell switching directions. For example, when writing '0', Word-line(WL) and Bit-line(BL) are connected to V_{dd} and Source-line(SL) is connected to ground. The V_{gs} of the NMOS transistor is V_{dd} while the V_{gs} equals $V_{dd} - I_{MTJ} \cdot R_{MTJ}$, where I_{MTJ} is the write current through the MTJ and R_{MTJ} is the MTJ resistance. When writing '1', WL and SL are connected to V_{dd} and BL is connected to ground. The V_{gs} of the NMOS transistor is reduced down to $V_{dd} - I_{MTJ} \cdot R_{MTJ}$ which leads to a low driving ability. We note that MTJ switching is mainly determined by the driving ability of the NMOS transistor before θ crosses 90°. In the above expressions, R_{MTJ} equals R_l or R_h at the switching directions of $0 \to 1$ or $1 \to 0$, respectively.

C. MTJ Switching Time Variations

Obviously the current through the MTJ is affected by the device variations of the MTJ and NMOS transistor. For instance, the driving ability of the NMOS transistor is affected by the variations of transistor channel length (L)/width (W) and the threshold voltage (V_{th}). The MTJ resistance R_{MTJ}, which determines the voltage drop across the MTJ device, is reversely proportional to the MTJ surface area and exponential to the oxide layer thickness. The fluctuations of the above device parameters in the chip fabrication introduce the bit-to-bit variations of STT-RAM cells.The operation errors that are incurred by pure device parameter variations can be repeated and categorized as "persistent" error [8].

We note that the normally distributed localized fluctuation of magnetic anisotropy $K = M_s \cdot H_k$ also affects the MTJ switching threshold current density, as shown in Eq. (1).

However, we ignore the impacts of magnetic anisotropy in our STT-RAM cell level analysis because it is related to the deposition of magnetic thin film and better considered as a systematic variation.

The magnetization switching of a MTJ can be modeled by the stochastic Landau-Lifshitz-Gilbert (LLG) equation as:

$$\frac{d\vec{m}}{dt} = \vec{m}\times(\vec{h}_{eff}+\vec{h}_{fluc})-\alpha\vec{m}\times(\vec{m}\times(\vec{h}_{eff}+\vec{h}_{fluc}))+\frac{\vec{T}_{norm}}{M_s} \quad (4)$$

Here $\vec{h}_{fluc}$ is the normalized thermal agitation fluctuating field. Under the intrinsic thermal fluctuations, the MTJ switching time becomes unrepeatable and follows a distribution. As we shall show in the next Section, this distribution is also affected by the MTJ and NMOS transistor device variations and causes the asymmetric STT-RAM cell switching at two switching directions.

III. Writing Errors of a STT-RAM Cell

A. Asymmetric MTJ Switching

Fig. 2 shows our simulation results of the MTJ switching current vs. the mean and the standard deviation of the MTJ switching time. The device parameters are extracted from a 45nm×90nm elliptical MTJ device, which have been calibrated with the measurement data of a real fabricated device from a leading magnetic recording company. The results of both switching directions ($1\rightarrow0$ and $0\rightarrow1$) are depicted. As discussed in Section II-B1, the distinction between the mean of the MTJ switching time of two switching directions under the same switching current can be explained as the asymmetric impacts of tunneling spin polarization P (see Eq. (3)). The different standard deviations of the MTJ switching time at two switching directions, however, is caused by the asymmetric influences of the thermal agitation fluctuating field $\vec{h}_{fluc}$, as shown in Section II-C. Larger MTJ switching time deviation is observed in $0\rightarrow1$ switching than $1\rightarrow0$ switching.

We noticed that when the MTJ works at long switching time (>40ns) under a low switching current, the standard deviation of the MTJ switching time for both switching directions are almost the same. However, following the decreasing of the MTJ switching time, the standard deviation difference of the MTJ switching time becomes prominent. It is due to the reduced thermal impacts and the increased asymmetry of the spin torque term $\vec{T}_{norm}$ in MTJ switching under a high switching current. In general, MTJ switching time has a larger mean and a wider distribution in $0\rightarrow1$ switching than $1\rightarrow$ switching under the same switching current.

TABLE I
Summary of Device Parameters

Device	Parameters	Mean	Std. Dev.
Transistor	Channel Length L	45nm	2.25nm
	Channel Width W	design dependent	2.25nm
	Threshold Voltage V_{th}	0.466V	δV_{th0}=30mV
MTJ	MgO Thickness τ	2.2nm	2% of mean
	Cross Section A	$45\times90nm^2$	5% of mean
	Low Resistance R_l	1000Ω	
	High Resistance R_h	2000Ω	

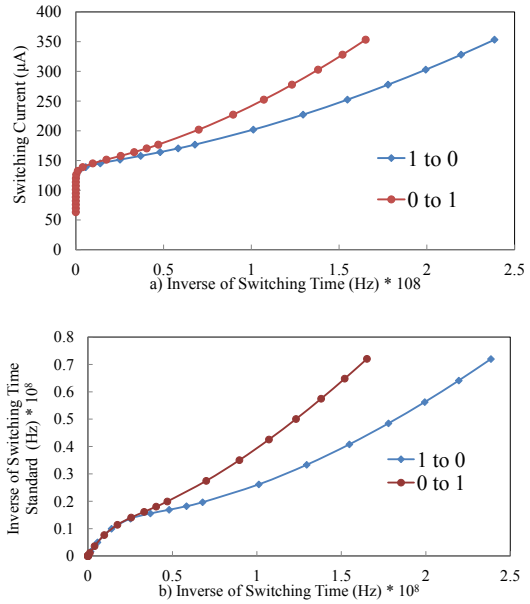


Fig. 2. (a) Switching current vs. Switching time mean. (b) Switching time mean vs. Switching time standard deviation.

B. Asymmetric Transistor Driving Ability

The MTJ write current decides the mean of the MTJ switching time distribution. The MTJ write current itself, however, is determined by the NMOS transistor driving ability under the bias conditions of two STT-RAM cell switching directions while subject to the device variations.

We conducted the Monte-Carlo simulations to obtain the distributions of the MTJ write current in a 1T1J STT-RAM cell at both switching directions. The memory cell is designed with 45nm PTM (predictive technology model) technology and the simulations are conducted under Cadence Spectre Analog environment. The device variations of both MTJ and NMOS transistors are considered in the simulations. The adopted device parameters are summarized in TABLE I and the simulated NMOS transistor size varies from 180nm to 720nm. TABLE II depicts our simulation results. The mean of the MTJ write current of $0\rightarrow1$ switching is always lower than that of

TABLE II
MTJ Write Current and Standard Deviation Under Process Variation

	$0\rightarrow1$		$1\rightarrow0$	
Transistor	$I_{MTJ}(\mu A)$	Std. Dev.	$I_{MTJ}(\mu A)$	Std. Dev.
180nm	148.28	14.35	186.00	14.02
270nm	194.75	18.11	263.03	15.64
360nm	230.18	20.68	323.27	15.34
450nm	258.18	22.76	362.77	17.15
540nm	280.79	24.51	387.48	19.82
630nm	299.91	26.15	404.43	21.96
720nm	315.41	27.31	416.69	23.49

$1\rightarrow0$ switching at all simulated transistor sizes. However, the standard deviation (Std. Dev.) of the MTJ switching time of $0\rightarrow1$ switching is always larger than that of $1\rightarrow0$ switching.

Following the increase of NMOS transistor size, the ratio between the means of the MTJ write currents at two switching directions, i.e., $I^{0\rightarrow1}_{MTJ,mean}/I^{1\rightarrow0}_{MTJ,mean}$, reduces. It is because that the driving ability of the NMOS transistor is quickly saturated when V_{gs} reduces. However, the ratio between the standard deviations of the MTJ write currents, i.e., $\sigma^{0\rightarrow1}_{I_{MTJ}}/\sigma^{1\rightarrow0}_{I_{MTJ}}$, slightly increases when the NMOS transistor size grows. These two trends indicate that the aggravation of the asymmetry of STT-RAM cell switching when the NMOS transistor size increases.

C. Writing Error Analysis

The write error of STT-RAM happens when the write pulse is removed before the actually needed MTJ switching time is reached. Although the current supplied by the NMOS transistor is affected by device variations, it becomes fixed after the chip is fabricated. However, as aforementioned in Section III-A, the MTJ switching is probabilistic process under thermal fluctuations. In other words, the STT-RAM write error rate P_{WF} is the probability that the MTJ switching time t is longer than the write pulse width T_W, or:

$$P_{WF} = \alpha\beta P(\tau_{th0} > T_W) + (1-\alpha)(1-\beta)P(\tau_{th1} > T_W) \quad (5)$$

Here, α is the probability of a cell storing '1', β is the probability that a cell will be written to '0'. $\alpha\beta$ and $(1-\alpha)(1-\beta)$ denotes the occurrence probabilities of switching $1\rightarrow0$ and $0\rightarrow1$, respectively. $\tau_t h0$ and $\tau_t h1$ are the MTJ switching time threshold of the switching of $1\rightarrow0$ and $0\rightarrow1$, respectively. We note that only the changes of memory cell content can cause the write errors.

Fig. 3 shows the MTJ switching time distributions at the transistor width W of 720nm. Both device variations and thermal fluctuations are considered in the simulations. The MTJ switching time at two STT-RAM switching directions are very asymmetric. If we assume the same write pulse width is applied to both switching directions, the write error rate of $0\rightarrow1$ switching will be significantly larger than that of $0\rightarrow1$ switching. $0\rightarrow1$ becomes the limiting factor on the write reliability of STT-RAM.

IV. Design Space Exploration

Device variations and thermal fluctuations on the write performance and reliability have been neglected in many researches on STT-RAM [3], [7], [11]. The designs based on the nominal device parameters certainly lead to an over-optimistic results. Other studies analyzed the thermal induced noise without giving detailed discussions on the impacts of NMOS transistor variations and the asymmetry of statistical MTJ switching [2], [5]. In this section, we compare the outcomes of different design methodologies and exploit the approach to minimize the design pessimism for the robustness of STT-RAM write operations.

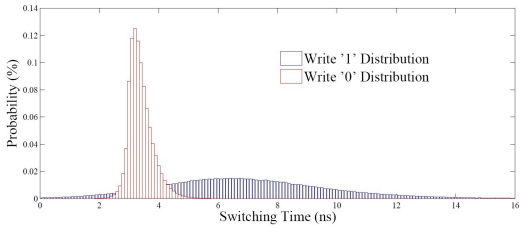


Fig. 3. MTJ switching time distributions at the transistor width W of 720nm.

A. Process variation aware only corner design

A corner design methodology is usually used to overcome the impacts of device variations. The design corner can be setup as the combinations of device parameters. In our simulations, the design corner can be setup as the follows:

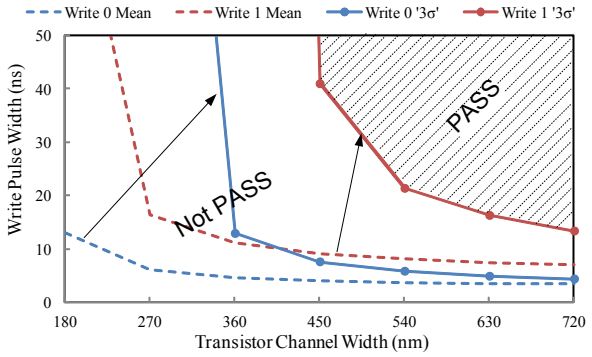
Based on the impacts of the major sources of device variations, the worst corner happens when L, V_{th} and τ show positive deviations from their nominal values and W shows a negative deviation from its nominal value. However, the worst corner of A is difficult to determined: a large MTJ surface raises the magnitude of MTJ switching threshold current while causes the reduction of MTJ resistance, which can improve the NMOS transistor driving ability, and vice versa. Two sub-worst corners need to be created for both the positive and the negative deviations of A. TABLE III lists the parameter deviations accepted in the 3σ worst corner of both NMOS transistor and MTJ devices.

TABLE III
3σ Worst Case Parameters

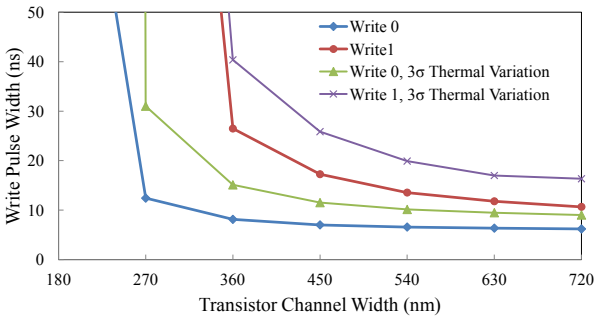
W	L	V_{th}	τ	A
-15%	+15%	+15%	+6%	$\pm15\%$

The simulated relationship between the NMOS transistor size and the required write pulse width are shown in Fig. 4(a). Here we only consider the device variations and neglect the thermal fluctuations. The required write pulse width value is calculated from the nominal relationship curve between the MTJ write current and the switching time (see Fig. 2(a)) while the MTJ write current is calculated based on the 3σ device parameter corner. The solid blue and red lines denote the results of $1\rightarrow0$ switching and $0\rightarrow1$ switching, respectively. The worst result is obtained when the MTJ surface area A is 15% less than the nominal value. Simulation shows that $0\rightarrow1$ switching is the limiting switching direction, which requires larger transistor size and/or longer write pulse width. The pass region is constrained by the solid red line. We denote this design method as "Corner-P-I". For comparison purpose, we also plot the nominal design results that do not consider any device variations or thermal fluctuations, as shown by the dash blue and red lines. A larger pass region is observed though it is an optimistic result.

There is another way to create design corner, i.e., directly using the 3σ value of the MTJ write current distribution to compute the required write pulse width. This method equals to characterize the MTJ write current corner by the conventional statistical CMOS circuit design method and then derive the MTJ switching time by using the nominal MTJ switching curve. We denote this design method as "Corner-P-II". The corresponding results are shown in Fig. 4(b). The pass



(a) Design space based on device parameters corner (Corner-P-I)



(b) Design space based on driving current corner (Corner-P-II)

Fig. 4. Design space obtained by different design methodologies under various transistor sizes.

region is relaxed from the "Corner-P-I" result by accurately estimating the 3σ corner value of the MTJ write current. However, this result may become optimistic as the thermal fluctuation is ignored.

B. Process variation and thermal fluctuation aware corner design

As aforementioned, thermal fluctuations cause the variation of MTJ switching time even the MTJ write current is fixed. If thermal fluctuations are considered in STT-RAM design, a corner representing MTJ switching time variation must be also created in the corner design. For example, the distribution of MTJ switching time under certain MTJ write current can be obtained by macromagnetic model. Then the required MTJ write pulse width can be selected as the one corresponding to the $+3\sigma$ deviation of the MTJ switching time from its nominal value. The simulations results of the requirement write pulse width at different transistor size is also shown in Fig. 4(b). Compared to the result of "Corner-P-II", additional pessimism is added into the pass region because of the consideration on thermal fluctuations. Here we use the same current corner of "Corner-P-II". We refer this corner design as "Corner-PT-II".

C. Process variation and thermal fluctuation aware statistical design

It is well known that the combination of the worst corners of all device parameters may derive very pessimistic design since the worst cases seldom happen simultaneously. To reduce the design pessimism introduced by the conventional corner

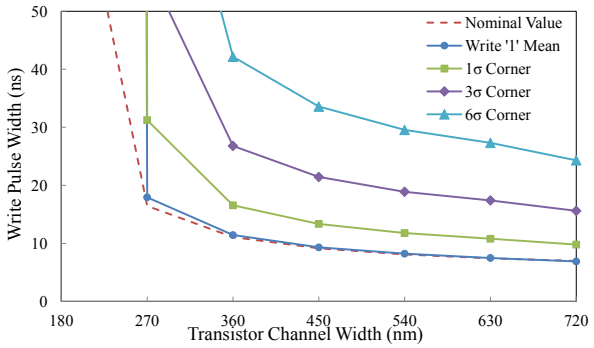


Fig. 5. Required write pulse width at various σ in statistical design.

designs, we established our macromagnetic-spice design platform to simulate the statistical property of STT-RAM cell operations. Monte-Carlo simulations are run on both macromagnetic MTJ model and spice transistor model to obtain the overall MTJ switching time distributions when both device variations and thermal fluctuations are considered.

Fig. 5 shows the pass regions of the STT-RAM cell at different σ's of MTJ switching time. The pass region of the STT-RAM cell at $+3\sigma$ corner of MTJ switching time is between the results of "Corner-P-II" and "Corner-PT-I" designs, indicating the optimism of "Corner-P-II" and the pessimism of "Corner-PT-I". In any cases, $0 \rightarrow 1$ switching continues to be the limiting direction. It actually means that we should avoid the $0 \rightarrow 1$ switching in the operation of STT-RAM, as pointed out by many other studies [5].

We also fit the boundary of pass regions at different σ's of MTJ switching time over the concerned transistor sizes as below:

$$T_W = \frac{1537N + 3240}{W} + 0.765N + 3.301 \qquad (6)$$

Here 1537, 3240, 0.765 and 2.301 are the fitted parameters, which relies on the particular fabrication process. T_W is the required MTJ write pulse width in nanosecond. N is the number of sigma in STT-RAM designs. W is the transistor width in nanometer. This equation can help designers to quickly estimate the pass regions of STT-RAM cell without running the exhausting Monte-Carlo simulations.

V. Bottom-to-Up STT-RAM Structure

TABLE II and Fig. 2 actually mean that in conventional 1T1J STT-RAM cell structure, the NMOS transistor driving direction with a lower nominal current and a larger variation is used to drive the MTJ switching direction that requiring a larger switching current. Therefore, it will be worthy to study the opposite 1T1J STT-RAM cell structure where the reference layer is connected to bit-line, as shown in Fig. 6(b). We call it "Bottom-to-Up" STT-RAM structure [12]. The conventional 1T1J structure is shown in Fig. 6(a).

TABLE IV shows the simulation results of the transistor driving ability in the 'Bottom-to-Up' STT-RAM cell structure. We assume the MTJ property keeps the same after we flip the MTJ fabrication sequence. As expected, the MTJ write

TABLE IV
BOTTOM-TO-UP MTJ STRUCTURE WRITE CURRENT

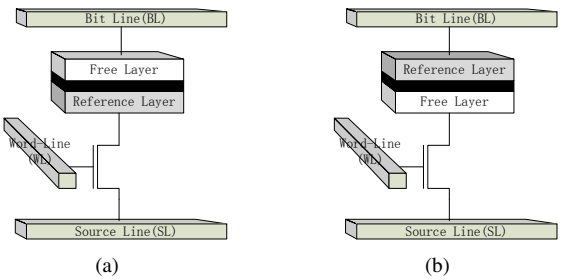
	0→1		1→0	
Transistor	$I_{MTJ}(\mu A)$	Std. Dev.	$I_{MTJ}(\mu A)$	Std. Dev.
180nm	198.80	17.85	113.85	10.64
270nm	291.71	23.40	139.55	12.61
360nm	378.17	26.82	157.04	13.80
450nm	458.27	28.85	169.79	14.69
540nm	531.24	29.70	179.53	15.40
630nm	596.38	29.80	187.52	16.09
720nm	650.16	29.97	193.68	16.49

current at $0 \rightarrow 1$ switching is substantially increased due to the reduced voltage drop across the MTJ and the improved V_{ds}. However, the MTJ write current at $1 \rightarrow 0$ switching reduces sharply down to below 200μA due to the increased MTJ resistance and voltage drop across the MTJ. The low MTJ write current leads to a very long MTJ switching time even the standard deviation of the write current is reduced.

'Bottom-to-up' structure introduced a more asymmetric operations of STT-RAM cell with our simulated technology node and device parameters, as shown in Fig. 7. The simulations are based on our statistical design flow where both process variations and thermal fluctuations are considered. Compared the results in Fig. 5 to Fig. 7, the pass region of STT-RAM design in conventional cell structure is much relaxed than 'Bottom-to-Up' structure. It indicates a more robust STT-RAM cell design.

VI. CONCLUSION

In this work, we quantitatively analyzed the statistical property of STT-RAM cell switching by considering both process variations and thermal fluctuations. Our analysis revealed the asymmetry of the STT-RAM write operations, which causes the significantly unbalanced write reliability at the switchings of 1→0 and 0→1. We then studied the effectiveness of different design methodologies to capture the pass region of STT-RAM cell designs, including nominal design, corner designs (with only device variations and with both device variations and thermal fluctuations) and full statistical design. Our results show that the conventional corner design with only device parameter corner failed to give a trustable pass region while the enhanced corner design with both device and thermal corners results in a over-pessimistic result. Our simulations proved the importance of a full statistical design method for STT-RAM



(a) (b)

Fig. 6. (a) Conventional 1TJ Structure (b) Bottom-to-Up 1T1J Structure.

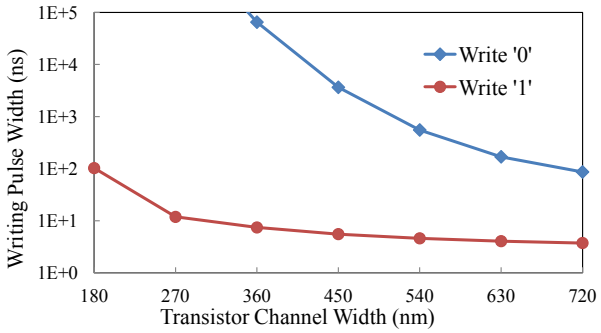


Fig. 7. Design space in 'Bottom-to-Up' structure.

designs. Finally, the simulation on the "Bottom-to-Up" STT-RAM cell design shows that reverting the connection of MTJ does not help to mitigate the asymmetry of STT-RAM write operation: the required write pulse width of 1→0 switching is significantly prolonged due to the heavily degraded NMOS transistor driving ability.

ACKNOWLEDGMENT

This work is supported by NSF award CNS-1116171.

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