# Challenges and Emerging Solutions in Testing TSV-Based $2\frac{1}{2}$D- and 3D-Stacked ICs

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**Abstract**

Through-Silicon Vias (TSVs) provide high-density, low-latency, and low-power vertical interconnects through a thinned-down wafer substrate, thereby enabling the creation of 2.5D- and 3D-Stacked ICs. In 2.5D-SICs, multiple dies are stacked side-by-side on top of a passive silicon interposer base containing TSVs. 3D-SICs are towers of vertically stacked active dies, in which the vertical inter-die interconnects contain TSVs. Both 2.5D- and 3D-SICs are fraught with test challenges, for which solutions are only emerging. In this paper, we classify the test challenges as (1) test flows, (2) test contents, and (3) test access.

## 1 Introduction

Advances in semiconductor process technologies enable the manufacturing of wafers containing Through-Silicon Vias (TSVs) [1–3]. TSVs allow to architect single-package multi-chip products using vertical interconnects with unprecedented density, performance, and low power dissipation, thereby enabling the creation of a new generation of 'super chips' [4, 5]. Despite its many technical challenges still, three-dimensional stacking of dies interconnected by TSVs is seen by many as a key technology to help the semiconductor industry to extend the momentum of Moore's Law into the next decade.

Due to its many high-precision steps, semiconductor manufacturing is defect-prone. Consequently, every IC needs to undergo electrical tests to weed out the defective parts and guarantee outgoing product quality to the customer. This is also true for the new TSV-based three-dimensional die stacks. Typically containing complex die designs in advanced technology nodes, these die stacks employ most of today's advanced test and design-for-test approaches. In addition, three-dimensional die stacks have some unique test challenges of their own. The main challenges can be classified as pertaining to (1) test flows, (2) test contents, and (3) test access. This paper provides an overview of these test challenges and their emerging solutions.

The remainder of this paper is organized as follows. Section 2 gives an outline of key technology aspects of $2\frac{1}{2}$D- and 3D-SICs. Section 3 presents 3D test flows. Section 4 discusses new 3D test contents. Challenges and solutions for external (probe) and internal (design-for-test) test access are described in Section 5. Section 6 concludes this paper.

## 2 TSV-Based $2\frac{1}{2}$D- and 3D-SICs

TSVs are conducting nails which stick out of the back-side of a thinned-down die, which allow that die to be vertically interconnected to another die. TSVs are high-density, low-capacitance interconnects compared to traditional wire-bonds, and hence allow for much more interconnects between stacked dies, and these interconnects can operate at higher speeds and lower power dissipation.

TSVs come in many different flavors. TSVs are typically made of copper or tungsten, each with different material properties. We distinguish between 'via-first', 'via-middle', and 'via-last' TSVs, referring to their moment of creation in the processing flow, relative to FEOL and BEOL processing.

Key parameters of TSVs are their shape, height, diameter, and pitch. TSVs are required to have a certain minimum height; the thinner a wafer, the more difficult the handling of that wafer in subsequent processing steps, and also the bigger the detrimental impact on transistor performance. TSVs should not have too much volume, in order to keep their switching capacitance low; for a given TSV height, this requirement translates into a maximum TSV diameter. The aspect ratio of TSV height and diameter determines the difficulty of, time required for, and costs associated with TSV processing. Typical TSVs at IMEC are 'via-middle' cylindrical Cu nails with aspect ratio 1:10, for example at 5$\mu$m diameter and 50$\mu$m height at a 10$\mu$m minimum pitch (see Figure 1).

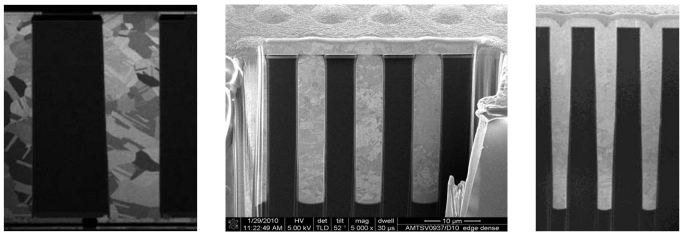

**Figure 1:** Various TSV examples processed at IMEC.

There exist multiple ways to make the actual bond between two vertically stacked dies. Commonly used is an intermetallic bond based on Cu and CuSn micro-bumps. In IMEC's reference process, these micro-bumps are 25$\mu$m in diameter at 40$\mu$m pitch (see Figures 2(a) and 2(b)). While small for industrial norms, this pitch is the bottleneck in overall interconnect density, and hence re-

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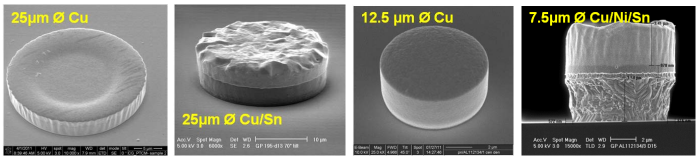
search efforts are directed at enabling micro-bumps at finer pitches (see Figures 2(c) and 2(d)).



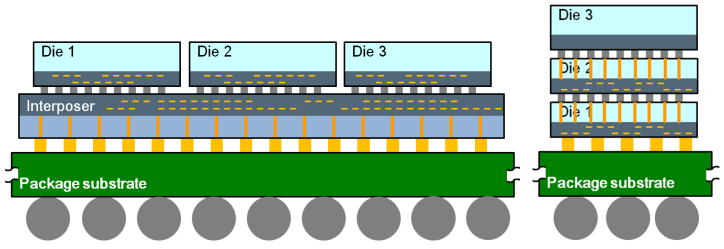

(a) (b) (c) (d)

**Figure 2:** Examples of micro-bump scaling at IMEC.

With these new technologies, vertical stacking options become virtually unlimited. Stacked dies can be manufactured in either homogeneous or heterogeneous technologies. Dies can be stacked face-up or face-down, face-to-face or face-to-back, connected by only wire-bonds, TSVs, or a combination of the two. We can build stacks of only two dies or more than two dies, consisting of a single or multiple towers [6]. At this moment in time, two configurations commonly emerge as industrial products; they are referred to as $2\frac{1}{2}$D-SICs and 3D-SICs.

In *$2\frac{1}{2}$D-SICs*, multiple active dies are placed side-by-side on top of and interconnected through a passive silicon interposer base which contains TSVs [7–10]. $2\frac{1}{2}$D-SICs are attractive for high-performance compute and communication applications, as they offer good cooling opportunities. Figure 3(a) depicts a typical $2\frac{1}{2}$D-SIC, in which three active dies are stacked face-down on top of an interposer base, connected through fine-pitch micro-bumps. The passive interposer provides both horizontal interconnects between the various dies through its multiple metal layers, as well as vertical interconnects to external I/Os through its TSVs. In a $2\frac{1}{2}$D-SIC as depicted, the stacked active dies do not require TSVs.

In *3D-SICs*, multiple active dies are stacked on top of each other. Consequently, 3D-SICs offer a small footprint, which is particularly attractive for hand-held and portable consumer electronics. Figure 3(b) depicts a typical 3D-SIC, in which three active dies are stacked face-down on top of each other, connected through TSVs and fine-pitch micro-bumps.




(a) (b)

**Figure 3:** Two common stack configurations: (a) $2\frac{1}{2}$D-SIC and (b) 3D-SIC.

In the foreseeable future, we can expect also hybrid combinations of the above, i.e., multiple towers of active dies stack on top of and interconnected through a passive silicon interposer base. In this paper, we coin the term *$5\frac{1}{2}$D-SICs* for such stack configurations.

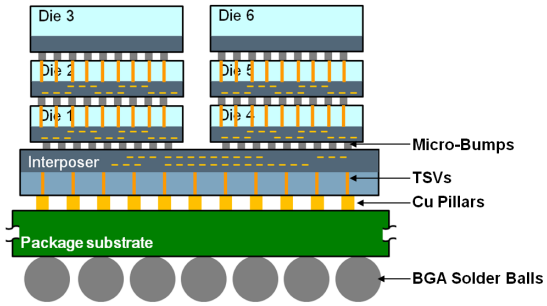



**Figure 4:** $5\frac{1}{2}$D-SIC: multiple towers of active dies on a passive interposer.

## 3 3D Test Flows

Most conventional single-die chips have a test flow consisting of two test moments: a *wafer test* and a final *packaged test*. The test flows for $2\frac{1}{2}$D- and 3D-SICs are potentially a lot more complex; their manufacturing process consists of many more steps and hence has many more potential natural test moments. Figure 5 illustrates these test moments for a three-die stack. We refer to tests before stacking as *pre-bond tests*; they can be performed either before and/or after wafer thinning. After stacking, tests can be performed on either partial stacks (called *mid-bond tests*) and/or complete stacks (called *post-bond tests*). For all these tests, external test access is achieved through probing, typically at wafer level. Once the stack is packaged, a final *packaged test* can be performed. External test access for the final test is typically via a test socket through the package pins.

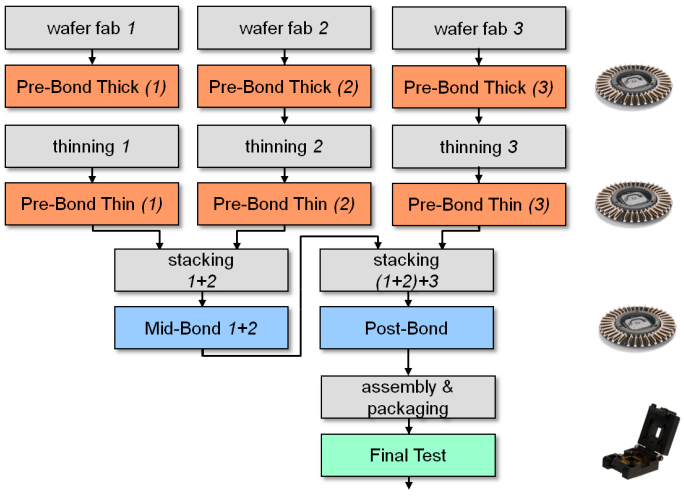



**Figure 5:** Potential test moments for a three-die stack.

The various test moments each come with their own technical challenges and constraints. Next to the technical (in)feasibility of executing certain tests at certain test moments, it is typically the business contract between supplier and customer that dictates the required testing.

In an *integrated* production flow, manufacturing of the dies/wafers, stacking, and packaging are all under control of a single company. In such a set-up, the outgoing product quality is typically deter-

mined by a comprehensive final test, while any preceding tests merely contain a subset of that final test, in order to weed out faulty parts early on and prevent higher costs downstream. This scenario allows to use the quality and costs of the intermediate pre-, mid-, and post-bond tests as optimization parameters to minimize the overall production costs [11–13]. For example, it might be well worthwhile to perform a 95% coverage test at pre-bond, instead of a significantly more expensive 99.5% coverage test.

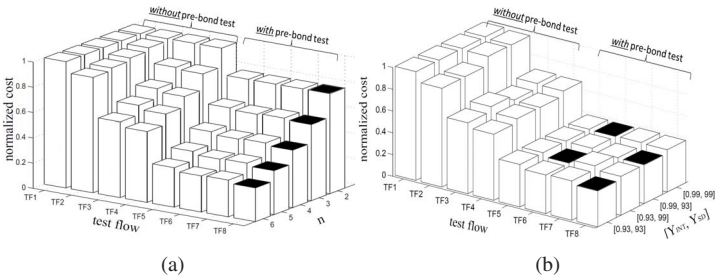
In a *disintegrated* production flow, the overall manufacturing chain is controlled by multiple companies. For $2\frac{1}{2}$D- and 3D-SICs, a disintegrated production flow is much more likely than it was for conventional (2D) ICs, especially for heterogeneous die stacks. In a disintegrated production flow, intermediate products which are building blocks for one company, are final products for another company. For example, DRAM dies to be stacked on top of logic dies are intermediate products in view of the overall stack, but are final products for the DRAM maker. In such a setting, the supply contract typically requires that the intermediate products (DRAMs, in our example) are tested with final-test quality, including at-speed and burn-in tests. Such intermediate products are termed *Known-Good Dies* (KGD) [14], or, in case of die stacks, *Known-Good Stacks* (KGS) [11, 12].

A *pre-bond test* should primarily focus on defects in the die-internal (CMOS, DRAM, etc.) circuitry, and only optionally be extended for TSV defects. If performed on an original (still thick) wafer, the pre-bond test has the benefit of conventional wafer handling, but has as drawback that wafer-thinning defects, if any, are not covered. Moreover, testing for TSV defects on not-yet-thinned wafers is cumbersome, as one side of the TSV is still buried in thick substrate; hence there is only single-sided test access and this requires dedicated DfT and test methods [15–17]. On the other hand, pre-bond testing on thinned-down wafers, which allows to cover defects induced by wafer thinning and actually test through TSVs, requires probe access on thinned wafers, which brings about a whole new set of challenges as outlined in Section 5.1.

*Mid-* and *post-bond tests* should primarily focus on testing the newly formed TSV-based interconnects. Assuming the die-internal circuitry was already tested during pre-bond testing, mid- and post-bond tests should only re-test that circuitry if stacking operations are likely to damage it [13]. The *final test* is the last safety net before the packaged die stack is shipped to the customer. Hence, the test infrastructure should be such that all components and interconnects of the die stack can be (re-)tested if required.

Testing should provide sufficient product quality at affordable costs for the application market addressed. Consequently, there is no single *one-size-fits-all* test flow. When setting up a test flow, a general guiding principle is that it is typically best to catch defects as early as possible, in order to prevent faulty components to move forward in the production flow and get permanently afixed to other, fault-free components. However, early tests have the drawback that passing components might get damaged afterwards due to downstream (thinning, stacking, packaging) operations and hence require re-testing. The manufacturing costs and yields are in complex ways intertwined with test flows and associated costs, and hence test cost modeling is required to determine the best test flow for a given product.

In [13], Taouil et al. present a cost model for Die-to-Die (D2D) and Die-to-Wafer (D2W) stacking, taking into account manufacturing, test, and packaging costs and yields as input parameters. The model is geared toward comparing various test flows that in- or exclude pre-bond, mid-bond, and post-bond testing. The model is based on two key assumptions. The first one is that a final packaged test catches all previously undetected faults, such that all test flows compared differ only in test and product costs, but not in outgoing product quality. The second assumption is that die stacking happens in a linear order and that each stacking operation will at most introduce new defects in the two dies and interconnects directly involved in the stacking operation. The cost model produces product cost comparisons of test flows, as depicted in Figure 6. All product costs are normalized to the cost of Test Flow 1. The bar with the black top indicates the test flow with the lowest overall product cost for a particular case. For all cases shown in Figure 6, test flows TF1–4 (which exclude pre-bond testing) have a significantly higher product cost than their counterpart test flows TF5–8 (which include pre-bond testing), clearly demonstrating that an investment in higher test cost might pay off in lower overall product cost.




(a) (b)

**Figure 6:** Cost comparison of eight test flows (normalized to TF1) for varying (a) number of stack tiers and (b) stacking interconnect and die yield [13].

Compared to D2W and D2D stacking, Wafer-to-Wafer (W2W) stacking offers the highest manufacturing throughput and allows for the smallest die sizes, thinnest wafers, and highest TSV densities [18, 19]. The drawback of W2W stacking is that one cannot avoid that a bad die is stacked onto a good die or vice versa, leading to low compound yields. This drawback is exacerbated by a large number of stack tiers, a small number of (large) dies per wafer, and/or low die yield. Research [19–22] has demonstrated that *wafer matching* on the basis of pre-tested wafer repositories can increase the (low) compound yield significantly, such that the costs of the pre-bond test are more than recuperated.

Test flows are not static in time. Manufacturing yields (hopefully) gradually increase once production starts maturing, and this has its impact on the optimal test flow. For this reason, a *modular* test approach [23] is favored. In a modular test approach the various components and interconnects can be tested as stand-alone units (as opposed to a *monolithic* test, in which the die stack is tested as a single, monolithic entity). A modular test approach allows to include, exclude, and re-schedule the various module tests [23, 24].

Additional benefits of a modular test approach are the dedicated focused test pattern generation, possibly with design IP protection [23], lower overall test data volume and application time [25], and first-order diagnosis capability [11].

# 4 3D Test Contents

For TSV-based die stacks, the vast majority of conventional wafer processing steps remain unchanged, and hence the same holds for their defects, fault models, and tests. New test content might be expected (1) due to new 3D processing steps, and (2) for the TSV-based interconnects, which form an entirely new structure.

## 4.1 New 3D Processing Steps

3D processing steps such as TSV manufacturing, back-side processing, and wafer thinning have an impact on the conventional (CMOS, DRAM, etc.) circuitry. For example, aggressive wafer thinning has been shown to cause degradation of *I-V* characteristics of transistors [26, 27]. Thermal dissipation and thermo-mechanical stress [28, 29] are other causes of concern.

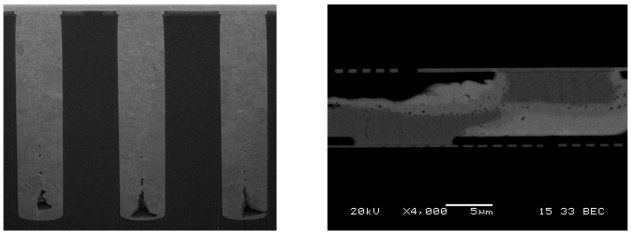
An important question is whether these effects induce new intra-die defects, of which the corresponding fault behavior is not covered by conventional tests. Until now, all phenomena observed are structural and predictable in nature, implying that they should be counteracted by design and design rules [28], instead of being filtered out by testing. Moreover, even though the defect root cause might be different, the resulting fault behavior is already covered by conventional existing test sets.

In conclusion, while it is important to stay alert for defects that are not covered by conventional test sets, there is currently no need for immediate action.

## 4.2 Test of TSV-Based Interconnects

TSV-related defects might occur either in the fabrication of the TSV themselves or in the (micro-bump) bonding of the TSVs to the next tier. During the fabrication of TSVs, (micro-)voids, for example due to quasi-conformal plating, might lead to (weak) opens in TSVs (see Figure 7(a)). Pinholes in the TSV oxide might lead to shorts between TSV and substrate. Ineffective removal of the seed layer might lead to shorts between TSVs. The bond quality might be negatively impacted by oxidation or contamination of the bond surface, height variation of the TSVs, or particles in between the two dies. Mis-alignment during bonding, in either $x$, $y$, and/or (tilted) $z$ direction, might lead to opens or shorts (see Figure 7(b)). In case of CuSn micro-bumps, the tin might squeeze out due to TSV height variation and cause shorts in between them.

Once the interconnects are formed, they serve as virtual 'wires' between two tiers. Interconnect testing requires a dedicated interconnect test pattern generator, to cover for specific driver-receiver transition tests [30] as well as layout-independent shorts [31]. These algorithms detect all (hard) open and shorts through a set of digital test patterns that can be kept small, as it grows only logarithmically with the number of interconnects. This is an attractive feature, as the number of TSV-based interconnects is potentially very large. The test algorithms rely on the presence of full controllability respectively observability at all interconnect inputs respectively outputs; this requirement is fulfilled by the DfT architecture described in Section 5.2.




(a) (b)

**Figure 7:** Examples of interconnect defects: (a) TSVs containing micro-voids, and (b) a short caused by mis-aligned micro-bumps.

Open challenges with respect to testing TSV-based interconnects are the detection of weak defects and timing faults, defects in 'infrastructure' TSVs (power, ground, clocks), and the implementation of effective and efficient redundancy and repair strategies [32].

# 5 3D Test Access

Test access deals with delivery of test stimuli and responses from the test equipment to the appropriate circuit-under-test (CUT) and vice versa. In this section, we subsequently discuss (1) the external test access from the test equipment to the chip I/Os and back through wafer probing and (2) the internal test access from the chip I/Os into the CUT and back through on-chip design-for-test (DfT).

## 5.1 External Test Access: Probe Access

In *pre-bond* testing we need to probe the dies before stacking. For the die holding the external I/Os (this is typically the bottom die), we can probe on wire-bond or flip-chip pads; this is 'business-as-usual'. However, the other (non-bottom) dies receive all their functional signals (for power, ground, clocks, control, data) through micro-bumps. Micro-bumps are typically too small ($\leq$25$\mu$m diameter), too dense ($\leq$40$\mu$m pitch), too numerous, and too fragile to be probed with conventional probe technology [33]. Cantilever probes go down to 20$\mu$m pitch, but do not support arbitrary array configurations. The minimum pitch of conventional vertical probes is 50$\mu$m, insufficient for fine-pitch micro-bumps. Conventional probe technology also makes significant probe marks that might inhibit downstream bonding on the same surface.

The probe industry is working to make a significant improvement in scaling down the probe pitch and reducing the probe mark dam-

age. This requires a collaborative effort of probe card makers [34–36] and probe station makers alike [37], as it is the sum of the accuracy tolerances that define the overall system accuracy (see Figure 8). Efforts are also spent on contact-less testing [38–40], which by definition does not cause any probe damage, but currently still lacks in pitch and density.

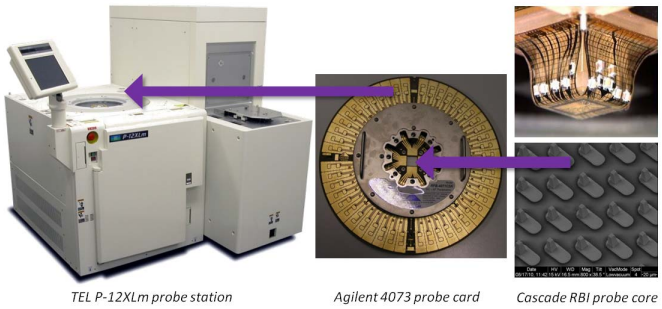



**Figure 8:** Experimental set-up at IMEC for fine-pitch micro-bump probing (photos courtesy of resp. TEL Test Systems and Cascade Microtech).

Until a robust probe technology is available for fine-pitch micro-bumps, the only solution to enable pre-bond testing is to equip non-bottom dies with additional probe pads, sized such that today's probe technology can handle them. Papers on various industrial 3D chips have indeed confirmed this practice [41, 42]. This comes with an area penalty, and hence the number of extra probe pads should be minimized; on-chip DfT such as Reduced Pin-Count Testing (RPCT) [43] and Test Data Compression [44] can help with this.

Additional probe challenges are in handling of and probing on thinned-down wafers, and the non-planar topology of post-bond D2W stacks. The latter causes probe challenges no matter what side we probe on. If probe access is on the bottom side of the wafer, the stacks create a very non-planar surface, which is difficult to keep stable on the chuck. If probe access is on the top side of the wafer, we need to manoeuvre carefully with long-enough probe needles in between the die stacks, while the stacks might obstruct the probe station's contact-view camera [12].

## 5.2 Internal Test Access: Design-for-Test

In [45–47] a DfT architecture for 3D die stacks was proposed, evolving around a die wrapper that can be based on either IEEE Std 1500 or IEEE Std 1149.1 (see Figure 9). The architecture supports a modular test approach with a serial (one-bit) and scalable parallel ($n$-bit) test access mechanism (TAM) that transports test stimuli from the external I/Os (typically at the base die) through the stack to the CUT and test responses vice versa. Each die of the stack can be individually instructed to go in either an INTEST (die-internal test), EXTEST (interconnect test), or BYPASS mode, and either connect to the TAM of the next-higher die or turn downward. The 3D DfT architecture is supported by various commercially available EDA tools [48, 49]. Also, it is under consideration for standardization [50], which especially makes sense in the case the stacked dies come from different suppliers.

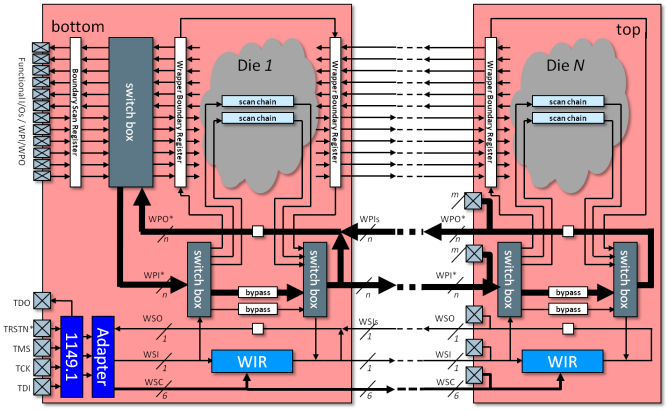



**Figure 9:** Basic 3D DfT architecture based on die-level wrappers.

The basic architecture can easily be extended to include support for multiple (sub-)towers [6, 47] and stacking boundary scan-equipped DRAMS (e.g., JEDEC Wide-IO DRAMs [41, 51]).

Chi et al. [9, 10] proposed a DfT architecture for $2\frac{1}{2}$D- and $5\frac{1}{2}$D-SICs containing a passive silicon interposer base; Figure 10 shows this architecture for an example $2\frac{1}{2}$D-SIC. It utilizes the 3D DfT wrapper described above for all active dies. The multiple active bottom dies are also equipped with IEEE Std 1149.1 DfT. The external I/O interface of the passive interposer base ('Port 0') is extended with a four- or five-pin IEEE 1149.1 Test Access Port (TAP) which is connected in a conventional way to the IEEE 1149.1 TAPs of the active bottom dies. A serial TAM is formed by daisychaining Test Data In (TDI) from Port 0, via the various active bottom dies, back to Test Data Out (TDO) at Port 0. This serial TAM is able to perform interconnect testing of micro-bumps and interposer connections. It also provides a basic low-bandwidth TAM for testing the (towers of) active dies. In [9, 10] algorithms are described that identify existing functional interposer interconnects that be be reused as parallel TAM; this is a way to increase the test access bandwidth and hence reduce the overall test length for the active dies at virtually zero cost.

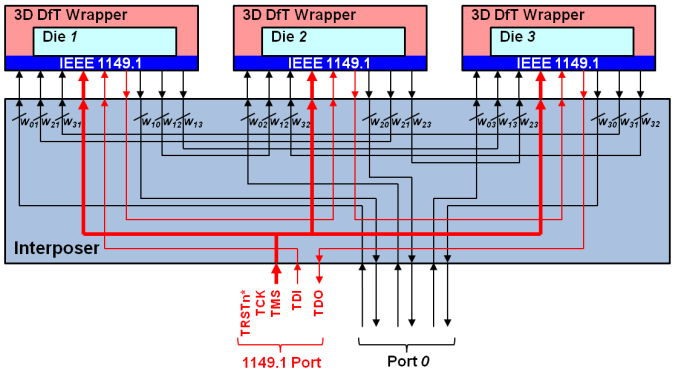



**Figure 10:** DfT architecture for $2\frac{1}{2}$D-SICs.

# 6 Conclusion

$2\frac{1}{2}$D-, 3D-, and $5\frac{1}{2}$D-SICs are fraught with test challenges. The main test challenges can be classified as (1) test flows, (2) test

contents, or (3) test access. Solutions to these challenges are only emerging. Research work is done on cost modeling to determine effective and cost-efficient test flows. The probe industry is working to enable fine-pitch micro-bump probing. A DfT architecture for $2\frac{1}{2}$D- and 3D-SICs has been defined and EDA tools have been developed to automatically insert 3D DfT and generate dedicated interconnect test patterns. Despite the many still open challenges, we are hopeful that test technology will not be in the way for bringing TSV-based die stacks into volume production.

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