Mitigating Lifetime Underestimation: A System-Level Approach Considering Temperature Variations and Correlations between Failure Mechanisms

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***Abstract*—Lifetime (long-term) reliability has been a main design challenge as technology scaling continues. Time-dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI), and electromigration (EM) are some of the critical failure mechanisms affecting lifetime reliability. Due to the correlation between different failure mechanisms and their significant dependence on the operating temperature, existing models assuming constant failure rate and additive impact of failure mechanisms will underestimate the lifetime of a system, usually measured by mean-time-to-failure (MTTF). In this paper, we propose a new methodology which evaluates system lifetime in MTTF and relies on Monte-Carlo simulation for verifying results. Temperature variations and the correlation between failure mechanisms are considered so as to mitigate lifetime underestimation. The proposed methodology, when applied on an Alpha 21264 processor, provides less pessimistic lifetime evaluation than the existing models based on sum of failure rate. Our experimental results also indicate that, by considering the correlation of TDDB and NBTI, the lifetime of a system is likely not dominated by TDDB or NBTI, but by EM or other failure mechanisms.**

I. INTRODUCTION

Usually measured by *mean-time-to-failure* (MTTF), long-term or "lifetime" reliability in the presence of wear-out failures is becoming a main concern for the design of long-lasting systems. Semiconductor devices have undergone dramatic innovations since the recent decade, but at the price of decreasing long-term reliability. As demonstrated in [1], the average MTTF of a contemporary superscalar processor drops by about 4X from 180nm to 65nm technology nodes. It is expected that, in the near future, the design cost and effort required for increasing lifetime reliability will be as high as for classic design constraints, *e.g.*, timing and power consumption.

Time-dependent dielectric breakdown (TDDB), *negative bias temperature instability* (NBTI), and *electromigration* (EM) are some of the critical failure mechanisms affecting lifetime reliability. With the continuous shrinking of transistor and interconnect dimensions, the rate of such progressive wear-out failures is getting higher. In addition, due to the increasing transistor density without proportional downscaling of supply voltage, the power density and thus the operating temperature will rise significantly, which further accelerates the failure mechanisms because they are all exponentially dependent on temperature. The temperature issue is potentially aggravated by higher leakage power, as a result of rising operating temperature, and finally thermal runaway may occur in the worst case. Therefore, the dependence of failure mechanisms on temperature is regarded as an important joint factor in determining the overall MTTF of a system [2].

Many of the existing methods for lifetime evaluation [3][4][5] follow a commonly-used MTTF model – *sum-of-failure-rate* (SOFR). The SOFR model makes two assumptions: (*i*) every failure mechanism has an exponential reliability distribution with a constant failure rate, and (*ii*) the effects of all failure mechanisms (in terms of failure rate) are additive and can be summed up for deriving the combined MTTF, as explained later in Section II.B. However, it has been shown in [6][7] that the models assuming constant failure rate may lead to pessimistic results during the early stage of lifespan and to misleading guidance for a design, despite its tractability and ease of implementation. In [7][8], the SOFR model is revised to accommodate the structural relationship using MIN/MAX approximation, whereas the relationship among various failure mechanisms is assumed to be fully serial and independent, namely, uncorrelated. Since some of the failure mechanisms such as TDDB and NBTI can affect each other due to their mutual dependence on temperature and other operating parameters, modeling the correlation of TDDB and NBTI is also a crucial step for more accurate lifetime estimation.

In this paper, we propose a new methodology which evaluates system lifetime while considering workload-induced temperature variations. For the first time compared to existing work, our proposed methodology can avoid lifetime underestimation by extracting the *correlation* between different failure mechanisms (*i.e.*, TDDB and NBTI) and by distinguishing the *impact* of every individual mechanism. Based on Monte-Carlo simulation and MIN/MAX operations, our methodology can not only calculate the average MTTF value but also find the lifetime distribution. The results are particularly useful in analyzing the long-term reliability of a given system.

The rest of this paper is organized as follows: Section II gives an overview of related background, including target failure mechanisms and the SOFR model. In Section III, we summarize the key points motivating our work and present the overall methodology for lifetime evaluation. Section IV describes our approach to deriving MTTFs associated with

[*] This work was performed while the author was with Carnegie Mellon University.

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various mechanisms. In Section V, the experimental setup and results are demonstrated. Finally, we conclude our work in Section VI.

II. Background

A. Wear-out Failure Mechanisms

This work targets four major wear-out failure mechanisms potentially dominating the MTTF of a system manufactured at 65nm or beyond: *time-dependent dielectric breakdown* (TDDB), *negative bias temperature instability* (NBTI), *electromigration* (EM), and *thermal cycling* (TC).

Time-dependent dielectric breakdown (TDDB) [10][11]: TDDB is the deterioration of the gate dielectric layer, which causes gradual wear-out in MOSFETs due to the formation of a conductive path through the oxide to the substrate. The MTTF for TDDB is shown as follows:

$$MTTF_{\mathrm{TDDB}} \propto \left(\frac{1}{V}\right)^{a-bT} \cdot e^{\frac{X+Y/T+ZT}{\kappa T}} \tag{1}$$

where V is the supply voltage, κ is the Boltzmann constant, T is the temperature in Kelvin, and a, b, X, Y, and Z are fitting parameters.

Negative bias temperature instability (NBTI) [12][13]: NBTI is due to the electrochemical reaction by dissociating *Si-H* bonds and trapping holes along the *Si-SiO*$_2$ interface[†], which leads to increasing $|V_{th}|$ of P-type MOSFETs. The MTTF for NBTI is shown as follows:

$$MTTF_{\mathrm{NBTI}} \propto \left(\frac{1}{V_{gs}}\right)^{\gamma} \cdot e^{\frac{E_{a,\mathrm{NBTI}}}{\kappa \mathrm{T}}} \tag{2}$$

where V_{gs} is the gate-to-source voltage, γ is the voltage acceleration factor, $E_{a,\mathrm{NBTI}}$ is the activation energy for NBTI.

Electromigration (EM) [15][16]: EM is the mass transport of metal atoms in interconnects due to electric current, which causes gradual displacement of metal wires manifesting as open- or short-circuit failures of interconnects. The MTTF for EM is shown as follows:

$$MTTF_{\mathrm{EM}} \propto \left(\frac{1}{J}\right)^{n} \cdot e^{\frac{E_{a,\mathrm{EM}}}{\kappa \mathrm{T}}} \tag{3}$$

where n is an empirical constant, depending on the material, $E_{a,\mathrm{EM}}$ is the activation energy for EM, and J is the current density, which can be further characterized as:

$$J \propto \frac{CV_{dd}}{WH} \cdot \alpha \cdot f \tag{4}$$

where C, W and H are the capacitance, width and height of a metal wire respectively, α is the switching probability, and f is the clock frequency.

Thermal cycling (TC) [17]: TC is due to the fatigue deformation of material layers by runtime thermal variations, which leads to fatigue failures of IC packaging. The MTTF for TC is shown as follows:

$$MTTF_{\mathrm{TC}} \propto \left(\frac{1}{T_{average} - T_{ambient}}\right)^{q} \tag{5}$$

where $T_{average}$ is the average runtime temperature of an on-chip structure, $T_{ambient}$ is the ambient temperature, and q is the Coffin-Manson exponent.

B. Sum-of-Failure-Rate (SOFR) Model

To obtain the overall MTTF of a given system S, one needs to combine the effects of various failure mechanisms across different components in the system. The sum-of-failure-rate (SOFR) model has been widely used to determine the combined MTTF from individual MTTF values. The standard SOFR model is defined as:

$$MTTF(S) = \frac{1}{\lambda(S)} = \frac{1}{\sum_i \sum_j \lambda_j(C_i)} = \frac{1}{\sum_i \sum_j \frac{1}{MTTF_j(C_i)}} \tag{6}$$

where $\lambda_j(C_i)$ stands for the failure rate of the ith component, C_i, due to the jth failure mechanism, which is the reciprocal of its corresponding MTTF value, $MTTF_j(C_i)$, given that $\lambda_j(C_i)$ is a constant.

The effects of failure mechanisms in terms of "failure rate" (*i.e.*, $\lambda_j(C_i)$ in Equation (6)) are additive under the assumptions of constant failure rate and series (competing) failure system [3][4]. Please refer to [3][4] for more details about the SOFR model.

III. Proposed Methodology

A. Motivation

In this subsection, we motivate our work by explicitly pointing out the pitfalls of existing MTTF models. In the original SOFR model [3][4][5], it is assumed that (*i*) a system fails if any of its components fails, (*ii*) a system component fails if any of the wear-out failures occurs, and (*iii*) each of the failure mechanisms has a constant failure rate. Based on these assumptions, the overall MTTF of system S in Figure 1 can be derived by Equation (6):

$$\begin{aligned} MTTF(S) &= \frac{1}{\sum_j \frac{1}{MTTF_j(C_1)} + \sum_j \frac{1}{MTTF_j(C_2)}} \\ &= \frac{1}{\left(\frac{1}{4}+\frac{1}{8}\right)+\left(\frac{1}{8}+\frac{1}{16}\right)} = 1.78 \end{aligned} \tag{7}$$

This model is conspicuously inaccurate (pessimistic) because the structural relationship and the relationship among various failure mechanisms are not taken into account. In the revised SOFR model [7][8], the first assumption (*i*) is relaxed by using MIN/MAX approximation to accommodate the structural relationship. Consider the same example in Figure 1 where the two components are in series. Therefore, the system will fail as long as one of the components fails (whichever is earlier), and the overall

[†] High-$\mathcal{K}$ gate dielectrics also experience crucial reliability challenges due to NBTI (and TDDB) [14].

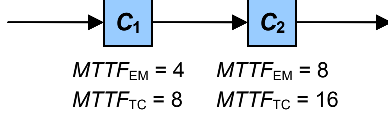

Figure 1. A system S with two components (C_1 and C_2) in series

MTTF of the system can be derived as:

$$MTTF(S) = \text{MIN}\left\{\frac{1}{\sum_j \frac{1}{MTTF_j(C_1)}}, \frac{1}{\sum_j \frac{1}{MTTF_j(C_2)}}\right\} \tag{8}$$

$$= \text{MIN}\left\{\frac{1}{\frac{1}{4}+\frac{1}{8}}, \frac{1}{\frac{1}{8}+\frac{1}{16}}\right\} = 2.67$$

However, the relationship among various failure mechanisms is assumed to be fully serial and is not generally addressed in this revised model. Also, the assumption of constant failure rate is not realistic for several wear-out failure mechanisms. In the sequel, we present a new methodology with all of the aforementioned shortcomings addressed.

B. Impact of Independent Failure Mechanisms

The key fact ignored by existing MTTF models is that different failure mechanisms impact on different components of a system; for example, TDDB and NBTI affect transistors, while EM affects interconnects and TC impacts on the packaging. In other words, the effects of failure mechanisms impacting on different components are independent from the spatial perspective and thus should not be additive, even though the "magnitude" itself of every single MTTF is positively correlated with each other due to the joint dependence on temperature and other technology-dependent parameters. Instead, the combined MTTF of a system component C_i, denoted by $MTTF(C_i)$, should be determined by the minimum MTTF across various failure mechanisms and is formulated as:

$$MTTF(C_i) = \underset{j}{\text{MIN}}\{MTTF_j(C_i)\} \tag{9}$$

where $MTTF_j(\cdot)$ is the independent MTTF result due to an individual failure mechanism (*e.g.*, EM or TC) or the joint effect of multiple failure mechanisms (*e.g.*, TDDB **and** NBTI).

From Equation (9), the overall MTTF of system S in Figure 1 is:

$$MTTF(S) = \text{MIN}\{MTTF(C_1), MTTF(C_2)\}$$

$$= \text{MIN}\left\{\underset{j}{\text{MIN}}\{MTTF_j(C_1)\}, \underset{j}{\text{MIN}}\{MTTF_j(C_2)\}\right\} \tag{10}$$

$$= \text{MIN}\left\{\text{MIN}\{4,8\}, \text{MIN}\{8,16\}\right\} = 4$$

Note that the lifetime underestimation incurred by previous MTTF models (Equations (7) and (8)) is avoided. The proposed model based on MIN operations relaxes the second assumption (*ii*) above. To relax the third assumption (*iii*) – constant failure rate due to the exponential distribution of lifetime reliability, we model the lifetime distribution of a target failure mechanism as a lognormal distribution whose mean value is simply the corresponding MTTF. Lognormal distributions have been found to be more appropriate for modeling many wear-out failure processes due to their capability of formulating time-dependent degradation rates, while exponential distributions are characterized by constant failure rates only‡ [7]. Nevertheless, the lack of a closed-form cumulative density function (CDF) for a lognormal distribution makes it difficult to derive analytically the overall MTTF from various MTTF values as in Equation (10). Hence, we propose to exploit Monte-Carlo simulation which, for each failure mechanism, generates samples of lifetime following a lognormal distribution, and then combines the corresponding samples generated for different failure mechanisms to obtain the overall MTTF in a statistically sound manner. To this end, lifetime instances rather than MTTFs are operated/combined by Equations (9) and (10). The resulting MTTF is computed as the arithmetic mean across all combined lifetime instances.

In the proposed methodology, the lifetime distribution associated with a failure mechanism, $\boldsymbol{L_m}$, is modeled as a lognormal distribution:

$$\boldsymbol{L_m} \sim \ln \mathcal{N}(\mu, \sigma^2) \tag{11}$$

where μ and σ^2 are the mean and variance of a normal distribution, respectively.

The mean value of $\boldsymbol{L_m}$ is simply the nominal MTTF due to the specific failure mechanism:

$$MTTF_m = \exp(\mu + \sigma^2/2) \tag{12}$$

Therefore,

$$\mu = \ln(MTTF_m) - \sigma^2/2 \tag{13}$$

Based on the μ value calculated by Equation (13) with $\sigma = 0.5$ as suggested in [7][18], we can obtain a normal distribution accordingly and then generate a set of lifetime samples following a lognormal distribution (*i.e.*, $\ln \mathcal{N}(\mu, \sigma^2)$) for Monte-Carlo analysis. This way, the overall MTTF of a system can be evaluated as the expected value of combined Monte-Carlo (lifetime) samples, for which no CDF of lifetime reliability is required.

C. Correlation between TDDB and NBTI

Among our target failure mechanisms, TDDB and NBTI have mutual impact on the behavior of transistors. More precisely, TDDB decreases V_{gs} [19][20] while NBTI increases $|V_{th}|$ [12][13], both of which will slow down a given circuit according to the alpha-power law [21] and will lead

‡ One of the main reasons for adopting exponential distributions in the SOFR model is the simplicity of deriving combined MTTFs based on constant failure rates.

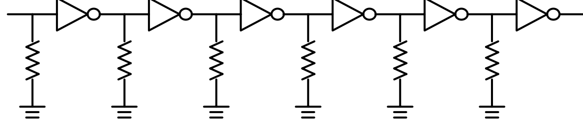

Figure 2. A chain of six inverters for joint TDDB and NBTI simulation

to progressive timing failures. Hence, TDDB and NBTI should not be treated separately for the purpose of lifetime evaluation. On the other hand, since the decreased V_{gs} due to progressive TDDB will also slow down the NBTI process, considering TDDB and NBTI jointly and extracting their correlation can further avoid underestimating lifetime reliability. The approach to deriving MTTF associated with correlated TDDB and NBTI is incorporated in our proposed methodology, and will be described in more detail later in Section IV.A.

IV. Deriving Mean-Time-to-Failure (MTTF)

Our methodology based on Monte-Carlo simulation needs to obtain the nominal MTTFs associated with different failure mechanisms such that, according to Equations (11)-(13), we can generate sets of Monte-Carlo samples and then combine them using MIN/MAX operations. In the following subsections, we show how to derive every MTTF of interest, jointly (for the case of correlated TDDB and NBTI) or separately (for the others).

A. MTTF due to Correlated TDDB and NBTI

To the best of our knowledge, this is the first work addressing the correlation between TDDB and NBTI for system-level lifetime evaluation. Existing work on the same problem is based on the standard/revised SOFR model [3]-[5] and/or do not consider the interdependent effects of TDDB and NBTI [7]-[9], resulting in substantial lifetime underestimation and unnecessary over-design for lifetime extension. Herein, we present our approach to analyzing and extracting the correlation between TDDB and NBTI.

The circuit-level model used for joint TDDB and NBTI simulation is shown in Figure 2, where the TDDB effect with respect to each gate is modeled as a time-varying resistor attached at the input [19][20]. According to the literature [20][22], the resistance ranges from hundreds of MΩ (fresh oxide) to a few kΩ (catastrophic breakdown). For NBTI simulation, we use the in-built reliability analysis tool (MOSRA) in HSPICE.

Due to the existence of resistors characterizing TDDB-induced gate oxide leakage, the input voltage for each gate is no longer ideal and is lower than the supply voltage at logic "1", which brings about three phenomena as follows:

(i) the NBTI effect on P-type transistors is diminished;
(ii) the rising propagation becomes slower;
(iii) the falling propagation becomes faster.

From the perspective of overall circuit performance, the second phenomenon is adverse while the first and third phenomena are actually beneficial. By simulating the chain of six inverters in Figure 2 via HSPICE, the long-term performance degradation seen when TDDB and NBTI are jointly considered is smaller than that when only NBTI is considered. This is because, from the simulation data, the first and third phenomena prevail over the second phenomenon. If we set a performance constraint to measure the MTTF of the inverter chain, the MTTF in the case of TDDB and NBTI becomes larger as compared to the case of NBTI alone. The observation that TDDB can recover a circuit from NBTI-induced performance degradation was recently confirmed by [20].

To derive the MTTF due to correlated TDDB and NBTI while considering temperature variations, we use the range of operating temperature from 300K to 400K with a discrete step of 10K in HSPICE simulation. Linear interpolation is employed if the actual temperature is between two simulation points.

B. MTTF due to EM

To find the MTTF of a metal wire in the 45nm technology, we use a publicly available tool called SysRel [23]. We provide SysRel with a copper interconnect of length 100μm driven by an inverter and driving another inverter, similar to the layout given in [24]. The operating temperature is fixed at 100°C. The MTTF of this specific circuit calculated by SysRel is about two years. Subsequently, based on this MTTF result and the actual operating temperature, we can scale and estimate the MTTF of a component/system running a combination of various workloads.

C. MTTF due to TC

The main task for deriving $MTTF_{\mathrm{TC}}$ is to compare the operating temperature ($T_{average}$) of every possible die structure of pre-defined size with its surrounding temperature ($T_{ambient}$). To this end, we use the results from an architecture-level temperature simulator, HotSpot [25], and extract the worst-case difference between $T_{average}$ and $T_{ambient}$ given a specific benchmark. The worst-case temperature difference will determine the MTTF under this benchmark. The weighted average MTTF across all benchmarks based on the workload profile is the overall MTTF of a system due to TC.

V. Experimental Results

The target system used for experimentation is the Alpha 21264 processor. The floorplan of a single Alpha 21264 core is taken from [25]. HotSpot [25] is used to obtain the temperature profiles associated with a set of SPEC CPU2000 benchmarks including *gzip*, *vpr*, *mesa*, *art*, *equake*, *ammp*, *vortex*, and *bzip2*. All benchmarks are assumed to be evenly executed on the processor. For a single-core application of Alpha 21264, we assume that each of the components in the processor is essential for reliable operation. Thus, the system lifetime is determined by the shortest MTTF among all components.

A. Results of Joint TDDB and NBTI Simulation

The first experiment is to demonstrate the non-orthogonality between the effects of V_{gs} and V_{th} variations on the propagation delay of a gate, where the V_{gs} and V_{th} variations result from TDDB and NBTI, respectively. In

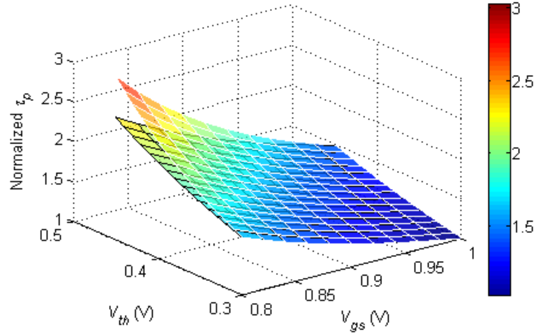

Figure 3. Normalized propagation delay (τ_p) versus V_{gs} and V_{th} variations

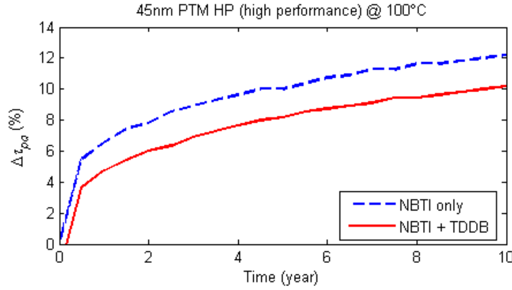

Figure 4. Results of HSPICE simulation for NBTI (and TDDB) analysis

Figure 3, the lower surface (with black grids) depicts the changes in propagation delay (τ_p) when the effects of V_{gs} and V_{th} variations are computed separately and then stacked up, while the upper surface (with white grids) depicts the τ_p changes due to joint treatment of V_{gs} and V_{th} variations. As shown in Figure 3, the case of joint treatment is always greater than the case of separate treatment, and the difference can be up to 20% in the worst case when V_{gs} is 0.8V (10kΩ resistance in Figure 2, nearly catastrophic) and V_{th} is 0.45V (10-year NBTI impact). Therefore, it is not accurate to consider TDDB-induced V_{gs} decrease and NBTI-induced $|V_{th}|$ increase separately for the evaluation of lifetime reliability.

Next, a more detailed analysis via HSPICE simulation is performed on the inverter chain in Figure 2. As it can be seen from Figure 4, the simulation for NBTI in conjunction with TDDB characterized as time-varying resistors reveals substantial performance recovery and a bit slower rate of NBTI degradation. If a performance constraint of 10% delay increase is applied, then $MTTF_{\mathrm{NBTI}}$ is 4.8 years while $MTTF_{\mathrm{TDDB+NBTI}}$ is 9.2 years in this specific case of 100°C operating temperature. At an even higher temperature of 125°C, $MTTF_{\mathrm{NBTI}}$ and $MTTF_{\mathrm{TDDB+NBTI}}$ are reduced to 2.6 and 4.4 years, respectively.

B. Results of MTTF for an Alpha 21264 Processor and a 16-core Chip-Multiprocessor Design

Before demonstrating the overall MTTF of a single-core Alpha 21264, we show the respective MTTFs due to EM and TC with workload-induced temperature variations considered. As shown in Figure 5, $MTTF_{\mathrm{EM}}$ and $MTTF_{\mathrm{TC}}$ vary widely from benchmark to benchmark, as a result of different thermal profiles and different temperature dependencies (see Equations (3) and (5)). On average, $MTTF_{\mathrm{TC}}$ is 1.16X larger than $MTTF_{\mathrm{EM}}$. Based on the results of $MTTF_{\mathrm{EM}}$ and $MTTF_{\mathrm{TC}}$ and the simulation data for TDDB and NBTI, the overall MTTF of the target system, an Alpha 21264 processor, is derived as follows.

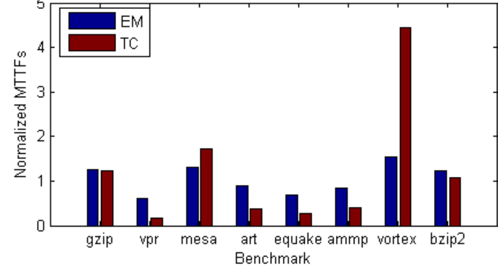

Figure 5. Normalized $MTTF_{\mathrm{EM}}$ and $MTTF_{\mathrm{TC}}$ results considering workload-induced temperature variations

As described in Section III.B, the proposed methodology exploits Monte-Carlo simulation which takes the nominal MTTFs associated with different failure mechanisms as input parameters and generates sets of 10^6 lifetime samples accordingly. The corresponding lifetime distributions for TDDB+NBTI, EM, and TC are shown on the left of Figure 6. By using the proposed methodology, the combined lifetime distribution is shown in Figure 6(d) with a mean value of 5.1 years, which is simply the overall MTTF of the system. Figure 6(e) shows the lifetime distribution obtained by the SOFR model and exhibits a pessimistic lifetime evaluation of 2.3 years (45.1%, as a fraction of 5.1). If more failure mechanisms are incorporated in the SOFR model, the resulting MTTF will be even more pessimistic. This property of SOFR does not reflect reality and explicitly reveals its deficiency of not being able to accurately analyze lifetime reliability, which depends on the effects (joint or independent) of various wear-out failure mechanisms. The inaccuracy of the SOFR model has been further confirmed in [9]. As demonstrated in [9], the error of SOFR assuming exponential distributions (constant failure rates) ranges from 20% up to 80% for a 4-core multiprocessor system-on-chip (MPSoC), and the error gets larger as the number of cores in an MPSoC increases. Finally, we employ our methodology with the correlation between TDDB and NBTI disregarded to emphasize the importance of joint consideration of TDDB and NBTI. The lifetime distribution is shown in Figure 6(f) and its mean value is 3.8 years (74.5%, as a fraction of 5.1).

The proposed methodology is also applied to a chip-multiprocessor (CMP) design consisting of 16 Alpha 21264 cores in a 4-by-4 mesh. According to [25], we classify SPEC CPU2000 benchmarks into two categories: intermediate and intensive thermal demands, and then randomly select eight benchmarks from each category to form a representative multi-program workload for the 16-core CMP. With this configuration and under the assumption that the CMP design is still operational as long as there exists at least one operational processor, the MTTF of the CMP implementation is 4.2 years.

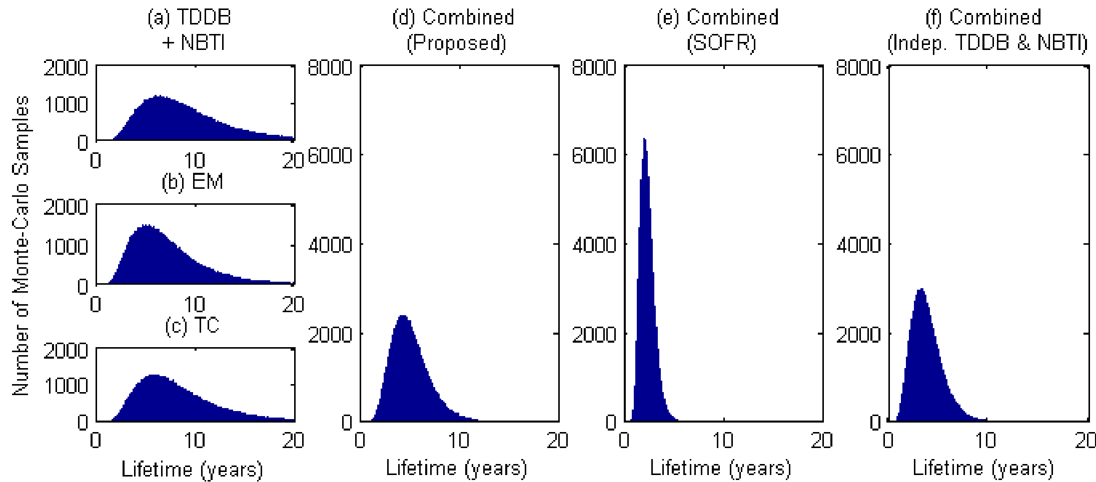

Figure 6. Lifetime distributions based on Monte-Carlo simulation for **(a)** TDDB+NBTI, **(b)** EM, **(c)** TC, and their combined distributions using **(d)** the proposed model, **(e)** the SOFR model, and **(f)** the proposed model with the correlation between TDDB and NBTI disregarded

VI. Conclusion

In this paper, we present a Monte-Carlo-based methodology for system-level lifetime evaluation considering temperature variations. Lifetime underestimation incurred by the standard/revised SOFR models is avoided, by distinguishing the impact of every individual mechanism and by extracting the correlation between TDDB and NBTI. HSPICE simulation on a chain of inverters indicates that the TDDB effect can indeed mitigate NBTI-induced performance degradation and thus implicitly enhance lifetime reliability. Furthermore, the lifetime of a system is more likely to be dominated by EM and TC, than TDDB and NBTI, if TDDB and NBTI are jointly considered.

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