Testing RF Circuits With True Non-Intrusive Built-In Sensors

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***Abstract*— We present a set of sensors that enable a built-in test in RF circuits. The key characteristic of these sensors is that they are non-intrusive, that is, they are not electrically connected to the RF circuit, and, thereby, they do not degrade its performances. In particular, the presence of spot defects is detected by a temperature sensor, whereas the performances of the RF circuit in the presence of process variations are implicitly predicted by process sensors, namely dummy circuits and process control monitors. We discuss the principle of operation of these sensors, their design, as well as the test strategy that we have implemented. The idea is demonstrated on an RF low noise amplifier using post-layout simulations.**

I. Introduction

Current and new generation electronic systems increasingly rely on RF circuits that enable wireless communication. The various manufacturing steps for such circuits may induce spot defects or large process variations that, in turn, may result in complete malfunction or in violation of a subset of specifications. Therefore, testing is necessary to verify that the specifications of every manufactured circuit are met and to guarantee that the functionality of the overall system is not jeopardized. However, testing the RF circuits of a system is a complex task which involves a very high cost. This is mainly due to the sophisticated automatic test equipment (ATE) of latest technology that is required, the long test times, the limited test access, etc.

Various design-for-testability (DfT) and built-in test (BIT) techniques have been proposed to date with the aim to reduce test cost and to improve testability. Examples include loop-back test [1], oscillation-based test [2], tuning-knobs for self-calibration [3], and built-in sensors [1], [4], [5], [6]. However, these techniques rely on connecting auxiliary circuitry along the signal path of the circuit under test (CUT) and, thereby, may degrade the matching and the overall performance. The fact that they are intrusive and that they often require to redesign the circuit to meet the desired specifications makes RF circuit designers rather reluctant to employ them.

In this paper, we propose sensors to be used in the context of RF BIT. The key characteristic of these sensors is that they are non-intrusive and transparent to the RF circuit since they do not tap into its signal path. Furthermore, they are generic (e.g. they can be used virtually for any RF circuit) and they provide a fast DC test response which lets us interface the CUT to basic ATE.

Non-intrusive process sensors were recently proposed with the aim to predict implicitly the performances of an RF CUT [7]. They consist of basic analog stages (called “dummy circuits”) and process control monitors (PCMs) that are placed on the same substrate, in close proximity to the CUT. They operate on the basis that they are subjected to the same process variations as the CUT. As a result, the performances of the CUT and the sensor measurements are expected to be highly correlated. In this case, alternate test can be used to infer the performances from the sensor measurements [8]. However, a random spot defect occurring within the CUT cannot be detected by the process sensors.

In this paper, we study a non-intrusive temperature sensor and we focus on its application for detecting defects within the CUT. The starting observation is that a defect will shift the power dissipated in the CUT which, in turn, will produce a temperature increase in the vicinity of the CUT that can be captured by the temperature sensor. The temperature sensor and the aforementioned process sensors offer a complete non-intrusive BIT solution for RF circuits to detect spot defects and to predict shifts in their performances.

The rest of the paper is structured as follows. Next, we present our case study which is an RF low noise amplifier (LNA). In Section III, we discuss the substrate thermal coupling mechanism, we present the design of the temperature sensor, and we show how it should be laid out on the die. In Section IV, we discuss the test strategy using the temperature sensor to detect defects. In Section V, we revisit the design of the temperature sensor in view of the test strategy. For the purpose of completeness, in Section VI, we discuss the operation of the process sensors and we provide a brief overview of alternate test. In Section VII, we demonstrate the operation of the various sensors on the case study using post-layout simulations. Finally, Section VIII concludes the paper.

II. CUT

Our case study is an inductive source-degenerated cascode LNA used in the 802.11g standard receivers that operate in the 2.4 GHz ISM band. The biasing stage is formed by resistors R1 and R2 and transistor M3. The inductors Lg and Ls and transistor M1 are chosen to provide appropriate input matching at 50Ω. The gain stage is composed by transistors M1 and M2. M1 provides the high gain, whereas M2 isolates the input from the output and reduces the Miller effect. The parallel Ld-Cd tank resonates at 2.4GHz and the resistor Rd controls the gain at this frequency.

III. Temperature sensor

A. Thermal coupling basics

The power dissipated by the CUT is a signature of its state and performances. The consequence of dissipating power is

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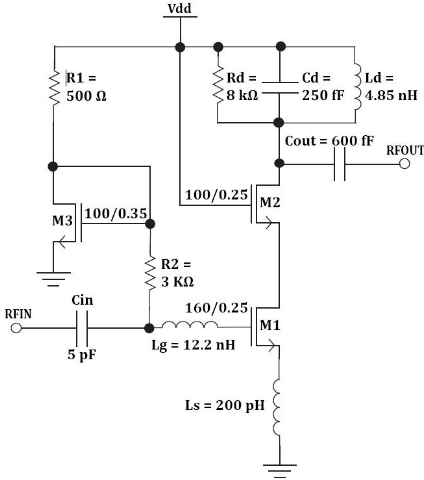

Fig. 1. CMOS low noise amplifier (LNA).

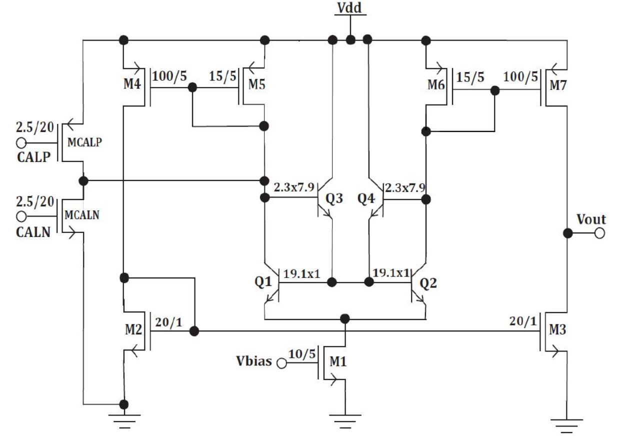

Fig. 2. BiCMOS differential temperature sensor.

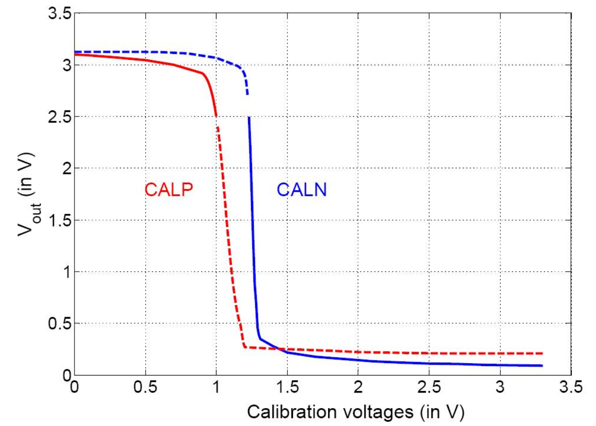

Fig. 3. Output of temperature sensor as a function of the calibration voltages.

self-heating which is conducted through the silicon substrate and results in thermal gradients across the silicon surface (known as the thermal coupling effect).

There exist several studies in the literature that focus on the characterization of the thermal coupling effect [9], [10], [11]. Although an accurate analysis requires solving the equation of the heat transfer across the silicon substrate, as a rule of thumb, we can draw the following main conclusions: (a) the transfer function of the thermal coupling behaves as a linear low-pass filter with a cut-off frequency between 10-100 kHz and an attenuation that increases as the distance between the CUT and the observation point increases. This implies that (b) only the low-frequency components of the power dissipated by the CUT generate measurable temperature increases, whereas the spectral components beyond the cut-off frequency do not induce any variation in the temperature. Nevertheless, (c) the high-frequency behavior of the CUT can be monitored with DC temperature measurements due to the Joule effect. In particular, the product of an AC voltage $v(t) = A\ cos(\omega_0 t)$ and an AC current $i(t) = B\ cos(\omega_0 t + \theta)$ at a frequency f_0 generates a DC component in the power spectrum with amplitude $\frac{AB}{2}$. In other words, the DC component of the dissipated power and, thereby, the temperature increase, is directly related to the AC voltage and current amplitudes at frequency f_0. Therefore, a temperature sensor placed in close proximity to the CUT reflects key information about the biasing point of the CUT and the RF operation.

B. Circuit design

We employed the differential temperature sensor shown in Fig. 2 [9]. It is based on an operational transconductance amplifier (OTA) whose differential pair is unbalanced due to the temperature difference between the npn bipolar transistors Q1 and Q2. In this work, Q1 is the transistor placed in close proximity to the CUT, whereas Q2 is placed far away from the CUT and any other heat source. Thus, Q1 is sensitive to variations in the DC power dissipated by the CUT, whereas Q2 is unaffected. The currents flowing through Q1 and Q2 are amplified through current mirrors (M4, M5) and (M6, M7) and converted to voltage through the output impedance of the two transistors M7 and M3. This differential sensor topology provides strong rejection of common-mode temperature variations which may affect Q1 and Q2, such as ambient temperature changes [9]. The small-signal output variation $\Delta Vout$ can be modeled as

$$\Delta Vout = Sdt \cdot \Delta T, \tag{1}$$

where ΔT = T_{Q1} - T_{Q2}, T_{Q1} is the temperature of Q1, T_{Q2} = T_{ref} is the temperature of Q2, and Sdt is the differential sensitivity which depends on the sensitivity of the collector currents to the temperature variation, the gain of the current mirrors, and the output impedance [9].

Transistors MCALP and MCALN allow to calibrate the temperature sensor against possible mismatches. They can be used to add or subtract current to one branch of the differential pair. Fig. 3 shows the output of the temperature sensor as a function of the two calibration voltages CALP and CALN. The transfer function for CALP (CALN) is drawn by fixing CALN (CALP) to a specific value. As it can be seen, $Vout$ decreases by increasing CALP or CALN while it increases by decreasing CALP or CALN. During calibration, either CALP or CALN is varied to avoid implementing two nested for loops.

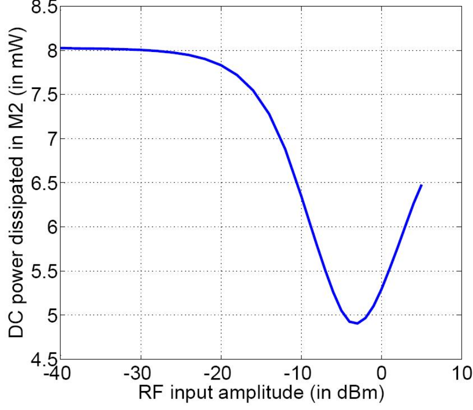

Fig. 4. DC power dissipation in transistor M2 of the LNA as a function of the amplitude of the RF signal applied to the input of the LNA.

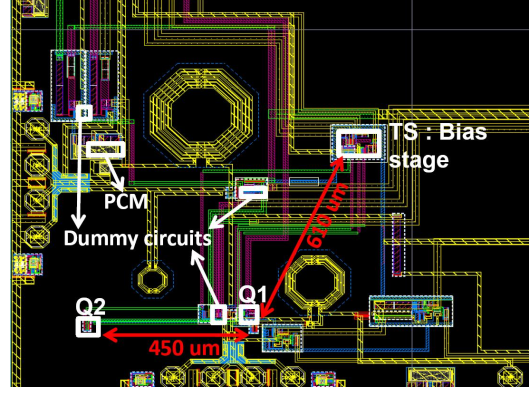

Fig. 5. Layout of the LNA with the embedded sensors.

In particular, to fix $Vout$ to a value $Vref$, we increase CALP if $Vout > Vref$ or we decrease CALN if $Vout < Vref$. The solid curves in Fig. 3 correspond to the calibration intervals for CALP and CALN in the case of $Vref = 2.5$V.

C. Placement on the die

Although transistors M1 and M2 in the LNA have the same geometry and exactly the same current flows through them, the AC drain-to-source voltage swing across the cascode transistor M2 is significantly larger since its output is a high-impedance node. Thus, the DC power dissipated by M2 will manifest more profoundly variations in the RF signal. For this reason, we have chosen to place the sensing transistor Q1 of the temperature sensor in close proximity to M2.

The DC power dissipated by M2 can be expressed as:

$$P_{M2} = P_{bias} + P_{RF} \tag{2}$$

where P_{bias} is the DC power dissipated due to the biasing condition and P_{RF} is the DC power dissipated due to the RF operation. It can be shown that

$$P_{M2} = Vds_{DC-M2}\, I_{DC} - \frac{1}{2}(gm_{M1}\, A)^2\, (R_d - \frac{1}{gm_{M2}}), \tag{3}$$

where Vds_{DC-M2} is the DC drain-to-source voltage of M2, I_{DC} is the DC current flowing through M2, gm_{M1} and gm_{M2} are the transconductances of M1 and M2, respectively, and A is the amplitude of the RF signal applied at the input of the LNA. Fig. 4 shows the DC power dissipated by M2 as a function of A. As it can be seen, the curve appears to have a minimum at a certain input amplitude and thereafter it increases as A increases. This effect, which is not taken into account in the small-signal model of eq. (3), is due to the nonlinearity of transistors. It can be shown that the minimum DC power dissipation is reached when A is approximately equal to the 1-dB compression point [12].

As shown in the layout of Fig. 5, the distance between Q1 and Q2 is more than 450μm. Furthermore, Q1 and Q2 are isolated from the rest of the components of the temperature sensor which are placed at a distance from Q1 and Q2 that is more than 610μm. Taking into account these layout precautions, the resulting change in the temperature difference between Q1 and Q2 will depend only on the variation in temperature of Q1 due to the DC power dissipated by transistor M2 in the LNA.

IV. Test strategy using the temperature sensor

The test strategy using the temperature sensor is divided into three modes that are carried out sequentially:

1) Mode DC-TS: In this mode, we begin the procedure of test by biasing the temperature sensor while the LNA is turned off. Our objective is to fix the output of the temperature sensor to the reference voltage $Vref$. This cannot be guaranteed by design due to offsets that result from mismatch and other process variations. For this purpose, we vary the gate voltages CALN and CALP of transistors MCALN and MCALP. The blue curve in Fig. 6 shows the transfer function of the temperature sensor at the end of this calibration step. The point 1 on this curve shows the operating point of the sensor (both Q1 and Q2 are at the reference temperature $T_{ref} = 25^o$C since the LNA is turned-off). In this mode, we also define the expected intervals in which CALN and CALP must be varied, in order to perform the calibration. Thus, in the test phase, if CALN and CALP go beyond these intervals, then we deduce that the temperature sensor is faulty and, in this case, the CUT should be tested instead through a typical functional test.

2) Mode DC-TS-CUT: This mode starts after accomplishing mode DC-TS and provided that the temperature sensor is healthy. In this mode, the LNA is biased and, under nominal conditions, it should dissipate DC power that induces an increase in the temperature in the vicinity of transistor Q1 (the temperature in the vicinity of Q2 stays at $T_{ref} = 25^o$C). Thus, the temperature sensor output saturates given its high sensitivity, as shown by point 2 on the blue curve of Fig. 6. It will be therefore necessary to make a second calibration, always through CALN and CALP, to bring the output of the temperature sensor back to $Vref$. The red curve in Fig. 6 shows the transfer function of the temperature sensor at the end of this calibration step and the point 3 on this curve corresponds to the operating point.

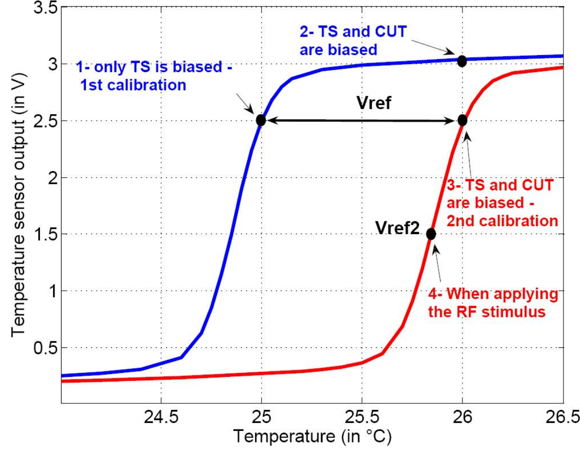

Fig. 6. Temperature sensor output versus temperature sensed by Q1.

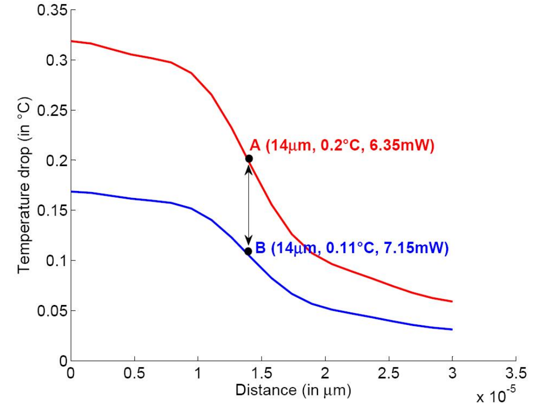

Fig. 7. Temperature variation $T_{ref} - T_{Q1}$ sensed by Q1. Q1 is placed at different distances from M2 following the axis along the width of M2.

The DC power dissipation of M2 and, thereby, the temperature sensed by Q1, may vary due to process variations occurring within the LNA. Thus, as in mode DC-TS, we need to define the intervals in which CALN and CALP must be varied in this step, in order to fix the output of the temperature sensor to $Vref$. In this mode, there are three possible scenarios:

- If the defect induces a large variation in the DC power dissipated by M2, then the temperature sensed by Q1 will vary significantly and the output of the temperature sensor will saturate. If by varying CALN and CALP in their predefined intervals we are not able to bring the output of the temperature sensor back to $Vref$, then the defect has been detected.
- If the defect induces little or no variation in the DC power dissipated by M2, then the temperature sensed by the device Q1 will remain practically unchanged. In this case, the output of the temperature sensor might vary slightly, which signifies that the LNA is faulty since, in the case of a fault-free LNA, the output of the temperature sensor should necessarily saturate.
- If the defect induces a DC power dissipation in M2 that saturates the output of the temperature sensor and through the calibration procedure we succeed to bring the output to the predefined value $Vref$, then the temperature sensor is not able to detect this defect in this mode. This is the case for defects that translate to short- or open-circuits across inductors or capacitors. In this case, we proceed to mode RF.

3) Mode RF: In this mode, we apply an RF signal to the input of the LNA. As a result, according to Fig. 4 and eq. (3), the DC power dissipated by M2 will be reduced and the operating point of the temperature sensor will change. This is shown for the nominal case by point 4 on the red curve of Fig. 6. The output of the temperature sensor is now fixed to $Vref2$. To detect defects in this mode, we define the expected interval where $Vref2$ should lie in the presence of process variations within the LNA. In this mode, if by applying the RF input signal the output of the temperature sensor exceeds this interval, then we conclude that the LNA contains a defect.

The test time using this strategy is dictated by the settling time of the temperature at the location of Q1 when the DC power dissipated by M2 undergoes a shift. It has been demonstrated experimentally that the settling time increases linearly with the distance between the heat source (e.g. M2) and the sensing device (e.g Q1) while it is independent of the magnitude of the shift in the DC power dissipated by the heat source [9]. For a distance $x = 20\mu m$ the settling time is around $T_s = 40\mu s$. The increase rate is around $\Delta T_s/\Delta x \approx 1.5$.

V. Design considerations and calibration limits

The design of the temperature sensor is related to the test strategy that is adopted. We proceeded as follows:

1) We chose $Vref = 2.5$V since the power supply voltage is equal to 3.3V.

2) We chose an RF stimulus with frequency 2.4 GHz and amplitude -11.5 dBm to be used in mode RF. As can be seen from Fig. 4, this stimulus causes the DC power dissipated by M2 to drop by 1.27mW with respect to mode DC-TS-CUT, i.e. from 8.05mW to 6.78mW. A Monte-Carlo simulation analysis shows that it can actually drop by 0.9mW to 1.7mW when considering process variations within the LNA, i.e. the DC power dissipated by M2 in mode RF is expected to lie between 6.35mW and 7.15mW in the absence of defects.

3) To examine the temperature variation at different distances from M2, we have solved the static heat transfer equation due to conduction within the silicon die using Fourier Series in rectangular coordinates with the quadruple approximation [12]. Since we are interested in differential temperature measurements, we can neglect to model the different layers that form the integrated circuit. Regarding the boundary conditions, we consider that the lateral and top surfaces are adiabatic and that the bottom surface is isothermal. Fig. 7 shows the temperature variation sensed by Q1 as a function of the distance between M2 and Q1. We consider only the expected minimum and maximum DC power dissipated by M2 in mode RF, e.g. 6.35mW and 7.15mW. Q1 is placed at different distances from M2 following the axis along the width of M2. We chose a distance equal to 14μm which implies a

temperature drop at the location of Q1 between 0.11^oC and 0.2^oC in mode RF with respect to mode DC-TS-CUT.

4) Given the above expected variations, the temperature sensor is designed with a sensitivity of 7V/^{o}C in the linear region. With this choice, in the RF mode, the output of the temperature sensor is expected to drop from $Vref$ to a value $Vref2$ in the range

$$1.1\text{V} < Vref2 < 1.73\text{V}. \quad (4)$$

5) We carry out corner simulations for the temperature sensor in mode DC-TS and, for each corner case, we calibrate the temperature sensor through CALN and CALP, in order to fix its output to $Vref$. This defines the calibration limits in mode DC-TS:

$$1\text{V} < CALP1 < 1.3\text{V} \quad (5)$$

$$1.04\text{V} < CALN1 < 1.24\text{V}. \quad (6)$$

6) We carry out corner simulations for the LNA in mode DC-TS-CUT. It turns out that the DC power dissipated by M2 is between 6.05 mW and 11 mW. We use these values in the thermal coupling model, in order to obtain the corresponding corner temperatures sensed by Q1. For each corner temperature, we calibrate the temperature sensor through CALN and CALP, in order to fix its output to $Vref$. This defines the calibration limits in mode DC-TS-CUT:

$$1.4\text{V} < CALP2 < 1.55\text{V} \quad (7)$$

$$1.15\text{V} < CALN2 < 1.3\text{V}. \quad (8)$$

VI. Process Sensors

Variations in process parameters can be categorized into inter-die (e.g. lot-to-lot, wafer-to-wafer, and wafer-level) and intra-die. Wafer-level variations are slow-varying and smooth which implies that neighboring areas on the same die are similarly affected [13]. Furthermore, for mature technologies, the intra-die variations are typically very small and inconsequential compared to inter-die variations. On the basis of these observations, it has been proposed to place basic circuits close to the CUT, without connecting them electrically, with the aim to monitor the CUT non-intrusively [7]. The underlying idea is that the basic circuits and the CUT will be subjected to the same inter-die variations, thus, by examining a large sample, we should expect to observe that the outputs of the basic circuits and the performances of the CUT will be highly correlated. In essence, we capitalize on the undesired process variations to facilitate a BIT approach for RF devices and minimize the test cost.

In this work, we placed close to the LNA basic analog stages (called "dummy circuits"), as shown in Fig. 8. These dummy circuits mimic part of the topology of the LNA. For example, we can see an analogy between transistors M1 to M3 in the LNA of Fig. 1 and transistors M1 to M3 in the bias circuit of Fig. 8(a). The dummy circuits of Fig. 8 offer a vectorless test and provide DC output voltages (e.g. DC1 to DC5). In

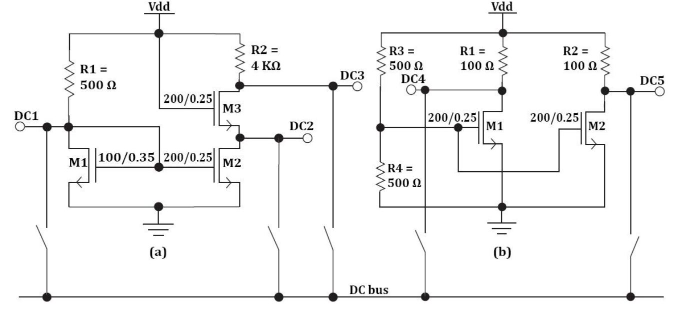

Fig. 8. Dummy circuits: (a) bias circuit with a current mirror and (b) CMOS gain stages with different geometries.

addition, we placed a metal-insulator-metal (MIM) capacitor close to the capacitor Cin of the LNA. The MIM capacitor is an example of a PCM that is typically placed on the wafer kerf to monitor the manufacturing process and identify off-target values of capacitance per unit area. PCMs are thrown away after slicing the wafer into dies. Instead, here we place them on each die close to the CUT and use them for monitoring the CUT during test. Finally, the dummy circuits and the PCMs are formed only by transistors, resistors, and capacitors, thus they occupy a very small area compared to the LNA and can be placed in the void areas of the layout, as shown in Fig.5.

The outputs of the dummy circuits and the value of the MIM capacitor are mapped to the performances of the LNA (e.g. scattering parameters, noise figure, 1-dB compression point, third order intercept point) using the alternate test principle [8]. In particular, we first collect a representative sample of CUT instances with the embedded sensors from different lots, wafers and sites on the same wafer. For each instance, we obtain the performances of the CUT and the sensor measurements. We then eliminate the outlier instances that have been identified by the temperature sensor to contain defects. Then, part of the remaining sample is used as a training set to fit regression functions mapping the process sensor measurements to each of the performances. The rest of the sample is used as a validation set to confirm that the regression functions have not been over-fitted.

In the test phase, the temperature sensor is used to detect the presence of defects within the CUT. If the CUT is free of defects, then the learned regression functions are used to predict its performances based solely on the process sensor measurements.

VII. Results

The circuits are designed using the Qubic4+ 0.25 μm BiCMOS technology provided by NXP Semiconductors. Special care is taken to account for the effects of capacitive, resistive, inductive, as well as mutual inductive layout-induced parasitics. The extraction of parasitics is carried out using the Assura tool. The following analysis is based on post-layout simulations that are performed using SpectreRF in Cadence.

We first generated an exhaustive list of short- and open-circuit defects that can occur in the LNA and the temperature sensor. In total, we consider 27 defects in the LNA and 32 defects in the temperature sensor. Each defect is injected one

TABLE I

RMS PREDICTION ERRORS (IN %) OF THE LNA PERFORMANCES USING PROCESS SENSORS.

S_{11}	S_{12}	S_{21}	S_{22}	NF	1-dB CP	IIP_3
2.9	0.6	1.3	2.2	1.1	1.6	3.3

at a time at the layout level, the layout is extracted including all parasitics, and a simulation is carried out following the test strategy explained in Section IV. A short-circuit is modeled with an interconnection between two metal layers, whereas an open-circuit is modeled by creating a cut in the metal layer. The analysis below shows that the temperature sensor is capable of detecting all of the injected defects:

- Mode DC-TS achieves a perfect coverage for the defects in the temperature sensor. The defects resulted in an output that cannot be calibrated to $Vref$ using $CALP$ and $CALN$ in the predefined intervals of eq. (5) and (6).
- Mode DC-TS-DUT detects 20 out of the 27 defects in the LNA. Some of these defects, in particular the short-circuits, incur a very high DC power dissipation in transistor M2, in the range of 24-38 mW, which saturates the temperature sensor. When varying CALN and CALP in their predefined intervals of eq. (7) and (8), we cannot bring the output below 2.9V, which implies the detection of the defect. Other defects, in particular the open-circuits, do not result in an appreciable variation in the DC power dissipated by M2 (the variation is in the order of uW). In this case, the temperature sensor output varies slightly which implies the detection of the defect since, otherwise, the temperature sensor should saturate.
- Mode RF detects the remaining 7 defects in the LNA. These defects are: an open-circuit in Cin, a short-circuit in Cin, an open-circuit in Cout, a short-circuit in Cout, a short-circuit in Lg, a short circuit in Ls, and a short circuit between the gate and the drain of M2 (which is equivalent to a short circuit across Rd, Cd, or Ld). For these defects, when applying the RF input signal, the DC power variation in M2 induces a variation in the output of the temperature sensor outside the predefined interval for $Vref2$ in eq. (4).

Table I shows the error (in %) when predicting the performances of the LNA based solely on the process sensors. The regression functions in the prediction models are learned based on 700 training instances generated through a post-layout Monte Carlo simulation with parasitic extraction where we consider both inter-die and intra-die variations. Another independent set of 300 validation instances generated in the same way was employed to evaluate the prediction accuracy. As can be observed from the figures in Table I, the prediction accuracy is acceptable since it can be considered comparable to the measurement repeatability errors.

VIII. CONCLUSION

We presented a built-in test approach for an RF LNA that relies on non-intrusive sensors. A temperature sensor monitors the DC power dissipated in the cascode transistor of the LNA and indicates whether a defect exists within the LNA. The operation of the temperature sensor is based on the substrate coupling mechanism. The test strategy is composed of three different modes, two DC and one RF, yet it was shown that the majority of defects within the LNA are detected by a DC mode. Furthermore, in the RF mode, only an RF stimulus is required since the test response is DC. In addition to the temperature sensor, we employed process sensors to infer implicitly the performances of the LNA based on the alternate test principle. It was shown that the process sensors can be used to build accurate prediction models. The analysis was carried out using post-layout simulations that take into consideration the extraction of parasitics.

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