Panel: What Is EDA Doing for Trailing Edge Technologies?

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Over the last decade, the semiconductor industry has advanced CMOS technology from 90 to 22/20 nanometers, and the EDA industry has developed a great deal of tools, methodologies, and flows to help "gigascale" design, implementation and verification, at these "leading edge" technology nodes. However, in 2010 approximately 75% of design starts used 130 nanometers or greater CMOS technologies [1], and 25% of wafers were fabricated using these "trailing edge" technologies [2]. There are possibly more designers working at 130 nanometers and above than at 90 nanometers and below, and there is certainly much more to electronics than just digital CMOS and microprocessors, and in order for the electronic industry to continue delivering on promises, "More than Moore" is needed, besides "More of Moore". What is EDA doing – or what should EDA do – in order to help design implementation and verification at trailing edge technologies?

[1] IBS 2011
[2] VLSI Research 2011

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