Measuring and Improving the Robustness of Automotive Smart Power Microelectronics

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Abstract—**Automotive power micro-electronic devices in the past were low pin-count, low complexity devices. Robustness could be assessed by stressing the few operating conditions and by manual analysis of the simple analog circuitry. Nowadays complexity of Automotive Smart Power Devices is driven by the demands for energy efficiency and safety, which adds the need for additional monitoring circuitry, redundancy, power-modes, leading even to complex System-on-chips with embedded uC cores, embedded memory, sensors and other elements. Assessing the application robustness of this type of microelectronic devices goes hand-in-hand with exploring their verification space inside and to certain extends outside of the specification. While there are well established methods for standard functional verification, methods for application oriented robust verification are not yet available. In this paper we present promising directions and first results, to explore and assess device robustness through various pre- and post-Si verification and design exploration strategies, focusing on metamodeling, constrained-random verification and hardware-in-the-loop experiments, for exploration of the operating space.**

Keywords-component; Automotive Smart Power IC, Robustness, Metamodeling, Constrained-Random-Verification

I. INTRODUCTION

As automotive power microelectronic products evolve from simple power switches to complex Systems-on-Chip, the robustness of these systems is a goal of every design. On one hand, it needs to be built-in by proper construction methods; on the other hand it must be assessed pre- and post-Si in the context of an ever increasing verification space. Robustness can be seen as the ability to work safely under all possible operating conditions or, not to fail under any allowed condition. Its assessment consists mainly in finding the worst operating condition where the device does not yet fail, which is a matter of observability and of efficiency in searching into a multi-dimensional space. In pre-Si simulation the search is limited by total simulation time and in post-Si the search is limited by real time.

Standard ways like corner case analysis and grid based search methods (e.g. shmoo [1] in post-Si) have shortcomings. In corner analysis, the assumption is made, that the worst case operating condition is always a minimum or maximum condition, which is not always the case. Though proposals have been made to decrease the simulation time i.e. increase coverage for corner tests [2], such directions must be explored more. For classical grid based sampling the observability is limited by the grid size and only suitable for low dimensional searches. The curse of dimensionality does not exist for gradient-based multi-dimensional search algorithms. Real-silicon device behavior is most often linear, but in cases where discontinuous exist, local search algorithms, like gradient search, are trapped in local extrema or cannot compute at all. We propose advanced methods which cope with these difficulties: Design of Experiment based methods extract as much information as possible out of a limited number of simulation runs or post-Si tests. [3] Several alternative directions, which explore where the system is robust, are also under research: advanced Monte Carlo methods e.g. Importance Sampling [4], as well as extensions to grid sampling, such as classification and evolutionary algorithms [5, 6]. They are iterative search methods with increased potential to improve the coverage of highly-dimensional verification spaces, for a possibly discontinuous system behavior.

Finally there is the need to deploy such verification experiments on hardware and assess the robustness of the real silicon device. While there is much freedom in the definition of a simulation testbench with application-like sources and loads, like motors, incandescent lamps, squibs, LEDs, batteries etc., most corresponding hardware setups are not configurable; robustness cannot be assessed for the full range of possible applications. Hardware-in-the-loop systems are in most cases the only systems fast and flexible enough to provide this functionality but are not available for power loads needed by automotive applications. For post-Si assessment of robustness we propose a system using reconfigurable load models on FPGA and push-pull drivers for power load emulation.

II. DESIGN OF EXPERIMENTS FOR ROBUST SYSTEMS

Design of Experiments (DoE) is an approach to plan and analyze real life as well as simulated experiments [3]. In the DoE framework, experiments are sets of tests which control the input variables referred to as factors of the system in order to identify reasons for changes in the overall performance (response). Factors can be operating conditions, parameters of the DUT etc. Statistical DoE plans experiments with minimum tests as to extract statistical significance about factor effects and how they interact. Regression extracts the effects which best fit simulation data and approximates the response with a multivariate polynomial i.e. a metamodel.

* This research project is supported by the German Government, Federal Ministry of Education and Research under the grant number 01M3195.
978-3-9810801-8-6/DATE12/©2012 EDAA

Robustness can be characterized by determining where the response is compliant to requirements, or less sensitive to factors. These issues are analyzed in what follows. To exemplify, Figure 1 shows the metamodel as it was fitted by Spectre simulation results of a voltage regulator, while varying the temperature and input voltage which must be stabilized. A CCD (Central Composite Design) [3] i.e. an experiment designed to find linear, interaction and quadratic factor effects was applied and it involves no more than 15 runs.

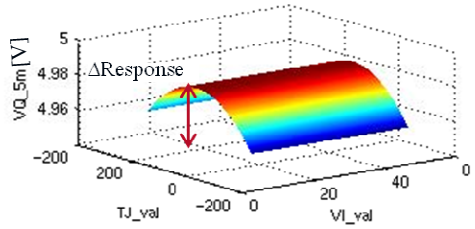

Figure 1. Metamodel of the Output of a Voltage Regulator

The total response variance can be quantified and compared against the expected or admitted thresholds. The extreme response values, and the corresponding factors can be determined by applying standard optimization algorithms to the metamodel. The predictions on ΔResponse (max.-min.) were simulated and compared against a new set of values, in order to validate the approach. Furthermore, iterative gradient-based searches are able to improve these estimates.

The metamodel can also be used reversely, to find the factor space where the response complies with requirements, i.e. where it does not exceed the admitted threshold and its variance is under control. This directly answers the question of where the system is compliant with the spec, which is of interest for any robustness assessment problem. Once the factors which are significant are determined, controlling their ranges in order to get the least variable response addresses the robust optimization problem. This is a direction currently under research.

The approach is restricted by the assumptions of continuity of the response and practical limit for the number of factors. This can be addressed by extensions such as improvement of convergence when only small discontinuities exist, as well as applying the algorithms locally instead of globally.

III. CONSTRAINED-RANDOM VERIFICATION

Constrained-random verification is a well developed and mature methodology for the verification of large digital designs [7]. The method relies on the algorithmic generation of mostly digital test patterns using an abstract description of the digital design, e.g. in SystemC, Verilog, Matlab or any other machine readable form; with additional constraints given, the constrained random generator is able to derive a valid pseudo-random sequence of digital device input and expected digital device output. The process is coverage driven, which means a coverage target is defined and the process stops, when the target is reached or the time is exceeded.

If we take (digital) coverage of constrained-random verification as a robustness measure, also CRV can add to a robustness assessment of Smart Power Microelectronics, but due to the mixed-signal and power related behavior this may not be enough for safety related products. Though there are attempts to extend CRV to mixed-signal designs [8], this is only partly systematically explored yet. For one part of the verification space that is related to the power profiles of the supply (battery and other secondary supplies) there exist standard random ramp profile methods, but there is mostly no generic method for loads and other sources.

IV. HARDWARE-IN-THE-LOOP FOR POST-SI VALIDATION

Evaluating the robustness of silicon devices and assessing robustness measures in realistic application-like environments is hard to achieve due to limited similarities between realistic automotive power-loads and standard lab or test equipment, which is built to provide accurate currents and voltages, but not to resemble realistic complex load behavior. For full hardware exploration of the verification space a configurable load is required, that can emulate typical automotive loads with their own spread of parameters to assess the real device robustness, see for example complex start-up switching of an incandescent lamp through a high-side switch in Figure 2. Hardware-in-the-Loop systems are the only configurable systems fast enough to resemble inductive, capacitive and thermally changing loads, like incandescent lamps, electrical motors or other. A hardware-in-the-loop system for automotive power loads will be target of investigation.

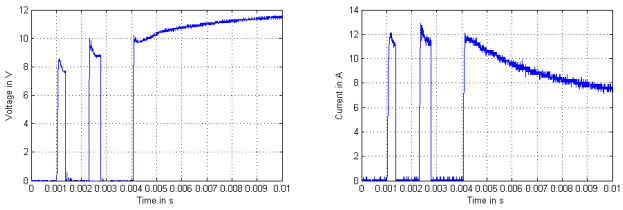

Figure 2. Voltage (left) and Current (right) over time for real-time emulated incandescent lamp and Smart High-Side Switch

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