Mach-Zehnder Interferometer Based Design of All Optical Reversible Binary Adder

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***Abstract*—In recent years reversible logic has emerged as a promising computing model for applications in dissipation less optical computing, low power CMOS, quantum computing, etc. In reversible circuits there exist a one-to-one mapping between the inputs and the outputs resulting in no loss of information. Researchers have implemented reversible logic gates in optical computing domain as it can provide high speed and low energy requirement along with easy fabrication at the chip level [1]. The all optical implementation of reversible gates are based on semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI) due to its significant advantages such as high speed, low power, fast switching time and ease in fabrication. In this work we present the all optical implementation of an n bit reversible ripple carry adder for the first time in literature. The all optical reversible adder design is based on two new optical reversible gates referred as optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) and the existing all optical Feynman gate. The two new reversible gates ORG-I and ORG-II are proposed as they can implement a reversible adder with reduced optical cost which is the measure of number of MZIs switches and the propagation delay, and with zero overhead in terms of number of ancilla inputs and the garbage outputs. The proposed all optical reversible adder design based on the ORG-I and ORG-II reversible gates are compared and shown to be better than the other existing designs of reversible adder proposed in non-optical domain in terms of number of MZIs, delay, number of ancilla inputs and the garbage outputs. The proposed all optical reversible ripple carry adder will be a key component of an all optical reversible ALU that can be applied in a wide variety of optical signal processing applications.**

I. Introduction

Among the emerging computing paradigms, reversible logic appears to be promising due to its wide applications in emerging technologies such as quantum computing, quantum dot cellular automata, optical computing, etc [2], [3], [4], [5], [6], [7], [8], [9]. Reversible logic is also being investigated for its promising applications in power-efficient nanocomputing [10], [11]. Reversible circuits are those circuits that do not lose information during computation and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between the input and the output vectors. The constant input in the reversible circuit is called the ancilla input, while the garbage output refers to the output which exists in the circuit just to maintain one-to-one mapping but is neither one of the primary inputs nor a useful output. The inputs regenerated at the outputs are not considered as garbage outputs [12].

Optical implementation of reversible logic gates is gaining the attention of researchers as photon can provide the unmatched high speed and can have the information stored in a signal of zero mass. Reversible logic gates implemented in optical computing can be useful to overcome the limits imposed by conventional computing with minimal energy dissipation, and is also considered one of the feasible alternatives to implement quantum computing [13], [14], [15], [16]. Recently, researchers have also implemented reversible logic gates such as Feynman gate, Toffoli gate, Peres gate and Modified Fredkin gate using semiconductor optical amplifier (SOA)-based Mach-Zehnder interferometer (MZI) optical switch due to its significant advantages such as high speed, low power, fast switching time and ease in fabrication [1], [4], [17].

In this work we present the all optical implementation of an n bit reversible ripple carry adder for the first time in literature. The all optical reversible adder design is based on two new optical reversible gates referred as optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) and the existing all optical Feynman gate. The two new reversible gates ORG-I and ORG-II are proposed as they can implement a reversible adder with reduced optical cost which is the measure of number of MZIs switches and the propagation delay, and with zero overhead in terms of number of ancilla inputs and the garbage outputs. In any reversible circuit the ancilla inputs and the garbage outputs are considered as overhead and need to be minimized, as more the number of ancilla inputs and the garbage outputs more will be the number of the I/O pins in the circuit [18]. The proposed all optical reversible adder design based on the ORG-I and ORG-II reversible gates are compared and shown to be better than the other existing designs of reversible adder proposed in non-optical domain in terms of number of MZIs, delay, number of ancilla inputs and the garbage outputs. The proposed all optical reversible ripple carry adder will be useful to design an all optical reversible ALU that can be applied in a wide variety of optical signal processing applications.

The paper is organized as follows: the basics of all optical reversible logic, the all optical implementation of Feynman

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gate, and the two new proposed gates optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) are presented in Section II; the design methodologies of proposed all optical reversible ripple carry adder is discussed in Section III. The delay and optical cost analysis of proposed optical reversible adder design is addressed in Section IV, while Section V and Section VI provide the comparison of n bit optical reversible ripple carry adders and conclusions, respectively.

II. Basics of All Optical Reversible Logic

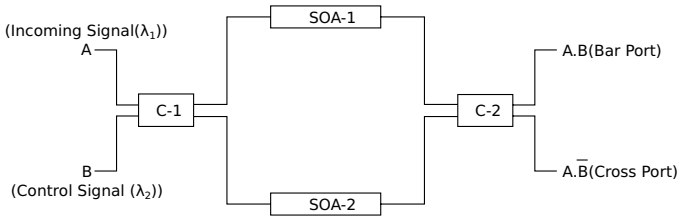
In recent years, the Mach-Zehnder interferometer (MZI) based optical switch has drawn interest of many researchers in the field of all optical reversible logic [4], [1], [17], [19]. A design of all optical MZI switch is shown in Fig. 1(a). A MZI based all optical switch can be designed using 2 Semiconductor optical amplifier (SOA-1, SOA-2) and two couplers (C-1, C-2). The operating principle of MZI based all optical switch can be explained as follows:

In MZI there are two inputs ports A and B and two output ports called as bar port and cross port, respectively, as shown in Fig. 1(a). At the input ports, the optical signal coming at port B is considered as the control signal (λ_2) and the optical signal coming at port A is considered as incoming signal (λ_1). The working of the MZI can be explained as: (i) when there is an incoming signal at port A and the control signal at port B then there is a light present at the output bar port and there is no light present at the output cross port, (ii) in the absence of control signal at input port B and incoming signal at input port A then the outputs of MZI are switched and results in the presence of light at the output cross port and no light at the bar port. In our work, we consider no light or absence of light as the value 0. The above behavior of MZI based all optical switch can be written as boolean functions having inputs to outputs mapping as (A, B) to (P=AB, $Q = A\bar{B}$), where A (incoming signal), B (control signal) are the inputs of MZI and P (Bar Port), Q (Cross Port) are the outputs of MZI, respectively. A block diagram of MZI based all optical switch is shown in Fig. 1(b). *In our work the optical cost and the delay (Δ) of MZI based all optical switch is considered as unity*.

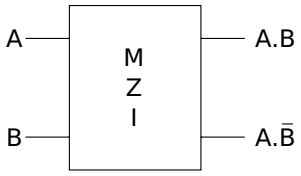
Next, we discuss the existing all optical Feynman gate and the two new reversible gates proposed in this work which are referred as optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II).

A. All optical Feynman gate

The Feynman gate (FG) is a 2 inputs and 2 outputs reversible gate. It has the mapping (A, B) to (P=A, Q=A$\oplus$B) where A, B are the inputs and P, Q are the outputs, respectively. The Feynman is also referred as the Controlled-Not gate (CNOT) as when the input A=1 then the output generated at Q will be complement of input B that is Q=$\bar{B}$. A Feynman gate can be implemented using 2 MZI based all optical switch, 2 beam combiner (BC) and 2 beam splitter (BS) in all optical reversible computing [4]. As the beam combiner (BC) simply combines the optical beams while the beam splitter simply splits the beams into two optical beams, hence researchers do not consider them in the optical cost and the delay calculations [20], [21]. Figures 2(a) and 2(b) show the block diagram and the all optical implementation of the Feynman gate. As the Feynman gate can be implemented using 2 MZI based optical switches thus the optical cost of Feynman gate is considered as 2. In the all optical implementation of the Feynman gate as two MZIs switches are working in parallel thus the delay of the optical Feynman gate is considered as 1Δ.

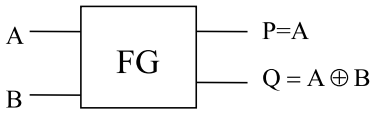


(a) Semiconductor optical amplifier based Mach-Zehnder interferometer

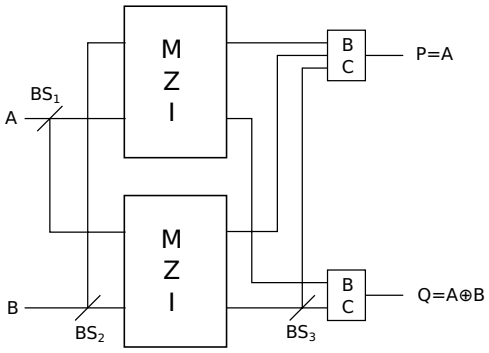


(b) Mach-Zehnder interferometer

Fig. 1. Mach-Zehnder interferometer based all optical switch



(a) Feynman gate



(b) All optical implementation of the Feynman gate

Fig. 2. Feynman gate and its all optical implementation

B. Proposed all optical reversible gates

We propose two new optical reversible gates that are most efficient to design an all optical reversible ripple carry adder with input carry. The proposed all optical reversible gates are referred as optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II). The block diagrams of optical reversible gate I and optical reversible gate II are shown in Fig.

3(a) and 3(b), respectively. The optical reversible gate I (ORG-I) is a 3 inputs and 3 outputs reversible gate with mapping of inputs (A, B, C) to outputs as ($P = AB + (A \oplus B)C$, $Q = A \oplus B$, $R = A\bar{B} + \overline{(A \oplus B)}C$). The optical implementation of ORG-I is shown in Fig. 3(c) and has 3 MZI based optical switch (MZI), 4 beam splitter (BS) and 3 beam combiner (BC). The optical reversible gate II is a 3 inputs and 3 outputs reversible gate with mapping between the inputs (A, B, C) and outputs (P, Q, R) as (A, B, C) to ($P = A\bar{B} + BC$, $Q = \bar{B}C + \bar{A}B$, $R = AB + \bar{B}C$). The optical implementation of an ORG-II is shown in Fig. 3(d) and has 3 MZI based switches (MZI), 4 beam splitters (BS) and 3 beam combiners (BC). The truth table representation of optical reversible gate I and optical reversible gate II are shown in Tables I and II, respectively. As the cost of an all optical reversible logic gate is the number of MZI based optical switches thus the optical cost of ORG-I and ORG-2 will be 3. In ORG-I out of 3 MZI switches, 2 MZI switches work in parallel thus its delay is considered as 2Δ. In optical implementation of ORG-II, all three MZI based optical switches works in parallel thus its delay is considered as 1Δ.

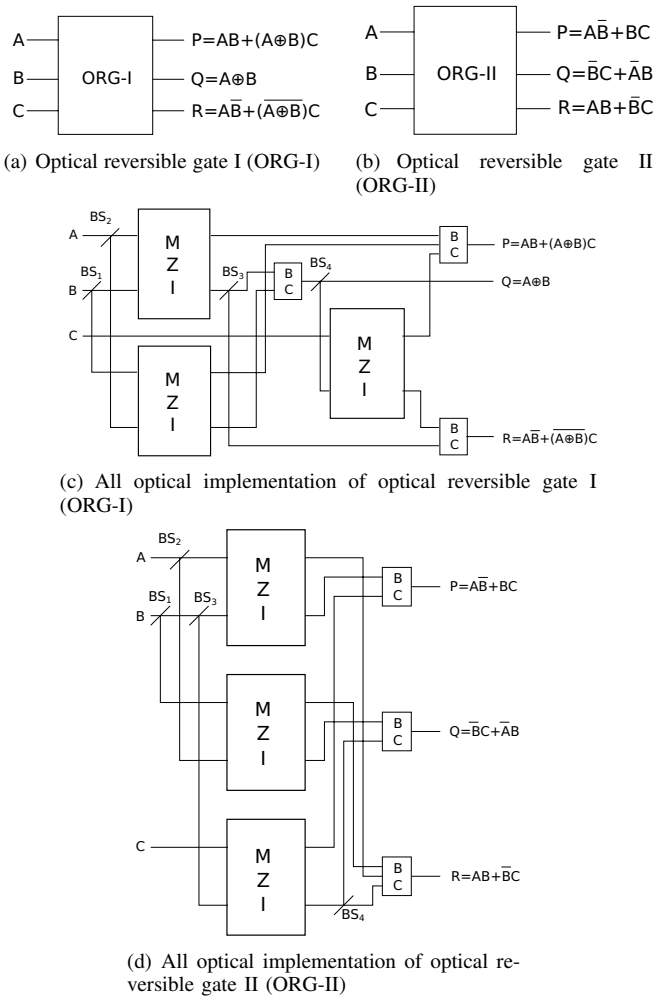
TABLE I
TRUTH TABLE OF OPTICAL REVERSIBLE GATE I (ORG-I)

A	B	C	$AB + (A \oplus B)C$	$A \oplus B$	$A\bar{B} + \overline{(A \oplus B)}C$
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	0	1

TABLE II
TRUTH TABLE OF OPTICAL REVERSIBLE GATE II (ORG-II)

A	B	C	$A\bar{B} + BC$	$\bar{B}C + \bar{A}B$	$AB + \bar{B}C$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	1	0	1

The graphical representation of optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) are shown in Figs. 4(a) and 4(b), respectively. As the proposed gates are new and performs unique boolean operations thus we have used three different geometries (triangle, pentagon and square) for their graphical representation. It is to be noted that these geometries are simply used to distinguish ORG-I and ORG-II from other existing optical reversible gates and hence provides a unique graphical representation. An important property of optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) is when the outputs of optical reversible gate I is connected to the inputs of optical reversible gate II in series it results in a 1 bit optical full adder design. This property is illustrated in Fig. 4(c) which shows that the proposed gates can implement an optical 1 bit reversible full adder with optical cost of 6 and delay of 3 Δ.



(a) Optical reversible gate I (ORG-I)

(b) Optical reversible gate II (ORG-II)

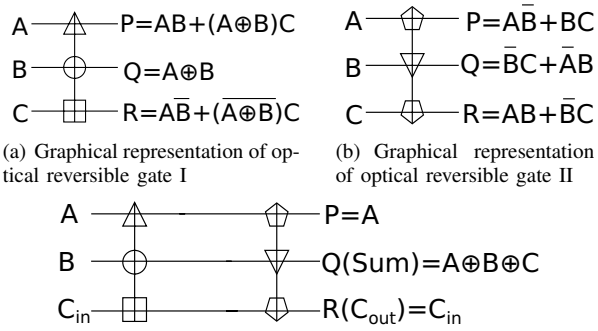
(c) All optical implementation of optical reversible gate I (ORG-I)

(d) All optical implementation of optical reversible gate II (ORG-II)

Fig. 3. Optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) and all optical implementations

III. PROPOSED ALL OPTICAL REVERSIBLE RIPPLE CARRY ADDER WITH INPUT CARRY

The optical reversible ripple carry adder with input carry (c_0) is designed without any ancilla inputs and the garbage outputs, and with less optical cost and reduced delay compared to the existing non-optical reversible ripple carry adder design approaches [22], [23], [24]. The comparison is done with non-optical reversible ripple carry adders as the proposed work of the design of optical reversible adder is the first attempt in the direction of implementing reversible adder in optical computing. Consider the addition of two n bit numbers a_i and b_i stored at memory locations A_i and B_i, respectively, where $0 \leq i \leq n-1$. The input carry c_0 is stored at memory location A_{-1}. Further, consider that



(a) Graphical representation of optical reversible gate I

(b) Graphical representation of optical reversible gate II

(c) Optical reversible full adder design using proposed gates

Fig. 4. Graphical representation of proposed optical reversible gates and design of an optical reversible full adder

memory location A_n is initialized with z $\in \{0, 1\}$. At the end of the computation, the memory location B_i will have s_i, while the location A_i keeps the value a_i for $0 \leq i \leq n-1$. Further, at the end of the computation, the additional location A_n that initially stores the value z will have the value $z \oplus s_n$, and the memory location A_{-1} keeps the input carry c_0 (here s_n represents the output carry of the n bit reversible ripple carry adder). Thus A_n will have the value of s_n when z=0. Here, s_i is the sum bit produced and is defined as:

$$s_i = \begin{cases} a_i \oplus b_i \oplus c_i & \text{if } 0 \leq i \leq n-1 \\ c_n & \text{if } i = n \end{cases}$$

where c_i is the carry bit and is defined as:

$$c_i = \begin{cases} c_0 & \text{if } i = 0 \\ a_{i-1}b_{i-1} \oplus b_{i-1}c_{i-1} \oplus c_{i-1}a_{i-1} & \text{if } 1 \leq i \leq n \end{cases}$$

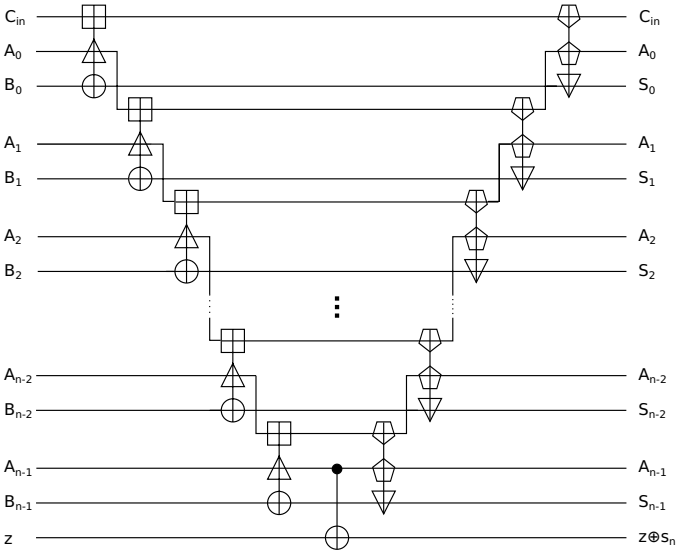


Fig. 5. Circuit generation of optical reversible n bit adder using proposed optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II)

The generalized methodology of designing the n bit optical reversible ripple carry adder with input carry is shown in Fig. 5. The methodology is explained below along with an illustrative example of 4 bit optical reversible ripple carry adder. The illustrative example of 4 bit all optical reversible ripple carry adder is shown in Fig. 6 that can perform the addition of two 4 bit numbers a=$a_0...a_3$ and b=$b_0...b_3$, and has the input carry c_0. The details of the proposed approach that uses optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) along with Feynman gates to minimize the optical cost and the delay, and has zero overhead in terms of garbage outputs and the ancilla inputs is discussed below.

Steps of Proposed Methodology for Optical Reversible Adder

1) The Step 1 has the following two sub-steps:
   a) For i=0 to n-1:
   At locations A_{i-1}, A_i and B_i apply the optical reversible gate I (ORG-I) gate such that the locations A_{i-1}, A_i and B_i are passed to the inputs C, A and B, respectively, of the optical reversible gate I (ORG-I).

   b) Further for i=n: apply the optical Feynman gate at pair of locations A_{n-1}, A_n.
2) For i=n-1 to 0:
   At locations A_{i-1}, A_i and B_i apply the optical reversible gate II (ORG-II) gate such that the location A_{i-1}, B_i and A_i are passed to the inputs C,A, B respectively, of the optical reversible gate II (ORG-II). After this step we will have the complete working design of the optical reversible adder an example of which is shown for addition of 4 bit numbers in Fig.6.

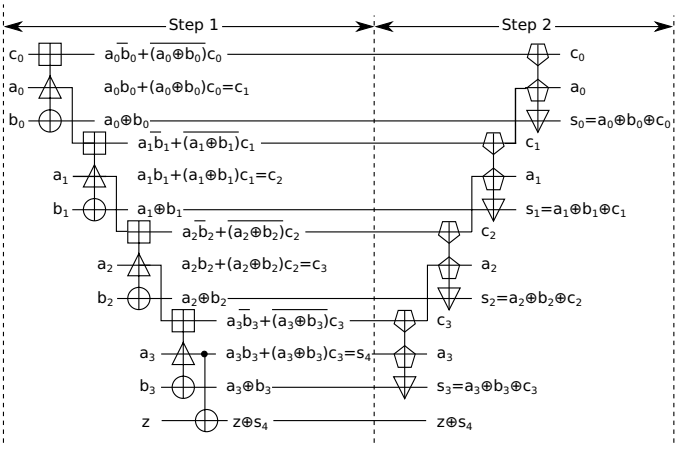


Fig. 6. Proposed optical reversible 4 bit adder

Theorem : *Let a and b are two n bit binary numbers represented as a_i and b_i, c_0 is the input carry (c_0), and z $\in \{0, 1\}$ is the another 1 bit input, where $0 \leq i \leq n-1$, then the proposed design steps of methodology result in the ripple carry adder circuit that works correctly. The proposed design*

methodology designs an n bit adder circuit that produces the sum output s_i at the memory location where b_i is initially stored, while the location where a_i is initially stored is restored to the value a_i for $0 \leq i \leq n-1$. Further, the memory location where z is initially stored transforms to $z \oplus s_n$, and the memory location where the input carry c_0 is initially stored is restored to the value c_0.

Proof: The proposed approach will make the following changes on the inputs that are illustrated as follows:

1) Step 1: The step 1 of the proposed approach transforms the input states to

$$\left|a_0\bar{b_0} + (\overline{a_0 \oplus b_0})c_0\right\rangle \left(\bigotimes_{i=0}^{n-1} |c_{i+1}\rangle \, |a_i \oplus b_i\rangle\right) |z \oplus s_n\rangle$$

where c_i is the carry bit and is defined as:

$$c_i = \begin{cases} c_0 & \text{if } i = 0 \\ a_{i-1}b_{i-1} \oplus b_{i-1}c_{i-1} \oplus c_{i-1}a_{i-1} & \text{if } 1 \leq i \leq n \end{cases}$$

For illustrative purpose, the transformation of the input states of a 4 bit all optical reversible adder circuit after step 1 is shown in Fig.6.

2) Step 2: The step 2 of the proposed approach transforms the input states to

$$|c_0\rangle \left(\bigotimes_{i=0}^{n-1} |a_i\rangle \, |s_i\rangle\right) |z \oplus s_n\rangle$$

For illustrative purpose, the transformation of the input states of a 4 bit all optical reversible adder circuit after step 2 is shown in Fig.6.

Thus we can see that the proposed two step will produce the sum output s_i at the memory location where b_i is stored initially, while the location where a_i is stored initially will be restored to the value a_i for $0 \leq i \leq n-1$. The memory location where z is stored will have $z \oplus s_n$ and the memory location where the input carry c_0 was stored initially will be restored to the value c_0. This proves the correctness of the proposed methodology of designing the all optical reversible ripple carry adder with input carry.

IV. Delay and Optical Cost Analysis

The proposed optical reversible ripple carry adder with input carry can be designed by following the two steps described previously in Section III. The delay and optical cost analysis of the proposed adder are preformed by analyzing the steps involved in the design of all optical reversible ripple carry adder with input carry.

- Step 1.a of the proposed methodology requires n optical reversible gate I (ORG-I) that works in series. Thus this step will have the optical cost of $3n$ and delay of $2n\Delta$. Step 1.b has a CNOT gate that is used to generate the carry out and it contributes the optical cost of 1 and delay of 1Δ. Thus, the Step 1 has the total optical cost of $3n+1$ and delay of $2n + 1\Delta$
- Step 2 of the proposed methodology requires n optical reversible gate II (ORG-II) working in series thus this step has the optical cost of $3n$ and delay of $n\Delta$.

Thus from Step 1 and Step 2, the total optical cost of the proposed optical reversible ripple carry adder with input carry can be summed up as $3n + 1 + 3n = 6n + 1$, while the propagation delay of the proposed design can be summed up as $(2n + 1)\Delta + n\Delta = (3n + 1)\Delta$.

V. Comparison of n bit Optical Reversible Ripple Carry Adders

There are various existing non-optical reversible designs of n bit ripple carry adders in the literature such as the design in [22], [23], [24]. Thus, we are summarizing the optical cost and the delay of the various reversible gates used in the existing work in Table III. The optical cost and the delay summarized in Table III will be used for comparison of the proposed design of the optical reversible n bit adder with the existing non-optical reversible n bit adders. The Table IV illustrate the comparison of the proposed design with the existing designs proposed in [22], [23], [24] . The Table IV shows that the proposed optical design of the reversible n bit adder excels the existing non-optical reversible designs of n bit adder in terms of optical cost and delay and have zero overhead in terms of number of ancilla inputs and the garbage outputs. From Table V it can be seen that the proposed design of the optical reversible carry adder achieves the improvement ratios ranging from 12.50% to 24.91%, 63.97% to 66.65%, 60.80% to 66.63% and 66.67% to 68.41% compared to the designs presented in designs of [23], [22], [24] in terms of optical cost. From Table VI, it can be seen that the proposed design of optical reversible ripple carry adder achieves the improvement ratios ranging from 0.03% to 3.85%, 24.24% to 24.99%, 25.07% to 32.43% and 25.05% to 30.56% in terms of delay compared to the designs presented in [23], [22], [24], respectively.

TABLE III
Optical cost and delay of all optical implementation of reversible gates

	Optical Cost	Delay
Feynman Gate [4]	2	1Δ
Fredkin Gate	2	1Δ
Peres Gate [17]	4	2Δ
Toffoli Gate [4]	3	2Δ
TR Gate	4	2Δ

TABLE IV
A comparison of reversible ripple carry adder with input carry

	1	2	3	4	Proposed
Ancilla Inputs	0	0	0	0	0
Garbage Outputs	0	0	0	0	0
Optical Cost	8n-8	18n-8	18n-19	19n-5	6n+1
Delay Δ	3n+2	4n+1	4n+5	4n+4	3n+1
1 is the design in [23], 2 is the design 1 in [22] 3 is the design 2 in [22], 4 is the design 2 in [24]					

TABLE V
OPTICAL COST COMPARISON OF REVERSIBLE RIPPLE CARRY ADDERS (WITH INPUT CARRY)

Bits	1	2	3	4	5	% Imp. w.r.t 1	% Imp. w.r.t 2	% Imp. w.r.t 3	% Imp. w.r.t 4
8	56	136	125	147	49	12.50	63.97	60.80	66.67
16	120	280	269	299	97	19.17	65.36	63.94	67.56
32	248	568	557	603	193	22.18	66.02	65.35	67.99
64	504	1144	1133	1211	385	23.61	66.35	66.02	68.21
128	1016	2296	2285	2427	769	24.31	66.51	66.35	68.31
256	2040	4600	4589	4859	1537	24.66	66.59	66.51	68.37
512	4088	9208	9197	9723	3073	24.83	66.63	66.59	68.39
1024	8184	18424	18413	19451	6145	24.91	66.65	66.63	68.41
* 1 is the design in [23], * 2 is the design 1 in [22], * 3 is the design 2 in [22] * 4 is the design 2 in [24], * 5 is the proposed design									

TABLE VI
DELAY (IN Δ) COMPARISON OF REVERSIBLE RIPPLE CARRY ADDERS (WITH INPUT CARRY)

Bits	1	2	3	4	5	% Imp. w.r.t 1	% Imp. w.r.t 2	% Imp. w.r.t 3	% Imp. w.r.t 4
8	26	33	37	36	25	3.85	24.24	32.43	30.56
16	50	65	69	68	49	2.00	24.62	28.99	27.94
32	98	129	133	132	97	1.02	24.81	27.07	26.52
64	194	257	261	260	193	0.52	24.90	26.05	25.77
128	386	513	517	516	385	0.26	24.95	25.53	25.39
256	770	1025	1029	1028	769	0.13	24.98	25.27	25.19
512	1538	2049	2053	2052	1537	0.07	24.99	25.13	25.10
1024	3074	4097	4101	4100	3073	0.03	24.99	25.07	25.05
* 1 is the design in [23], * 2 is the design 1 in [22], * 3 is the design 2 in [22] * 4 is the design 2 in [24], * 5 is the proposed design									

VI. CONCLUSION

In this work we have presented a new design of optical reversible ripple carry adder using proposed optical reversible gate I and optical reversible gate II. The proposed design of all optical reversible ripple carry adder is primary optimized for the optical cost and the delay and has zero overhead in terms of number of ancilla inputs and garbage output compared to the existing counterparts. We conclude that the use of the proposed new optical reversible gates for the design of optical reversible ripple carry adder can be very much beneficial in minimizing the optical cost and the delay along with number of ancilla inputs and garbage output. The proposed optical reversible adder design is functionally verified at the logical level by creating a Verilog library of optical reversible gates using Verilog modules of Mach-Zehnder interferometer, beam combiner and beam splitter. The proposed efficient design of optical reversible ripple carry adder will find promising applications in optical reversible computing and could form key component of optical reversible digital processing circuits and architectures.

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