Impact of Resistive-Open Defects on the Heat Current of TAS-MRAM Architectures*

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Abstract—*Magnetic Random Access Memory (MRAM) is an emerging technology with the potential to become the universal on-chip memory. Among the existing MRAM technologies, the Thermally Assisted Switching (TAS) MRAM technology offers several advantages compared to the others technologies: selectivity, single magnetic field and integration density. As any other types of memory, TAS-MRAMs are prone to defects, so TAS-MRAM testing needs definitely to be investigated since only few papers can be found in the literature. In this paper we analyze the impact resistive-open defects on the heat current of a TAS-MRAM architecture. Electrical simulations were performed on a hypothetical 4×4 TAS-MRAM architecture enabling any read/write operations. Results show that W0 and/or W1 operations may be affected by the resistive-open defects. This study provides insights into the various types of TAS-MRAM defects and their behavior. As future work, we plan to utilize these analyses results to guide the test phase by providing effective test algorithm targeting fault related to actual defects that may affect TAS-MRAM architecture*

Keywords–non-volatile memories, spintronics, TAS-MRAM, heat current, resistive-open defects, fault modeling, test.

I. INTRODUCTION

Since the Giant Magneto-Resistance (GMR) effect discovery by A. Fert [1] and P. Grünberg [2], a special attention has been given to one of the most interesting and challenging branches in today's nanotechnology, called Spin Transport Electronics (Spintronics). This technology prompted scientific research and microelectronic industry to think about alternatives to replace especially non-volatile memories.

According to the 2010 International Technology Roadmap for Semiconductors (ITRS) [3], embedded memories occupy most of silicon area in typical System-on-Chip (SoC) implementations. Moreover, many applications require integrating non-volatile memories in a SoC. Although Flash memories are widely used today, they require high supply voltage and inherit reliability issues, which are difficult to mitigate. Magnetic Random Access Memory (MRAM) is an emerging technology with the potential to become the universal on-chip memory. MRAMs have high data processing speed, low power consumption and high integration density compared with Flash memories. In addition to non-volatility, these memories, when compared with Static RAMs (SRAMs), have fair processing speed and reasonable power consumption. Additionally, MRAMs are Complementary Metal Oxide Semiconductor (CMOS) process fabrication compatible [4].

As any other kind of memory, MRAMs are prone to defects and since only few papers can be found in literature, a thorough investigation followed by an in-depth analysis needs to be done in order to examine the reliability of MRAMs. In [5], authors presented the Write Disturbance Fault (WDF) model, a fault that affects data stored in the MRAM cells due to excessive magnetic field during write operation. In [6], two new faults were identified and are related to the magnetic junction behavior. Although their results are interesting, these papers deal with FIMS (Field Induced Magnetic Switching) MRAM technology.

The objective of this paper is to analyze resistive-open defects in Thermally Assisted Switching (TAS) MRAM. First, we define a hypothetical 4x4 TAS-MRAM architecture. It is composed of an array of magnetic junctions and a set of driver/decoder enabling any read/write operations. We have chosen to study here a write procedure inspired by the Flash program/erase scheme. Next, resistive-open defects were injected and analyzed on the proposed architecture. Among the six selected defect locations, only two that have highest significant impact on the heat current of the TAS-MRAM are analyzed in detail.

Electrical simulations performed in presence of the resistive-open defects show that the heat current of the TAS-MRAM is affected during the write operation. Depending on the defect size, W0 and/or W1 operations are affected. These operations become non-functional or destructive. Based on the SRAM literature, the fault models considered for resistive-open defects are TF0 (Transition Fault 1 to 0), TF1 (Transition Fault 0 to 1) and WD1 (Write Destructive Fault 1).

The rest of the paper is organized as follows. Section II provides the fundamentals and background on MRAM technologies. The proposed 4x4 TAS-MRAM architecture is described in Section III. The resistive-open defect analysis is provided in Section IV. Section V concludes the paper.

II. MRAM TECHNOLOGIES

MRAMs are Spintronic devices that store data in Magnetic Tunnel Junctions (MTJs). A basic MTJ device is usually composed of two ferromagnetic (FM) layers separated by an

* This work has been funded by the French national research agency under the framework of the ANR-10-SEGI-007 EMYR (Enhancement of MRAM Memory Yield and Reliability) project.

978-3-9810801-8-6/DATE12/©2012 EDAA

insulating layer, as shown in Figure 1. One of the FM layers is pinned and acts as a reference layer. The other one is free and can be switched between, at least, two stable states. These states are parallel or anti-parallel with respect to the reference layer. When it is in the parallel state, the MTJ offers the minimum resistance (Rmin) while the maximum resistance (Rmax) is obtained when anti-parallel. The difference between Rmin and Rmax quantified by the Tunnel Magneto Resistance (TMR), is high enough to be sensed during the read operation.

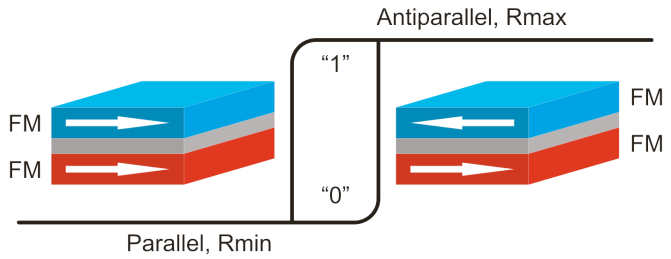

Figure 1. MTJ in parallel and antiparallel states

Read operation consists in determining the MTJ's magnetization state and can be performed by voltage or current sensing across the MTJ stack. A CMOS sense amplifier can be used to obtain the stored bit information. High TMR allows simple and stable sense amplifiers, improving reading accuracy [7].

Write operation can be performed using magnetic fields or spin polarized current and depends on MRAM technologies: FIMS (Field Induced Magnetic Switching), Toggle Switching, TAS (Thermally Assisted Switching) and CIMS (Current Induced Magnetic Switching) are detailed in the following sub-sections.

A. Field Induced Magnetic Switching (FIMS) MRAMs

The first MRAM generation relies on the Stoner-Wohlfarth theory of coherent rotation in single domain particles [8]. In this approach, the energy required to reverse the magnetization is minimized by applying simultaneously two perpendicular magnetic fields. The field necessary to switch is mainly determined by shape anisotropy and edge roughness. However, a small deviation of these characteristics has a huge influence in the switching field distribution in large bit arrays. Another issue is the thermal activation of half-selected MTJs, which increases addressing errors. The MTJ is fully selected when two magnetic fields are applied to it. The ability to write a fully-selected MTJ without disturbing half-selected MTJs is called write margin. Finding a set of fields, which can be used to program all cells, becomes difficult due to the very narrow write margin in this technology [9].

B. Toggle MRAMs

A new approach called Toggle Switching was proposed by Savtchenko [10] to overcome the selectivity issue of FIMS technology. The FM layers were replaced by synthetic layers and two perpendicular current lines generating magnetic fields are oriented at 45 degrees from the two magnetization stable states. To toggle the magnetization state, two magnetic pulses are applied in four steps:

1. Switch on bit-line field.
2. Switch on word-line field.
3. Switch off bit-line field.
4. Switch off word-line field.

When the field is removed the synthetic storage layer will be reversed. A prior read is mandatory as it is only possible to toggle the state. This drawback is compensated by the advantage of using a single current polarity to create the magnetic fields.

C. Thermally Assisted Switching™ (TAS) MRAMs

Thermally Assisted Switching™ is an alternative switching method for MRAMs. In the scheme proposed by Spintec [11] and industrialized by Crocus Technology, the MTJ is modified by inserting an anti-ferromagnetic layer (AFM) that pins the storage layer while below its blocking temperature (BT). BT is the threshold temperature above which it is possible to change the magnetization state of the free layer. When MTJ's temperature rises above BT, the storage layer is freed and can be reversed under the application of a small magnetic field provided by a single field-line. The magnetic field is maintained beyond the heating voltage pulse to ensure the correct pinning of the storage layer.

TAS approach offers several advantages. The selectivity problem is reduced since only heated MTJs are able to switch and all other MTJs remain in their stable state as they remain below their blocking temperature. Although TAS needs an additional heating current, this current is much smaller than the current used to generate the second magnetic field in FIMS-MRAM. The integration density is improved due to thermal stability and the need of only one field-line. Finally, as the free layer can be pinned to any stable state, multi level logic can be achieved [12]. TAS is for the moment the most promising MRAM solution as it mitigates most drawbacks from its predecessors and offers scalability down to the 65nm technology node and below.

D. Current Induced Magnetic Switching (CIMS) MRAMs

CIMS is the most recent MRAM technology. The writing is accomplished by injecting a spin-polarized high current density through MTJ without the assistance of any external magnetic field [13]. This approach relies on Spin Transfer Torque (STT) effect. STT phenomenon is the exchange of spin angular momentum between an incoming spin-polarized current and the local magnetization. This effect applied to MRAMs could restore the scalability beyond several Gbit/chip. However, there are some problems to solve in this recent technology. Lowering the write current density while maintaining data stability and improving the read signal are the main concerns of spin induced reversal mechanism. This raises considerable challenges since the MRAM cells must be able to withstand high current densities without exceeding the MTJ's breakdown voltage. Moreover, the transistor's size is related to the writing current, which sets a limit on the memory density.

III. THE 4X4 TAS-MRAM ARCHITECTURE

Figure 2 shows the TAS-MRAM architecture we have chosen for our study. The organization is done in a square matrix that has 2^{MR} rows and 2^{NC} columns, for a total storage

capacity of 2^{MR+NC} bits, where MR and NC are the numbers of bits used to specify the row and column address, respectively. In our case study, MR and NC are 2; hence, the storage capacity is 16 bits. Each cell in the array is connected to one of the row-lines, called word-lines, and connected to one of the column-lines, called bit-lines or digit-lines. A particular MTJ can be accessed for a read or write operation by selecting its word-line and bit-line.

During a read operation, the read driver applies a small voltage that generates negligible heat to both the selected MTJ and a reference MTJ. The reference MTJ is halfway between the high and low resistance values. The resistance difference is then sensed to determine the stored data in the selected MTJ.

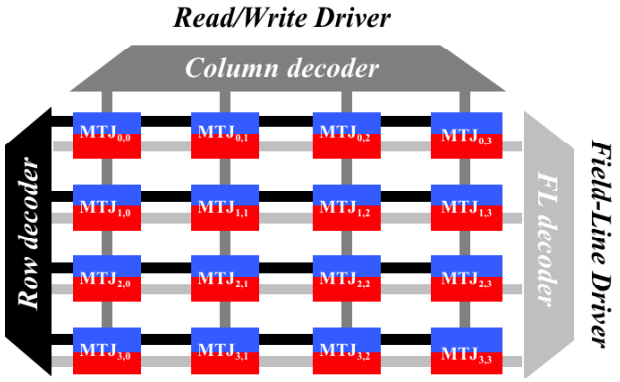

Figure 2. TAS-MRAM architecture

During a write operation, initially the write driver applies a voltage to heat the selected MTJ above its BT. Next, the field-line driver applies a current to generate the data zero magnetic field. While the MTJ is cooled down below BT, the magnetic field is maintained. At this point, the field-line driver inverses the current direction. The MTJ is heated again to perform the write 1 operation, if needed. When the MTJ reaches room temperature, the writing procedure is accomplished. This approach allows writing a 0 and 1 in one cycle to different MTJs sharing the same field-line. Note that, a write 1 operation (denoted W1) consists of applying first a write 0 and then a write 1 operation. Conversely, a write 0 operation (denoted W0) consists of applying only a write 0 operation. These write procedures are inspired by the Flash programming procedures where a write operation (write 1) is always preceded by and erase operation (write 0).

Electrical simulations were performed using the TAS-MTJ model from Spintec [11]. This model is compiled in C language and is compatible with the Spectre simulator of the standard Cadence design suite [14].

Table I summarizes field-line currents applied and MTJ's simulated characteristics for all read and write operation polarities (R0, R1, W0 and W1).

During read operations the two resistive states of the MTJ are 2.6kΩ for Rmin and 5.9kΩ for Rmax. These two resistance values are correctly sensed by the sense amplifier that provides data 0 and data 1, respectively. During write operations, the current is enough to heat the MTJ above its blocking temperature, *i.e.* 215°C and 201°C for the W0 and W1, respectively.

TABLE I. MTJ'S FAULT-FREE OPERATING CONDITIONS

			R0	*R1*	*W0*	*W1*
	Field-line	mA	0	0	+16	+16/-16
MTJ	**Current**	uA	44	42	294	305
	Voltage	mV	115	249	849	798
	Resistivity	kΩ	2.6	5.9	-	-
	Logic Value		0	1	-	-
	Temperature	°C	32	38	215	215/201

16 bits TAS-MRAM fault-free temperature profiles for W1 and W0 operations are shown in Figure 3 and Figure 4, respectively. Note that MTJs are written row by row starting from $MTJ_{0,0}$ to $MTJ_{3,3}$. We observe that the temperature rises twice during each write cycle in W1 operations, while during W0 operations, the temperature rises only once per cycle, following the writing approach described previously.

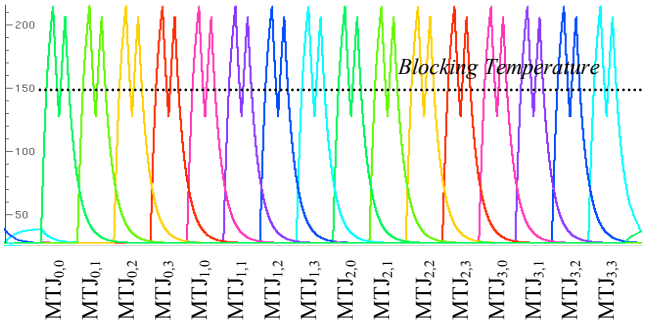

Figure 3. W1 fault-free temperature profiles

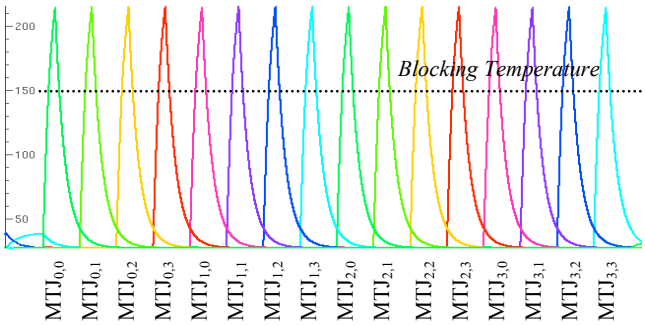

Figure 4. W0 fault-free temperature profiles

IV. RESISTIVE-OPEN DEFECT ANALYSIS

Interconnect imperfections have become an issue in deep sub-micron technologies. Opens are the major type of defects, as reported in [15]. A resistive-open defect happens when there is a resistive interconnection between two circuit nodes. In defect-free operation, these two nodes should be entirely connected. These resistive-open defects can cause hard failures for huge resistance values, and increase the circuit delay introducing timing defects for small resistance values.

The defect injection in the TAS-MRAM is depicted in Figure 5. Resistive-open defects are placed on interconnects of the memory array as follows:

- Df1: global defect affecting the bit-line heat current.
  Df1': semi-global distributed defect along the bit-line.
- Df2: local defect affecting a single MTJ heat current.
- Df3: global defect affecting the (column) bit-line selection transistor.
- Df4: global defect affecting the (row) word-line.
  Df4': semi-global distributed defect along the word-line.
- Df5: local defect affecting a single MTJ selection transistor.
- Df6: global defect affecting the field-line current

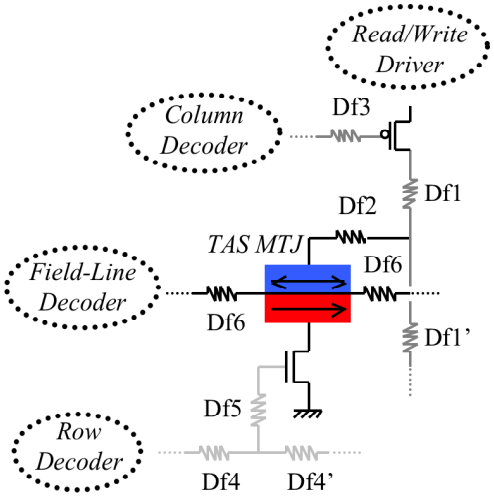

Figure 5. Resistive-open defect injection

These six defects can impact the TAS-MRAM behavior in different ways. In the following sub-sections, we analyze in detail the two defects (Df1 and Df2) that impact directly the MTJ's heat current. The other defects are out of the scope of this study and will be investigated in future analyses.

A. *Df1 analysis*

Table II summarizes field-line currents applied and MTJ's simulated characteristics of $MTJ_{1,1}$ under 5kΩ Df1 resistive-open defect. Simulations were performed using the following sequences:

- *0W1*: a W1 operation is performed on $MTJ_{1,1}$ that initially contains a 0. This sequence corresponds to a rising transition.
- *1W1*: a W1 operation is performed on $MTJ_{1,1}$ that initially contains a 1. This sequence allows verifying the W1 operation since it is composed of write 0 and write 1 successive operations as described earlier.
- *1W0*: a W0 operation is performed on $MTJ_{1,1}$ that initially contains a 1. This sequence corresponds to a falling transition.

Note that the *0W0* sequence is not considered since no transition occurs. Moreover, a read operation is preformed before and after any write operations.

Results are shown in Table II. We notice that the current passing through the magnetic junction was not high enough to heat the selected MTJ above its blocking temperature (150°C). Consequently, W1 and W0 operations were not performed. As a result, $MTJ_{1,1}$ keeps its initial magnetization state during all simulations.

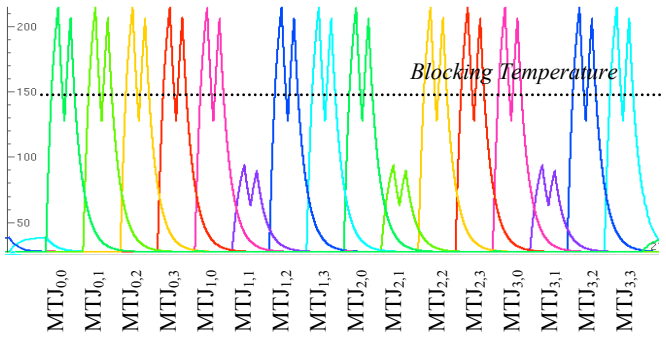

Figure 6. W1 temperature profile under resistive-open defect Df1'

TABLE II. $MTJ_{1,1}$ CHARACTERISTICS UNDER DF1

			0W1			*1W1*			*1W0*		
			R0	***W1***	***R1***	***R1***	***W1***	***R1***	***R1***	***W0***	***R0***
Df1	**Field-line**	mA	0	+16/-16	0	0	+16/-16	0	0	+16	0
5k Ω	**$MTJ_{1,1}$ Current**	uA	40	183	40	38	162	38	38	162	38
	$MTJ_{1,1}$ Voltage	mV	107	471	107	235	671	235	235	676	235
	$MTJ_{1,1}$ Resistivity	kΩ	2.6	-	2.6	6	-	6	6	-	6
	$MTJ_{1,1}$ Logic Value		0	-	0	1	-	1	1		1
	$MTJ_{1,1}$ Temperature	°C	31	95/89	31	36	111/106	36	36	111	36

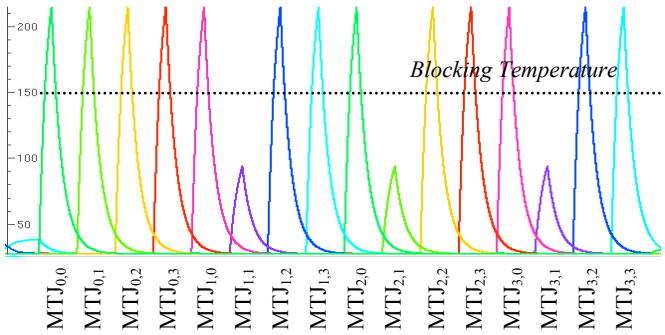

Figure 7. W0 temperature profile under resistive-open defect Df1'

Since Df1 is a global defect, it affects all MTJs that share the same bit-line. In Figures 6 and 7, the temperature profiles of the 16 bits TAS-MRAM under resistive-open defect Df1' are depicted for W1 and W0 operations respectively. Df1' was placed on the second bit-line after the first MTJ. Consequently, it may affect only three MTJs and not all MTJs of the bit-line as for Df1.

As previously mentioned, MTJs are written row by row starting from $MTJ_{0,0}$ to $MTJ_{3,3}$. In Figures 6 and 7, we can see that three MTJs were affected by Df1': $MTJ_{1,1}$, $MTJ_{2,1}$ and $MTJ_{3,1}$. These results confirm the impact of Df1' on MTJs of the second bit-line of the TAS-MRAM array.

B. *Df2 analysis*

Df2 is a local resistive-open defect that may impact only one MTJ heat current. Previously, we described the global behavior of Df1, while in this sub-section, we provide a more detailed analysis considering different Df2 sizes.

Table III summarizes field-line currents applied and MTJ's simulated characteristics of $MTJ_{1,1}$ under four Df2 resistive-open defect sizes i.e. 0.9kΩ, 1.2kΩ, 2.0kΩ and 2.4kΩ. Simulations were performed using *0W1*, *1W1* and *1W0* sequences.

For Df2=0.9kΩ, write operations were performed correctly and $MTJ_{1,1}$ exhibits correct logic levels during read operations.

With a higher defect value, faulty operations start to appear. For Df2=1.2kΩ, the *0W1* sequence is corrupted and the read operation returns a wrong value. In that case, the current passing through the magnetic junction was enough to heat $MTJ_{1,1}$ above its blocking temperature (150°C) but during a time too short to switch the magnetization state. $MTJ_{1,1}$ remains at 0 after the W1 operation.

For Df2=2.0kΩ, the observed faulty behavior is more complex. As described before, the W1 operation in the *0W1* sequence does not work anymore. In addition, the W1 operation in the *1W1* sequence becomes destructive and the following read operation returns a 0. In that case, only write 0 operation included in any W1 operation works correctly. Consequently, $MTJ_{1,1}$ undergoes a non desired W0 operation.

Finally, for Df2=2.4kΩ, W0 and W1 were not performed. As for Df1 analysis, $MTJ_{1,1}$ keeps its initial magnetization during all simulations.

C. *Fault modeling*

Based on previous simulations, here we provide a set of fault models associated with the observed faulty behaviors. Df1 and Df2 involve the same set of faults. Only the location of the affected MTJs differs: all MTJs of the affected bit-line for Df1 (or remaining ones for Df1') and only one MTJ in the case of Df2.

For each corrupted sequences (*0W1*, *1W1* and *1W0*), we associate a FFM (Functional Fault Model) with respect to the SRAM literature [16]. Based on previous simulations, the following sequences were corrupted depending on the defect size:

- *0W1* where the W1 operation does not work: The affected MTJ cannot undergo a rising transition. The related fault model is a TF1 (Transition Fault 0 to 1).
- *1W1* where the W1 operation is destructive: The affected MTJ loses its data when a W1 is performed. The related fault model is a WD1 (Write Destructive Fault 1).
- *1W0* where the W0 operation does not work: The affected MTJ cannot undergo a falling transition. The related fault model is a TF0 (Transition Fault 1 to 0).

Figure 8 shows the distribution of fault models with respect to the defect size. Three defective regions appear: 1) MTJ is affected by a TF1, 2) MTJ is affected by a TF1 and WD1 and 3) MTJ is affect by both TF0 and TF1, meaning that it remains at its initial state.

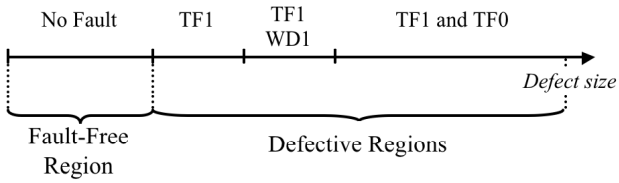

Figure 8. Fault modeling function of the defect size

V. CONCLUSION

In this paper, we have analyzed the impact of resistive-open defects on the heat current of TAS-MRAM architecture. Initially, we develop a hypothetical 4x4 TAS-MRAM architecture to perform electrical simulations. This architecture is made of drivers/decoders/MTJs and it allows simulating any read/write operations.

Electrical simulations performed in presence of the resistive-open defects show that W0 and/or W1 operations are affected. These write operations become non-functional or destructive. Based on the SRAM literature, the applied fault models are TF0 (Transition Fault 1 to 0), TF1 (Transition Fault 0 to 1) and WD1 (Write Destructive Fault 1).

This study provides insights into the various types of MRAM defects and their behavior. As future work, we plan to use these analyses results to guide the test phase by providing effective test algorithm targeting fault related to actual defects that may affect TAS-MRAM architecture.

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TABLE III. $MTJ_{1,1}$ CHARACTERISTICS UNDER DF2

			0W1			***1W1***			***1W0***		
			R0	***W1***	***R1***	***R1***	***W1***	***R1***	***R1***	***W0***	***R0***
Df2	**Field-line**	mA	0	+16/-16	0	0	+16/-16	0	0	+16	0
0.9k Ω	**$MTJ_{1,1}$ Current**	uA	43	277	41	41	269	41	41	256	43
	$MTJ_{1,1}$ Voltage	mV	114	682	245	246	729	246	246	804	114
	$MTJ_{1,1}$ Resistivity	kΩ	2.6	-	5.9	6	-	6	6	-	2.6
	$MTJ_{1,1}$ Logic Value		0	-	1	1	-	1	1	-	0
	$MTJ_{1,1}$ Temperature	°C	32	174/163	37	37	181/170	37	37	181	32
1.2k Ω	**$MTJ_{1,1}$ Current**	uA	42	267	42	40	262	40	40	245	42
	$MTJ_{1,1}$ Voltage	mV	113	661	113	246	689	244	246	794	113
	$MTJ_{1,1}$ Resistivity	kΩ	2.6	-	2.6	6	-	5.9	6	-	2.6
	$MTJ_{1,1}$ Logic Value		0	-	0	1	-	1	1	-	0
	$MTJ_{1,1}$ Temperature	°C	32	169/154	32	37	173/159	37	37	173	32
2k Ω	**$MTJ_{1,1}$ Current**	uA	40	243	42	40	241	42	40	218	42
	$MTJ_{1,1}$ Voltage	mV	112	610	112	243	623	112	243	776	112
	$MTJ_{1,1}$ Resistivity	kΩ	2.6	-	2.6	6	-	2.6	6	-	2.6
	$MTJ_{1,1}$ Logic Value		0	-	0	1	-	0	1	-	0
	$MTJ_{1,1}$ Temperature	°C	32	148/134	32	37	155/139	32	37	155	32
2.4k Ω	**$MTJ_{1,1}$ Current**	uA	42	233	42	40	208	40	40	207	40
	$MTJ_{1,1}$ Voltage	mV	11	587	111	242	760	242	242	773	242
	$MTJ_{1,1}$ Resistivity	kΩ	2.6	-	2.6	6	-	6	6	-	6
	$MTJ_{1,1}$ Logic Value		0	-	0	1	-	1	1	-	1
	$MTJ_{1,1}$ Temperature	°C	32	133/125	32	37	149/141	37	37	149	37