# A Multi-Parameter Bio-Electric ASIC Sensor with Integrated 2-Wire Data Transmission Protocol for Wearable Healthcare System

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***Abstract*— This paper presents a fully integrated application specific integrated circuit (ASIC) sensor for the recording of multiple bio-electric signals. It consists of an analog front-end circuit with tunable bandwidth and programmable gain, a 6-input 8-bit successive approximation register analog to digital converter (SAR ADC), and a reconfigurable digital core. The ASIC is fabricated in a 0.18-µm 1P6M CMOS technology, occupies an area of 1.5 × 3.0 mm$^2$, and totally consumes a current of 16.7 µA from a 1.2 V supply. Incorporated with the ASIC, an Intelligent Electrode can be dynamically configured for on-site measurement of different bio-signals. A 2-wire data transmission protocol is also integrated on chip. It enables the serial connection over a group of Intelligent Electrodes, thus minimizes the number of connecting cables. A wearable healthcare system is built upon a printed Active Cable and a scalable number of Intelligent Electrodes. The system allows synchronous processing of maximum 14-channel bio-signals. The ASIC performance has been successfully verified in *in-vivo* bio-electric recording experiments.**

***Keywords- Bio-electric ASIC; multi-parameter biosensor; Intelligent Electrode; Active Cable; wearable healthcare system***

## I. INTRODUCTION

With the development of the biomedical technology and low-power electronics, it is possible to realize a bio-electric signal read-out, process and transmission system on a single chip. In recent years, bio-signal acquisition using a fully integrated design has become an important feature of advanced medical applications. The system in [1] sequentially detects 64-channel electroencephalogram (EEG) signals using time-division-multiplexing (TDM) method. A power efficient analog signal processor application specific integrated circuit (ASIC) for bio-potential signal monitoring is developed in [2]. Ref. [3] demonstrates a micro-power neural recording amplifier with improved noise efficiency factor. At the mean time, the advantages of synchronous and simultaneous measurement of multiple bio-signals have been demonstrated to bring additional value to improve the diagnostics accuracy. For example, to characterize the epilepsy seizure stages or detect epileptic events, the information of simultaneously recorded EEG and electrocardiogram (ECG) is required [4]. Similarly, to evaluate the athletes' performance, a routine

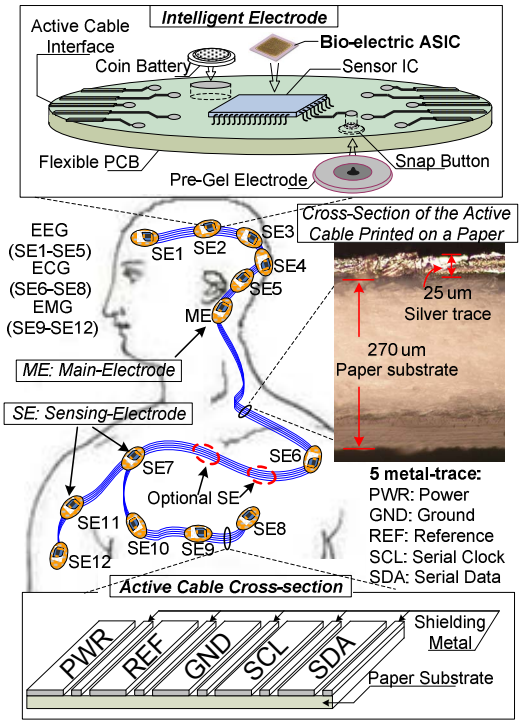


Fig. 1. A wearable healthcare system based on scalable Intelligent Electrodes and an Active Cable.

electromyogram (EMG) signal to monitor the athletes' muscle status is not sufficient; a concurrent ECG signal is necessary to provide complementary physical information. However, the equipments currently available to the medical community are commonly limited to detecting only one type of bio-signal per device, and are difficult to be synchronized. A desirable biosensor for the medical community should be a multi-parameter bio-electric sensor which can provide synchronous extraction of multiple bio-signals.

In this paper, we present a compact, programmable bio-electric ASIC sensor. The ASIC is composed of three key parts: 1) a gain and bandwidth programmable front-end, 2) a 6-input 8-bit successive approximation register analog to

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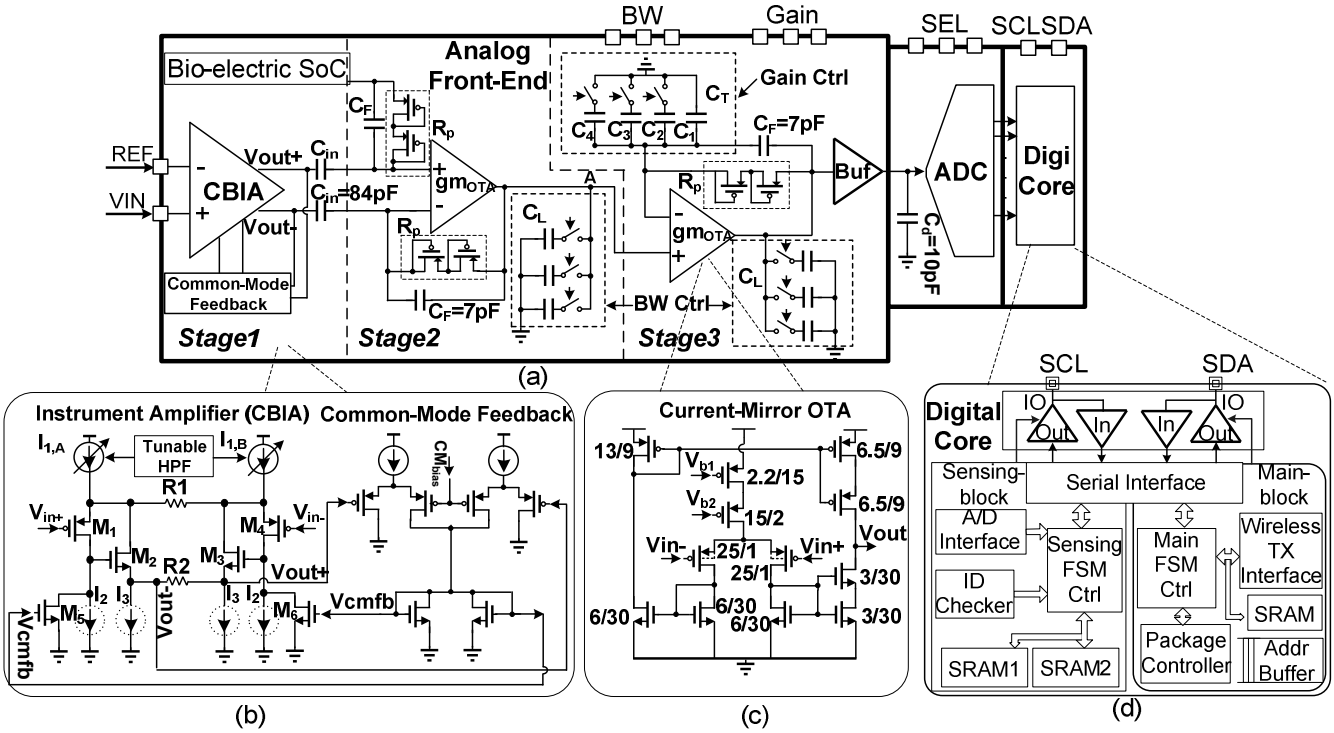



Fig. 2. Overall architecture of the bio-electric ASIC and detail schematic for the building blocks.

digital converter (SAR ADC), and 3) a reconfigurable digital core. The front-end circuit with gain and bandwidth adjustment is quite useful in multi-parameter recording systems, which enables the ASIC to process a variety of bio-potential signals, including EMG, ECG, and EEG. The amplified bio-signal is converted to a digital format by the on-chip ADC, and stored by the digital core in an on-chip RAM.

The concept of the proposed Intelligent Electrode is illustrated at the top Fig.1, it is built on a flexible PCB and composed of a bio-electric ASIC, a coin battery, and a snap button for conductive electrode. Each Intelligent Electrode has two operation modes: it can be configured either as a Main-Electrode (ME) or a Sensing-Electrode (SE). The ME takes charge of the whole system, while the SE performs bio-electric signal acquisition task. Different from the traditional acquisition approach (centralized bio-signal processing in a medical device), the proposed Intelligent Electrode allows biological sensing and processing distributed on-site each electrode. In addition, a two-wire bi-direction serial transmission protocol is on chip implemented which provides communication link between different Intelligent Electrodes, thus enables the setup of a scalable body area network. The communication between the ME and SEs is command based. By using broadcast command, the ME can set the SEs to low power sleep mode. Also, via broadcast command, the ME can trigger all of the SEs to startup their acquisition circuit simultaneously for bio-signal sensing. In this way, synchronous measurement of multiple bio-potential signals can be achieved. An Active Cable is also proposed in this paper, shown at the bottom of Fig.1. It is composed of five silver traces printed on a flexible photo paper substrate. Instead of the full cable connection used in traditional approaches, in this work, one single Active Cable is applied to connect all Intelligent Electrodes together, and thus relaxes the cable tangling problem and improves users' comfort. Each ASIC corresponds to one bio-electric channel, depending on the application requirement, up to 14 ASIC can be applied to synchronously detect a user's bio-signals.

## II. Active Cable and Intelligent Electrode Placement

The concept of printed flexible Active Cable was firstly presented in [5]. The cable is fabricated by inkjet printing of nano-silver ink on a photo paper substrate. It is composed of five silver traces (PWR, GND, REF, SCL and SDA) with the trace width of 1 mm and clearance of 0.5 mm. It serves two purposes: 1) to share the power (PWR), ground (GND) and reference signal (REF), 2) to establish a wired network via a serial bus (SCL and SDA).

The electrical characterization (both in frequency domain and time domain) of the printed Active Cable is measured and reported in [6]. The experimental results show that the digitized bio-potential signal can be successfully transmitted through the printed Active Cable with a date rate of 150 Kbits/s. The cross-section view of the cable is shown in Fig.1, where the paper thickness and metal thickness are 270 μm and 25 μm respectively, resulting in a conductivity of 12.8 m/(Ω •mm$^2$).

Different from the traditional connecting approach (multiple lead wires connected to a central device), one single Active Cable is applied to serially connect each Intelligent Electrode, thus relaxes the problems of cable tangling and cable noise. Comparing with a full cable solution, this serial connection method drastically reduces the amount of connecting cables, thus free the user form the cable

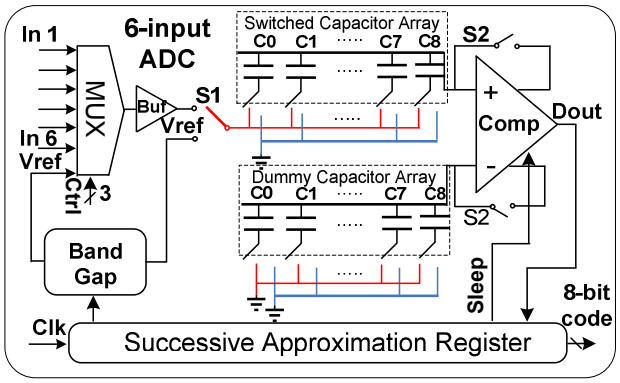



Fig. 3. Architecture of the 6-input 8-bit SAR ADC.

confinement and maximize the user's comfort. In addition, the inkjet printing technology makes the Active Cable low cost and disposable after use, hence partially solves problems such as environmental load issues, as well as potential infections and hygienic issues.

For the Intelligent Electrodes placement on a subject's skin, the ME is located behind one ear, and its local voltage is used as the global reference (the REF signal in Active Cable). This is a typical reference position in EEG experiments since little EEG signal can be detected there. The SEs are placed on specific examined body areas. For example, the SEs placed on a subject's forehead are used to detect EEG signal, SEs on the chest are for ECG signals, and SEs on the arm are for EMG monitoring. One recording channel is formed by detecting the voltage difference between the REF (from the ME) and a local voltage (from a SE). So each SE corresponds to one recording channel. Since the number of SEs in the network is scalable, the ME is required to make a dynamic network control in cases of new SEs joining in or the existing SEs moving out from the network. The detailed network management will be described in section III.

## III. ASIC DESIGN

### A. Programmable Analog Front-End

The architecture of the ASIC is illustrated in Fig.2. A key part of the ASIC is the analog front-end, which defines the quality of the detected bio-signal. To enable multiple applications, the front-end is designed for a wide range of electrode potentials (from tens of μV to several mV) and a variety of 3-dB frequency span (from sub 100 Hz to 1.5k Hz). The analog front-end can be split into three stages. Fig.2a illustrates the block diagram of the programmable analog front-end. Stage1 is mainly composed of a current balanced instrument amplifier (CBIA) [7] and a common mode feed back (CMFB) circuit. For the bio-electric signal sensing, a common reference signal REF is connected to the inverting input of the CBIA, and a local electrode is connected to the non-inverting input (one channel per AISC). In order to have a large input impedance, PMOS input pair is employed in CBIA. The flicker noise is suppressed by choosing large gate area for the input transistors. CMFB is accomplished by sensing the common-mode level of the two outputs available at the terminals of resistor $R_2$, comparing with a reference $CM_{bias}$, and returning the feedback to CBIA. Due to the fully differential architecture, the CBIA is able to effectively cancel the common-mode interference. The current balancing feature keeps Vds of $M_2$ and $M_3$ constant, thus DC offset at the input ports is also well suppressed. Fig.2b shows the detail schematic of the CBIA and CMFB circuit. The differential gain of Stage1 is defined by the ratio of resistor $R_2$ (300 kΩ) and $R_1$ (40 kΩ). The differential outputs of Stage1 are coupled to Stage2 through capacitor $C_{in}$. The transfer function of Stage2 can be written as

$$A_{Stage2} = Z_f \Big/ \left( Z_{in} + \frac{Z_{in} + Z_L + Z_f}{gm_{OTA} Z_L} \right) \approx \frac{Z_F}{Z_{in}} \approx \frac{C_{in}}{C_F} \quad (1)$$

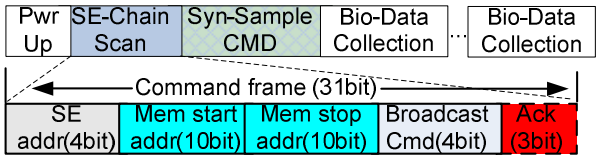
where $Z_f = R_p \,//\, (1/sC_F)$, $Z_{in} = (1/sC_{in})$. $Z_L$ is the equivalent impedance of the variable load capacitor $C_L$ (with a value ranging 16.5~66 pF) in parallel with any parasitic resistance between node A and ground; $gm_{OTA}$ is the transconductance of the operational transconductance amplifier (OTA) [8, 9], with a value of 0.55 μS. The schematic of the current-mirror OTA is illustrated in Fig.2c. As $Z_f$ is much larger than $Z_{in}$ and $Z_L$, the close-loop gain of Stage2 can be approximately set to 12.5 V/V, the ratio of the input capacitor $C_{in}$ and the feedback capacitor $C_F$. Stage3 offers a digitally controlled gain by adjusting the equivalent capacitance ($C_T$) of a switched capacitor bank ($C_1$, $C_2$, $C_3$ and $C_4$). If a capacitor is connected to ground, its value is counted into $C_T$; otherwise it is canceled. The transfer function of Stage3 can be expressed as

$$\begin{aligned} A_{Stage3} &= \left(1 + \frac{Z_f}{Z_T}\right) \Big/ \left(1 + \frac{Z_T + Z_L + Z_f}{(gm_{OTA} Z_L)(Z_T)}\right) \\ &\approx \left(1 + \frac{C_T}{C_F}\right) \Big/ \left(1 + s\left(\frac{C_T C_L}{gm_{OTA} C_F}\right)\right) \end{aligned} \quad (2)$$

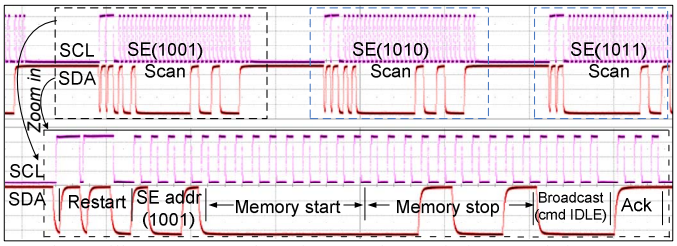
where $Z_T = (1/sC_T)$, $Z_f = R_p \,//\, (1/sC_F)$. Since $Z_f$ is much larger than $Z_T$ and $Z_L$, the transfer function of Stage3 can be approximated as (2). By tuning the value of $C_T$ via three external switches, the in-band gain of the Stage3 can be set to eight different values ranging from 2 V/V to 19 V/V. From the gain equations, it can be calculated that in theory the three-stage analog front-end can provide a set of close-loop gains ranging from 45 dB to 64 dB. In addition, for a selected gain, for instance gain=49 dB, the high cut-off frequency can be adjusted to 80 Hz, 260 Hz, 400 Hz or 1.5 KHz by varying the load capacitance $C_L$ through the external bandwidth switches. The low cut-off frequency is set to 0.3 Hz. Since a sampling ADC is connected in the following stage, a unit buffer is employed at the output of front-end to enhance the current driving capability. The analog front-end (including the unit buffer) totally draws a current of 2.3 μA from a 1.2 V supply.

### B. 6-input 8-bit SAR ADC

A standard 8-bit charge-redistribution SAR ADC with 6-input channels is implemented in a fully differential architecture, as shown in Fig.3. A MUX is used to select one from six inputs to connect the capacitive binary search array for A/D conversion. In this design, the input5 is reserved for the amplified bio-signal from the front-end; the other five




(a) Command frame for SE-Chain Scan process.




(b) Oscilloscope screenshot of SCL and SDA during SE-Chain Scan.

Fig. 4. Command-based SE-Chain Scan.

inputs are available for other biological sensing, such as blood pressure and body temperature *et al*. The capacitive binary search array is composed of 256 digitally controlled unit-capacitors, with a unit capacitance of 124 fF each (the minimal mini-cap capacitor for UMC 180 nm technology), resulting in a total capacitance of 31.7 pF. The upper common plate of the switched capacitor array is connected to one terminal of the comparator. In order to cancel the charge injection errors induced by CMOS switches and achieve a high linearity, an identical dummy capacitor array is used to connect the other terminal of the comparator. A bandgap module is designed to generate a reference voltage of 800 mV. Since the system is battery-operated, the reference signal is required to keep stable in case of supply voltage drop when the battery is low. An experiment is taken to test the stability of the reference signal by tuning down the supply voltage from 1.8 V to some extent. Measurement results show that the reference can keep stable at 800 mV even when the supply is tuned to 1.2 V. Although the measurement results show the ADC can work at a maximum conversion rate of 100 KS/s, in this system it operates at a sample rate of 3.3 KS/s with an external clock of 100 KHz. Like the analog front-end, the ADC operates at 1.2 V supply and consumes 1.8 µA.

### C. *Reconfigurable Digital Core and Network Management*

A low-power digital core (the first tapeout was reported in [10]) with 2-wire serial transmission protocol is on-chip implemented, which enables the establishment of a body-area network of a group of Intelligent Electrodes. The architecture of the digital core is illustrated in Fig.2d. The on-chip SPRAM enables the Intelligent Electrode to buffer the digitized bio-signal. Since the digital core has a reconfigurable architecture, the operating mode of each Intelligent Electrode can be dynamically set via an external pin 'Mode'. If the pin is set to logic '1', the Intelligent Electrode is configured as a ME; otherwise it is configured as a SE. The digital core also includes a disable feature that can turn off certain circuit modules which are not needed at a particular operating mode to minimize power consumption. For instance, the front-end and the SAR ADC of a ME are turned off for power-saving. For each operating mode, the functionality differs in:

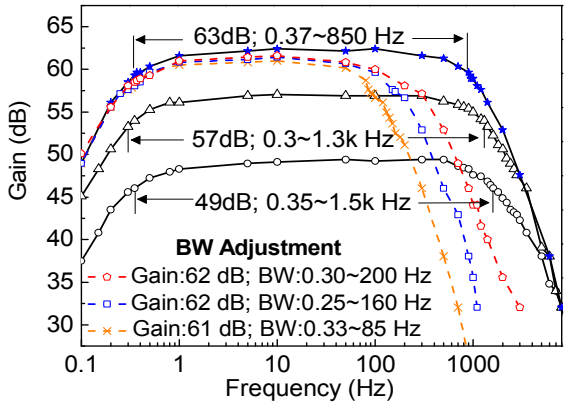



Fig. 5. Gain and bandwidth measurement of the analog front-end.

*1) SE mode:* The bio-potential signal is detected and amplified by the analog front-end in a SE. The outptut is converted to a digital format by its on-chip ADC. The logic controller of the SE picks up the digitized bio-signal from its A/D interface and saves the data temporarily in an on-chip SPRAM until these data are periodically collected by a ME. If one SPRAM is full, the coming data will be automatically switched to the second on-chip SPRAM.

*2) ME mode:* When the system is powered up or reset, the ME initiates a command-based SE-Chain Scan (SECS) process. Fig.4a shows the structure of the command frame. During SECS process, all active SEs in the serial chain are scanned. Address information of each active SE is recorded in an on-chip buffer. Fig.4b illustrates the SCL and SDA waveforms captured on an oscilloscope during SECS, where the scan of SE with address of '1001' is enlarged for illustration. The SECS process is accomplished within 6 ms. Once SECS is completed, a synchronous sampling command 'Syn-Sample' is broadcast by the ME which triggers the ADC in each SE to startup simultaneously. In this way, synchronous recording of multiple bio-signals can be achieved.

For the case of a new SE joining in or an existing SE moving out, the ME initiates a quick SECS on a periodic basis of every 5-second to update the address information in the buffer. If a new SE is detected, the 'Syn-Sample' command will be resent to resynchronize the ADC in each SE. The bio-signal data stored in each SE are collected by the ME through the Active Cable every 0.1 second with a data rate of 120 Kbits/s. Collected data are saved temporarily in a ME's on-chip SPRAM. When the storage is full, the ME forwards the stored data to an external wireless transmit module. The average current consumed by the digital core is 12.6 µA for a SE and 12.7 µA for the ME from a 1.2 V supply with a 1 MHz system clock.

## IV. Experimental Results and In-vivo Tests

Fig.5 plots the gain and bandwidth measurement result of the analog front-end which is in agreement with the results calculated from equation (1) and (2). The measured largest gain (63 dB) is slightly smaller than the simulation result (64 dB) which may due to the slight attenuation of unit buffer at

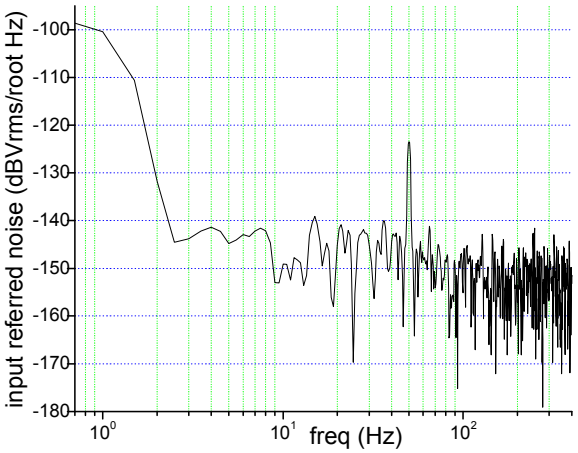



Fig. 6. Input-referred noise of the analog front-end.

the front-end output port. The gain or bandwidth can be independently adjusted via external pins. Totally eight different gain, ranging from 45 dB to 63 dB can be achieved (three of them chosen for illustration) to accommodate different bio-electric signals. For each selected gain, four user-programmable 3-dB bandwidths can be achieved using bandwidth switches. The upper part of Fig.5 shows the case of 3-dB bandwidth adjustment with an almost consistent gain. The measured low cut-off frequency is around 0.3 Hz.

### *A. Noise and CMRR Performance*

The circuit noise is measured by using HP dynamic signal analyzer 35670A connected to the buffer output. Low frequency noise of the front-end circuit is dominated by flicker noise. PMOS input pair is adopted in this design since it exhibits less flicker noise than NMOS transistors [11]. Moreover, by choosing large gate area for the input transistors, the flicker noise is well suppressed. In order to measure the input-referred noise (IRN), two input terminals are shorted to ground. The measured output noise divided by the measured gain at the closest measured frequency point equals IRN. Fig.6 shows the input-referred noise spectrum density where a noise spectral density of 56 nV/√Hz is observed. By integrating the noise spectral density curve from 1 Hz to 100 Hz we obtain a total input-referred noise voltage of 8.7 $\mu V_{RMS}$.

Also, the common mode rejection ratio (CMRR) is measured by setting the in-band gain of the circuit to 63 dB and applying a sine signal to both input nodes of the front-end and observing the amplitude at the buffer output. A 50 $mV_{p-p}$ sine signal with a frequency of 100 Hz is fed to the front-end; the resulting output signal is below the oscilloscope noise floor of 2 mV. Taking the mismatches induced by package bonding and measurement circuit board into consideration, the CMRR of analog front-end exceeds 90 dB.

### *B. In-Vivo Test*

In order to verify the ASIC performance, an *in-vivo* test is taken to collect live physiological data, where H124SG pre-gelled electrodes are placed on a subject's right arm, chest, and forehead to collect EMG, ECG, and EEG signal respectively. For ECG extraction, the gain and bandwidth are

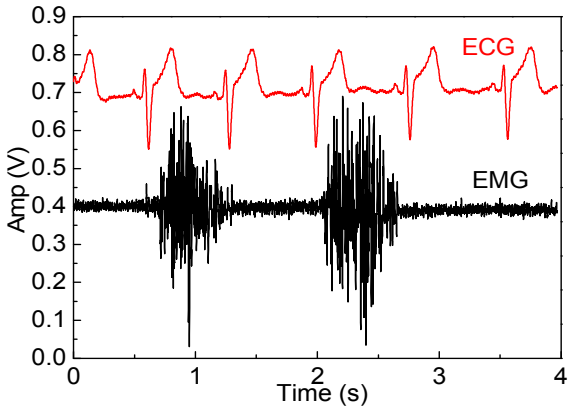



Fig. 7. ECG and EMG signals captured from the analog front-end.

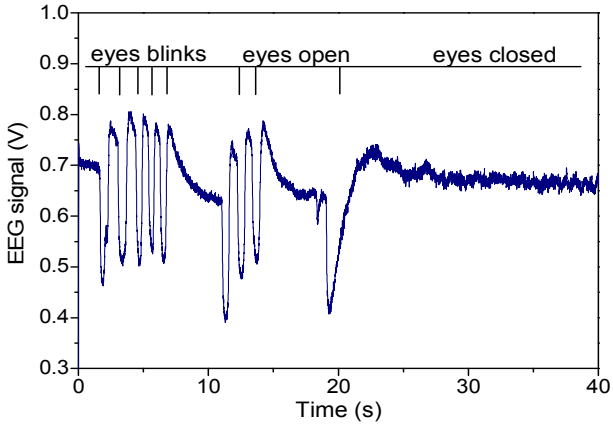



Fig.8 . EEG signal in time domain with eye blinks.

set to 55 dB and 0.3~200 Hz. For EMG extraction, the gain and bandwidth are set to 55 dB and 0.3 Hz~1.5 KHz. For EEG measurement, the gain and bandwidth are set to 61 dB and 0.37~85 Hz. Fig.7 shows the extracted ECG and EMG signals without any post-processing (the DC level is manually adjusted for better illustration). For the EEG measurement, the subject is asked to blink his eyes for 15 seconds, keep eyes open for 5 second, and eyes closed for around 20 seconds. Fig.8 shows EEG recorded from a subject's forehead. The large periodic excursions correspond to eye blinks. The two waveforms in Fig.9 correspond to the cases of eyes-closed and eyes-open. In the first case, the subject closes his eyes for 3 seconds in a relaxed state, evoking the Alpha wave with a characteristic 10 Hz rhythm. In the second case, the subject opens his eyes, and is stimulated by the environment; as a result, alpha wave is vanished. The power spectral density of the two blocks are shown in Fig.10, highlighting the 10 Hz activity of the Alpha wave during the relaxed, eyes closed state. Fig.11 shows the microphotograph of the bio-electric ASIC. The performance summary of the implemented ASIC and a comparison with a state-of-the-art design [1] are summarized in Table I.

## V. CONCLUSION

The proposed ASIC is implemented in a 180 nm 1P6M CMOS technology, occupying 1.5 mm × 3 mm silicon area (including pads), totally consuming 16.7 µA from a 1.2 V

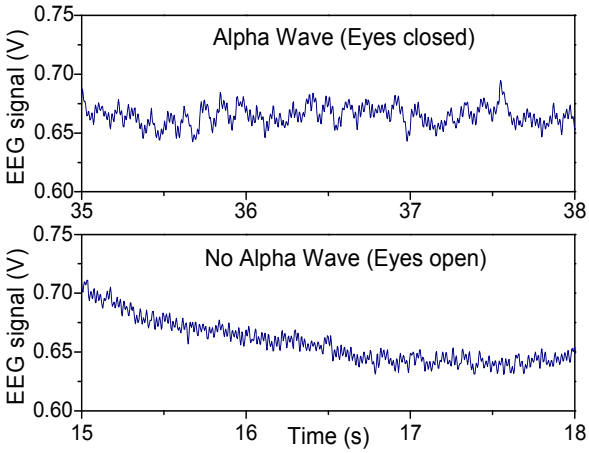



Fig. 9. Time-domain frontal position Alpha wave recording.

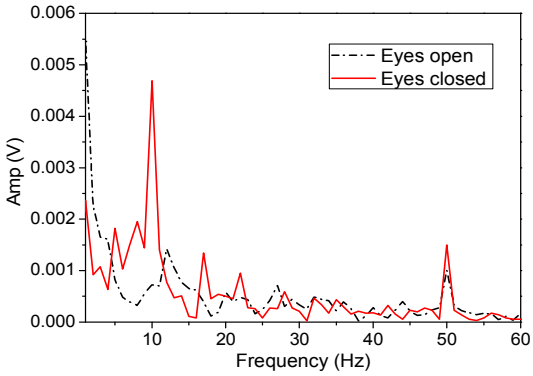



Fig. 10. FFT results for eyes open and eyes closed, where the bump at 10 Hz is the result of Alpha wave typically appears when eyes are closed.

supply. The presented ASIC performs EMG, ECG, and EEG acquisition, digitization and serial communication. Each ASIC corresponds to one bio-potential channel, and up to 14 channels can be applied depending on application requirement. Integrated with the ASIC, an Intelligent Electrode can be dynamically configured as a ME or a SE, and interface directly with μV level signals from the body. The serial connection method using the Active Cable drastically reduces the amount of connecting wires, thus improves the user's comfort and convenience. The command-based SECS process can realize a dynamic network management and trigger the read-out circuit in each SE to extract bio-signal synchronously.

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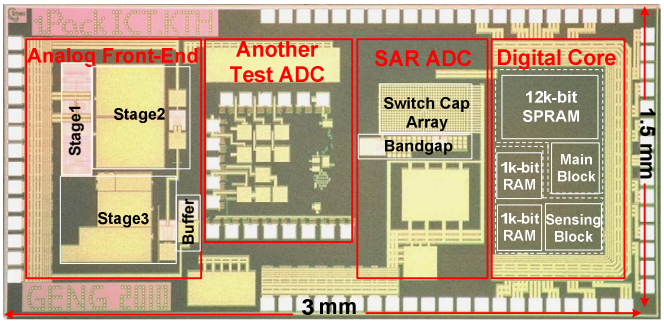


Fig. 11. Die microphotograph of the bio-electric ASIC.

TABLE I
PERFORMANCE COMPARISON

| Parameter | *[1] in ESSCIRC 2010* | ***This work*** |
|---|---|---|
| Technology | 350 nm | 180 nm |
| Supply voltage | 3 V | 1.2 V |
| Num. of Channels | 16 | 14 |
| Sampling method | TDM Sequential | Synchronous |
| Front-end power | >29 μA@3 V | 2.3 μA@1.2 V |
| Mid-band gain | 65 dB | 63 dB |
| ADC power | 410 μA@3 V | 1.8 μA@1.2 V |
| Digital core power | 400 μA@3 V | 12.6~12.7 μA@1.2 V |
| CMRR | - | >90 dB |
| Low cut-off $F_{3dB}$. | 1 Hz | 0.3 Hz |
| High cut-off $F_{3dB}$. | 10 KHz | Tunable to 1.5 KHz |

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