NOCEVE: Network On Chip Emulation and Verification Environment

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***Abstract*—We present in this paper NOCEVE an industrial Network on Chip (NoC) emulation and verification environment on industrial large scale multi-FPGA emulation platform for billion cycle application. It helps designer to improve system performance by the analysis of traffic distribution and balance through the network on chip. The hardware monitoring network is generated by another commercial NoC design tool. It consists of traffic collectors, which is reconfigurable to collect different traffic information such as packet latency and throughput. The statistic traffic information is collected during real application execution on FPGA platform and it is sent through monitoring network on FPGA and then PCI bright board back to host computer for real-time visualization or post-execution data analysis. NOCEVE is the first industrial NoC emulation and verification environment for billion cycle applications.**

Keywords: emulation, FPGA, NoC, verification.

I. INTRODUCTION

Network on Chip (NOC) is adopted as the on-chip communication backbone for modern system on chip (SoC) design. Design with this type of communication architecture presents a new range of debug challenges because its permits split, pipelined, and concurrent transactions between IP blocks. NoC monitoring components and designs are proposed for communication centric debug [1-2]. As the design complexity of SoC keeps increasing, the software design effort need has exceeded that assigned to the hardware. High level abstraction based simulation is used to accelerate the validation of software, while the trade-off of accuracy for speed still cannot solve the hardware/software integration challenges. We use another alternative to prototype SoC design and debug application by emulation on FPGA platform, which has an accurate representation of the design and rapid execution of software application. In this paper, we present NOCEVE a NoC traffic monitoring tool for billion cycle application debug. It helps designers improve system performance by the analysis of traffic distribution and balance through the network on chip.

To our best of knowledge, NOCEVE provides the first industrial NoC monitoring solution for billion cycle application debug.

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II. NOC MONITORING TOOL ON EMULATION PLATFORM

A. EVE Zebu-ServerFPGA platform

Figure 1. ZeBu Server configuration

NOCEVE is designed based on EVE Zebu-Server FPGA emulation platform [4]. ZeBu Server Platform is an extremely high-capacity system emulator with the easy setup and debugging associated with emulation. It is also expandable in a multi-unit environment to accommodate up to 1 billion ASIC gates.

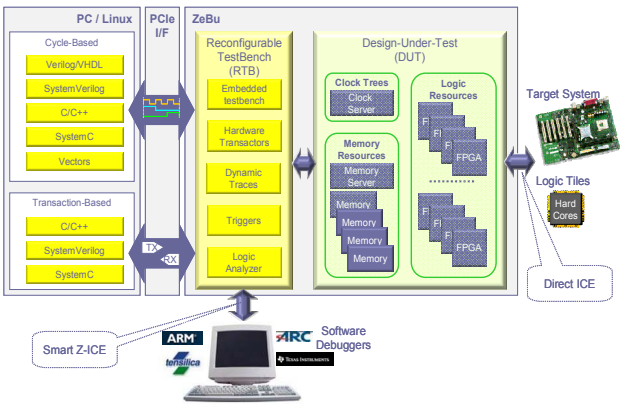

Figure 2. ZeBu-Server Runtime Architecture

In ZeBu-Server, the Design Under Test (DUT) is mapped onto one or several Xilinx Virtex-5 LX330 FPGAs and memory chips. Billion cycle applications can be emulated within 7 minutes on the FPGA platform with a emulation clock of 10MHz.[1,2] The test environment is mapped onto dedicated FPGAs (interface FPGAs, IF) which implement the Reconfigurable Test Bench (RTB), an innovative interface technology made up of a combination of proprietary hardware, firmware and software layers. The ZeBu-Server unit is

connected to the host PC through a PCI Express interconnection board.

B. *NoC monitoring system architecture*

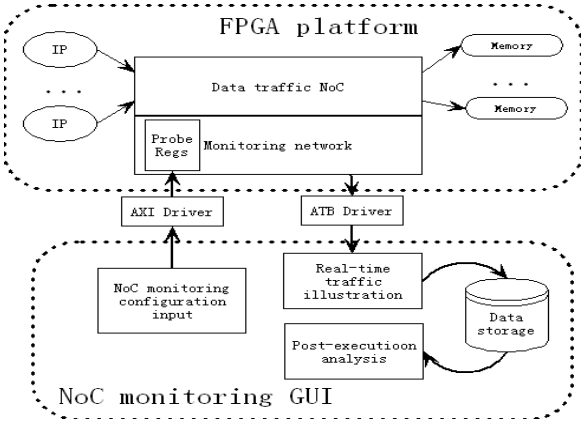

Figure 3. NOCEVE architecture.

The NoC monitoring system architecture is presented in figure 3. It contains three parts: NoC monitoring GUI, hardware monitoring network and HW/SW communication drivers. The software part gets monitoring configuration such as throughput or latency measurement from user and send to hardware monitoring network by AXI driver. The application is executed on FPGA platform. The monitoring network collects traffic information according to user's configuration and sends back to host computer by ATB driver for real-time traffic illustration. Meanwhile, the traffic data is stored to files for post-execution analysis.The monitoring probes capture the information passing from the link and detect the monitored events without introducing any flow control in the system. The internal configuration registers control the monitoring behaviors and can be predefined at design time or be modified and control at run time.

III. NOCEVE BASED PERFORMANCE EVALUATION

The OCP has released a set of synthetic workloads as micro-benchmarks for the evaluation of network on chip [6]. A cluster mesh NoC based multiprocessor is used for benchmark execution [1,2].

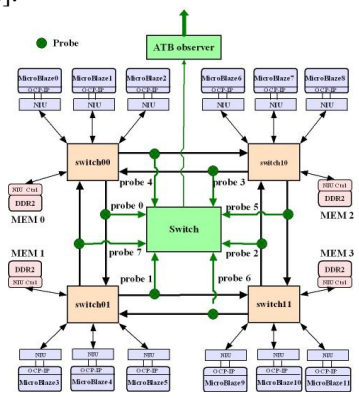

Figure 4. Design case study

We conducted performance evaluation of the OCP Hot Spot benchmark and present post-execution performance analysis.

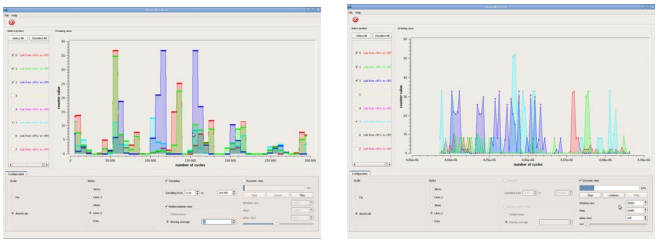

Figure 5. Real-time traffic illusatration interface.

We select the one of the memories as the only hot spot. The packet latency results collected by NoC monitoring are pictured in figure 5 for real-time and post-execution analysis. The real-time traffic is illustrated in the graphic interface of our tool as shown in figure 5. Different traffics are distinguished by colors. Through the interface, user can stop or restart the execution anytime during the application execution for debug. A post-execution analysis can help user to get a global view of NoC traffic distribution both on temporal and spatial distribution as shown in figure 5. Billion cycles traces monitoring and visualization on large SOC designs require efficient traces compression and visualization. 50% compression ratio achieved through wavelet transform of NOC traces. Hardware wavelet IPs can be used on the ZeBu server for fast real-time compression.

IV. CONCLUSION

In this paper, we presented NOCEVE an industrial for NOC emulation and verification environment based on large scale emulation platform for billion cycles application. NOCEVE help designers to improve system performance by the analysis of traffic distribution and balance through the network on chip in a fast and efficient way. Results demonstrate the efficiency of our industrial NoC monitoring tool.

To the best of our knowledge this tool is the only industrial available tool on large scale multi-FPGA platform .

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