IR-Drop Analysis of Graphene-Based Power Distribution Networks

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***Abstract*—Electromigration (EM) has been indicated as the killer effect for copper interconnects. ITRS projections show that for future technologies (22nm and beyond) the on-chip current demand will exceed the physical limit copper metal wires can tolerate. This represents a serious limitation for the design of power distribution networks of next generation ICs.**

New carbon nanomaterials, governed by ballistic transport, have shown higher immunity to EM, thereby representing potential candidate to replace copper. In this paper we make use of compact conductance models to benchmark Graphene Nanoribbons (GNRs) against copper. The two materials have been used to route a state-of-the-art multi-level power-grid architecture obtained through an industrial 45nm physical design flow. Although the adopted design style is optimized for metal grids, results obtained using our simulation framework show that GNRs, if properly sized, can outperform copper, thus allowing the design of reliable circuits with reduced IR-drop penalties.

I. Introduction

The need to account for large switching current demands at scaled supply voltages makes the design of metallic power distribution networks (also called *power-grids*) a key issue for the next generation of gigascale ICs [1]. The capability of delivering stable V_{dd} and ground levels across the entire chip is essential not just for controlling signal noise immunity and circuit functionality, but also to determine the speed of signals transitions. The latter, in particular, is of paramount importance when considering power optimization: slow transitions at the input of CMOS gates may result in longer periods of time during which both pull-up and pull-down paths conduct simultaneously allowing more current to flow from V_{dd} to ground, i.e., more *short-circuit* current.

Unfortunately the power supply integrity is severely compromised due to the non-ideal nature of the conductors used to connect active devices to off-chip supply/ground pins; While the resistive effect of parasitics cause ohmic voltage drops, i.e., *IR-drop*, parasitic inductance may induce large inductive voltage drops in the presence of fast current transients, i.e., *L(di/dt)-drop*.

In the last decade, the problem of controlling transient voltage drops has been addressed following two orthogonal directions [2]. On the one hand, research efforts have been focusing on alternative physical design solutions that aim at reducing the effective impedance of the power distribution network, such as multi-layers power-grids and decoupling capacitors insertion; On the other hand, several optimization techniques have been proposed at the circuit level to distribute current demands and avoid fast current variations, such as clock skewing, flip-flop de-synchronization, and, for power-gated circuits, time-shifted power mode transition [3], [4].

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While effective in reducing power supply noise, these techniques fail to address another critical issue, that is, reliability. Metal reliability is generally assessed by studying *electromigration* (EM). EM refers to the gradual displacement of the metal atoms of a conductor from one point to another due to the current carried by the conductor itself. This mechanism leads to the formation of *voids* at some points in the metal line and *hillocks* (or extrusions) in other points, which result in the creation of open-circuit of individual wires or short-circuits among adjacent wires. EM-induced wear-out mechanisms have been well modeled through the Black's equations which describes the maximum current density (J_{EM}) that can safely flow in a wire ($10^7 A/cm^2$ for copper) before causing EM. A common design practice is to size cross-section of the metal wires such that $J_{MAX} \leq J_{EM}$, where J_{MAX} is the maximum equivalent dc current expected to be required by the circuit divided by the cross-sectional area of a metal wire itself. However, due to higher switching currents and the aggressive scaling of wire geometries, the gap between J_{MAX} and J_{EM} is getting closer at each technology node and, unless new breaking solutions will appear, this physical constraint will be violated within the next decade [1].

The discovery of new one-dimensional carbon nanomaterials, like *Carbon NanoTubes* (CNT), and *Graphene NanoRibbons* (GNRs), offer potential solutions to the reliability problem. Besides showing longer mean-free path, which traduces into higher carrier mobility, the ballistic transport that governs current flow makes such materials resilient to EM. Results reported in [5] show that graphene-based materials can tolerate maximum current density of one order of magnitude larger than that of copper ($10^8 A/cm^2$). Nevertheless, the debate about which of these materials will prevail is still open, and it will be clear only when the candidate to replace FET transistors will show up. For instance, if graphene-based switches are identified as substitute to CMOS transistors, than it would be logical to use graphene conductors.

While waiting for such market-driven decision, it is important to understand whether one can take advantage of these new materials. Most of the works done in this field rings around CNT interconnects [6], [7], [8], and only few of them deal

with power interconnects [9]. However, while the fabrication of CNTs requires a bottom-up method in which the tubes must be aligned and placed either during growth, for GNRs, that are planar by nature, standard pattering process similar to those used for CMOS technologies can be used. Moreover, and this is another main reason why GNRs are becoming more popular than CNTs, many research groups started to investigate *all-graphene* designs where the metal-semiconductor junctions are formed on the same one-dimensional layer through a change of chirality [10]. Enabling such a technology in the VLSI domain could have a true impact on the semiconductor industry, and may open new research scenarios, especially in the field of design automation [11].

Motivated by this revolutionary change, in this paper we benchmark GNRs against copper as power-grid material. The goal is to prove that, if properly sized, GNRs can show smaller equivalent resistance than Cu, thus allowing smaller voltage drops, better performance and immunity to aging mechanisms. As preliminary study we assumed a classic ASIC implementation flow where the power distribution network consists of a mesh made up of alternate V_{dd} and ground parallel wires that are routed on two different layers (the horizontal layer and the vertical layer); contacts and vias assure the full connectivity through the layers and toward the logic gates placed at the lowest level. The circuit netlist is generated through a commercial design flow during which the HDL code is synthesized, placed and routed using an industrial 45nm design kit. Based on compact conductance models, an in-house simulation framework is then used to generate the equivalent electrical model of the power-grid, for both Cu and GNR, and emulate actual current demand under real workloads. Collected output provide detailed voltage tracking across the layout of the chip. It is worth emphasizing that we opted for a standard power-grid implementation, that is optimized for metal conductors, in order to make copper the front runner competitor. The paper is organized as follows: Section II introduces the conductance models for the GNR, while Section III describes the simulation framework we implemented to simulate GNR-based power-grids; experimental results are collected and discussed in Section IV; Section V gives ends the paper with some final remarks.

II. Conductance Models of GNR

Graphene Nanoribbons (GNRs) are narrow sections a single layer of carbon atoms packed in a hexagonal lattice [12] (Figures 1-a and 1-b). Using standard pattering process, it is possible to extract two types of GNRs depending on the number of hexagon rings present along the width (i.e., the *chirality*): *ZigZag* or *Armchair*. Zigzag GNRs (zz-GNRs)show always metallic properties, while Armchair can be either semiconducting or metallic depending on the total width of the ribbon. For pure interconnect purposes Zigzag GNRs are typically preferred.

Single layer GNRs can be stacked obtaining a multilayer nano-structure (Figure 1-c). The latter, if properly engineered, can show enhanced electrical properties w.r.t. single-layer

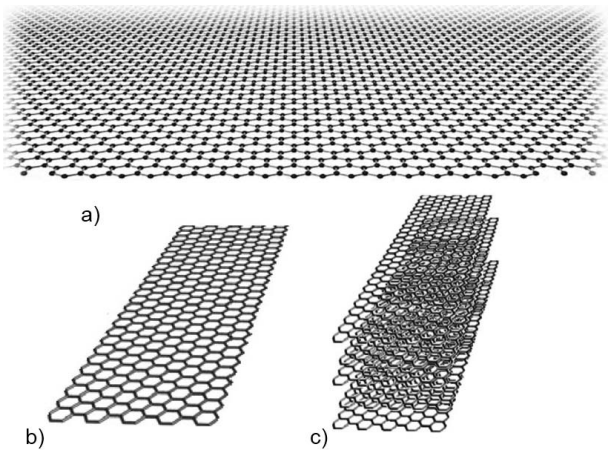

Fig. 1. a) A sheet of graphene[12]; b) Single-layer GNR;c) Multi-Layers GNR [5]

GNRs. The next two sections introduce compact conductance models for both Single- and Multi-Layer Zigzag GNRs that we embedded in our IR-drop simulation framework.

A. Single-Layer GNR

Since its discovery in 2004, many papers have been published about the conductance model of GNR [13][5][14]. The following lines provide a quick overview of one of the most accredited model. Readers can refer to [5] for a more detailed discussion.

The total conductance of a single layer zigzag GNR layer G_{SL} (in unit of S) can be calculated by summing conductance due to the electrons in the conduction energy bands $G_m(e^-)$ and to holes in the valence bands $G_m(h^+)$

$$G_{SL} = \sum_m G_m(e^-) + \sum_m G_m(h^+) \tag{1}$$

with G_m the conductance of the m-th conduction mode (due to electrons or holes) as described by the Landauer formula [15]. The number of modes M supported in the structure depends on the total width of the structure itself, that is, the wider the ribbon, the larger the number of supported modes; intuitively, larger structures show higher conductance due to larger number of modes that contribute to electric transmission.

For zz-GNRs the summation of Equation 1 can be transformed into an integration form as follows:

$$G_{SL} \approx \left[\int_0^\infty G_m(e^-) dE_m + \int_{-\infty}^0 G_m(h^+) dE_m \right] \tag{2}$$

where E_m is the minimum (maximum) energy of the m-th conduction (valence) mode, and can be expressed as

$$E_0 = 0; \qquad E_m = (|m| + 1/2) \cdot h v_f / 2w \qquad m \neq 0 \tag{3}$$

with h the Planck's constant, $v_f = 10^6$ m/s the Fermi velocity, and w the width of the GNR.

The results of the above integrals provide the final total conductance as reported in Equation 4.

$$G_{SL} = \frac{1}{L}\frac{2q^2}{h}\frac{2w^2}{h\nu_F}2K_BT\ln\left[2\cosh\left(\frac{E_F}{2K_BT}\right)\right]f(w,l_D) \tag{4}$$

with,

$$f(w,l_D) = \begin{cases} 2\ln\left(\frac{l_D}{w}\right) + 2\ln 2 - 2 + \frac{\Pi w}{l_D} & \text{if } l_D \gg w \\ \frac{\pi l_D}{2w} - \frac{2l_D^2}{3w^2} & \text{if } l_D \ll w \end{cases} \tag{5}$$

where L is the length of the GNR, and l_D(=1μm) is the mean free path corresponding to scatterings due to physical defects and phonons. Please refer to [5] for a detailed derivation.
Figure 2 shows the Resistance vs. Width plot for a 1μm metal wire realized with copper (dotted line) and single layer GNR (full line); the thickness for copper wires is assumed to be 7% of the wire width for W $\geq$ 30 nm, and 2 nm for smaller widths [16]. As one can see, the resistance of the single layer graphene is less than copper only for widths less than 7nm. Since for typical width of the global interconnects, that are in the order of some μm, copper show better resistance, single-layer GNRs are clearly not competitive. However, this analysis underline the possibility to use single-GNR for local-level power-grids, or in the future, for mono-layer all-grapehene circuits.
In the next section, we make use of the equation derived for G_{SL} to create a conductance model for stacked layers GNR.

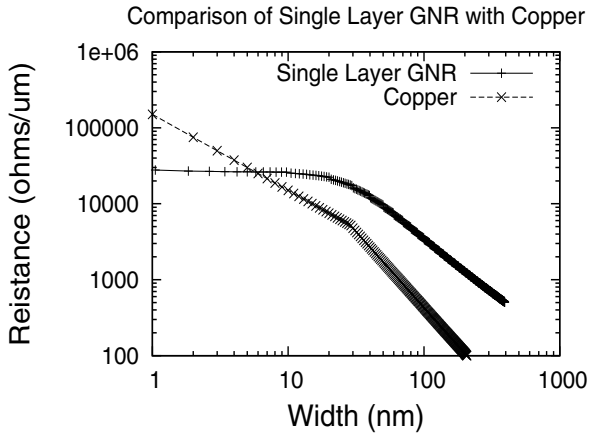

Fig. 2. Copper vs. GNR resistance for a 1μm length wire

B. Multi-Layer GNRs

While simpling stacking single-layer GNRs generate neutral structures with poor electrical conductance, the use of intercalation doping allows to generate multi-layer GNRs with enhanced conductivity [17]. The intercalation process involves an insertion of dopant layers (dots in Figure 3) between each pair of graphene layers (solid lines in Figure 3). The level of intercalation doping is indicated by stage indexes, where stage g indicates that there are g graphene layers between each pair of adjacent intercalation layers; in Figure 3, *Stage-1* (*Stage-2*) denotes structures with one (two) graphene layer(s) between two doping layers. The effect of the intercalation doping is that of increasing the carrier density, due to charge transfer, and increase the Mean Free Path (MFP), due to suppression of inter layer scattering [18]. For a fixed thickness t of material, the total number of graphene layers N can be easily calculated as t/s, where s represents the average layers spacing $(S_1+S_2)/2$ using as reference Figure3.

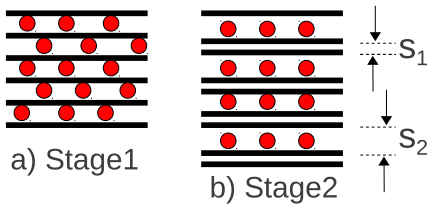

Fig. 3. Intercalated doped multi-layer GNR; with $s1$ and $s2$ representing the thickness of graphene layers and doping layers respectively

Since the interaction between each and every pair of graphene layers can be made very small [5], the conductance of multi-layer graphene can be simply obtained by superimposing the contribution of each single layer:

$$G_{ML} = \sum_n G_{SL}(n) \tag{6}$$

where $G_{SL}(n)$ the conductance of the n-th layer. Considering homogeneous GNRs, where all the layers have the same atomic structure, the final conductance equation becomes:

$$G_{ML} = N * G_{SL} \tag{7}$$

with N the total number of graphene layers.

III. Power Grid Model and Simulation Framework

Main function of the on-chip power distribution network is to uniformly distribute V_{dd} and ground signals across the entire layout while guaranteeing a minimum impedance path toward the external power supply pins. State-of-the-art architectures for digital ICs are commonly structured as multilayer grid [2] where V_{dd}/ground stripes are orthogonally routed in adjacent metalization layer (usually the topmost metal layers). As shown in Figure 4, where blue and white stripes represent V_{dd} and ground respectively, the lines are typically alternate and equally distanced. Contacts at the crossing junction allow electric continuity between layers. The thickness of the stripes are typically dictated by the metalization process of a given technology, while length and width are suitably selected according to the current demand and the voltage drop constraints. Accurate voltage drop analyses require dedicated power-grid modeling. To accomplish this task we implemented a dedicated SPICE-based simulation framework. As shown in Figure 5 it consists of three main steps:

1) *Resistive mesh generation:* using physical data generated by the routing tool, an intermediate abstract model of the power-grid is generated (Figure 6). It consists of a matrix data-structure where each element represents a cross junction between layers; such elements store the geometries of the segment wires connecting adjacent

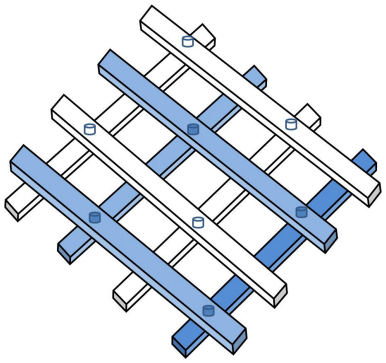

Fig. 4. A two-level power grid structure.

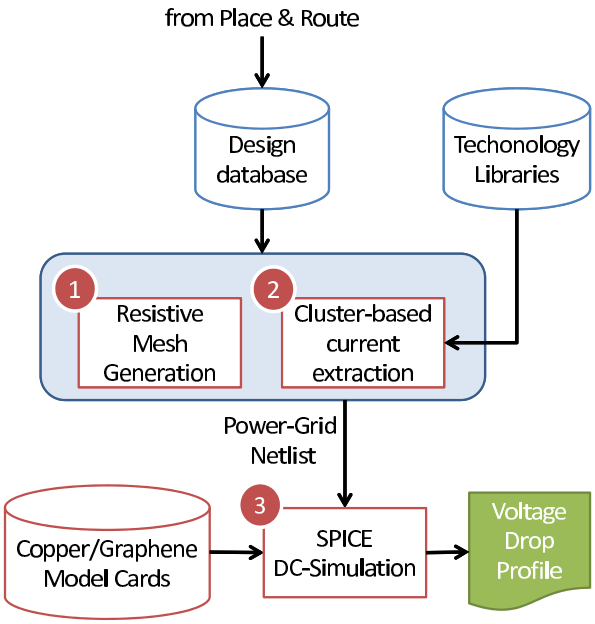

Fig. 5. Implemented simulation framework

points, i.e., segment width W_{seg}, length L_{seg}, and thickness t (that we consider as fixed technology-dependent value). Those data are than fed as input to a built-in tool that is in charge of generating an equivalent SPICE netlist. The latter consists of a regular grid of elements associated to a parametrized SPICE macro. Such macro can be linked to different model cards whose internal equations describe the resistive behavior of an unitary piece of material. Available models include copper or graphene. Notice that two meshes are generated, the V_{dd} mesh and the ground mesh.

2) *Current matrix extraction:* the placed layout is partitioned into a number of equally sized square regions. Cells belonging to a specific region form a cluster for which the total peak circuit is computed as the sum of individual cell currents using the upper-bound method described in[19]. For each cluster, the current demand is modeled as an ideal dc current supply source. Each current source is integrated within the SPICE netlist and connected to junction points of the power/ground grid, Figure 6.
3) *Simulation:* The generated netlist is then simulated using DC analysis and voltage drops measured at each crosspoint of the mesh.

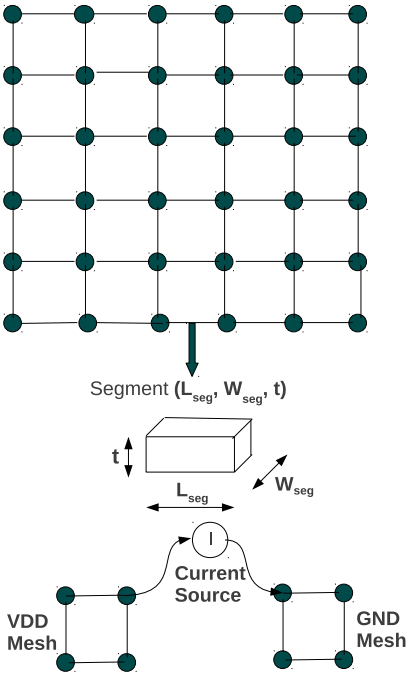

Fig. 6. R/I based power-grid modeling through

IV. Analysis

A. Design Flow and Simulation Set-up

The power-grids we used as benchmarks have been obtained through a commercial physical synthesis flow belonging to an industrial 45nm design kit provided by STMicroelectronics. The simulation have been conducted on three different digital circuits that are representative of different chip sizes: *benchmark1* $\simeq$ 2 Kgates, *benchmark1* $\simeq$ 20 Kgates, *benchmark3* $\simeq$ 100 Kgates. The HDL description of the circuits have been synthesized using Synopsys Design Compiler. The obtained logical netlists are then placed & routed following a semi-custom row-based layout style using Synopsys ICCompiler. Knowing the physical dimensions of the die we run the power-network synthesis of the power grids. During this process, V_{dd} and ground stripes are routed at the two upper metal layers (M6 and M7). Constraints have been fixed such that the total voltage drop across the logic gates is below 15% pf V_{dd} with $V_{dd} = 1.1V$ in the presence of worst-case current pattern.
After synthesis, an output file containing information on the physical dimensions of all the instances placed in the layout (also including those of the V_{dd} and ground rails) is made available. Using ad-hoc plug-in written in TCL and integrated into IC-Compiler, we implemented the simulation flow described in Section III. As final stage we used the HSPICE

Power Grid Material	Benchmark1 (V_{dd} / ground)	Benchmark2 (V_{dd} / ground)	Benchmark3 (V_{dd} / ground)
Copper (t=1.04um)	15.5 / 18.99	44.4 / 50.43	72.2 / 77.58
Multi-layer GNR (t=1.04μm)	11.9 / 10.19	33.1 / 27.43	45.82 / 42.19
Multi-layer GNR (t=0.8μm)	15.3 / 13.25	43.01 / 35.65	59.21 / 54.83
Multi-layer GNR (t=0.6μm)	20.40 / 17.59	57.35 / 47.53	79.39 / 73.11

TABLE I
PEAK VOLTAGE DROP (mV) MEASURED ON THE V_{dd} AND GROUND RAILS.

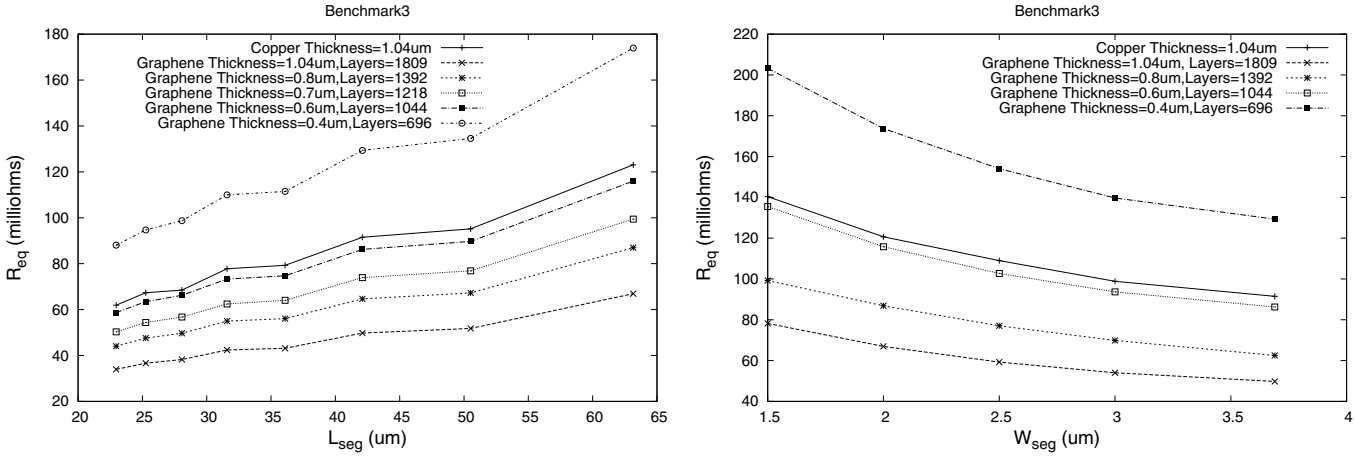

Fig. 7. Characterization of the equivalent resistance R_{eq}; left: R_{eq} vs. L_{seg} with W_{seg}=3.7; right: R_{eq} vs. W_{seg} with L_{seg}=42.1

engine of Synopsys to perform the electrical simulations. To notice that the conductance model of graphene is embedded through the Verilog-SPICE feature of HSPICE.

B. Simulation Results

Table I summarizes the peak IR-drop voltages we measured across the power-grids for the three benchmarks under test. Each column reports both V_{dd} and ground drops. Three multi-layer GNRs wires with different thickness t have been considered; t=1.04um (1809 layers), t=0.8μm (1392 layers), t=0.6um (1218 layers). Width W_{seg} and Length L_{seg} of power grids segments are those obtained from the synthesis flow, i.e., those obtained considering copper resistivity. As one can see, thanks to a multi-layered structure, GNRs having the same thickness of copper can guarantee lower IR-drops, while, for lower thickness, IR-drop increases. However, for $t = 0.08$, i.e., 22% less than copper, GNRs still show better performance.

For an in-depth comparison of the two materials, we now show the results obtained from the characterization of the equivalent resistance R_{eq} of the power-grid for different sized wire segments. The R_{eq} is defined as the ratio between the maximum IR drop in the grid and the peak current drained through the grid itself: $R_{eq-V_{dd}} = V_{drop-V_{dd}}/I$ for the V_{dd} grid, and $R_{eq-GND} = V_{drop-GND}/I$ for the ground grid. For the sake of space, in Figure 7 we report the characterization results for the $R_{eq-V_{dd}}$ only and for the largest benchmark. The first plot (left) clearly shows that, as the thickness increases, i.e., larger number of stacked layers, the resistive path to V_{dd} reduces, and, in the best case (t=1.04μ), it results lower than that of copper (solid line). To notice that this is true whatever the value of L_{seg}, namely, whatever is the routing density of the power-grid. Moreover, one should also observe that the same R_{eq} of copper can be approximately obtained using a multi-layer GNR that is 40% thinner ($t = 0.6\mu$m). Similar conclusions can be carried out when considering the dependence from W_{seg}: If the thickness is the same of copper, GNR power grid has less equivalent resistance, no matter the width of the stripes.

The above analysis underlines that is possible to achieve the same IR-drop of copper using less dense GNR power-grids. In other words, the use of multi-layer GNRs, besides making ICs more reliable at no cost of performance penalties, may be also exploited to reduce the routing area of the power grids. The saved space could be therefore used to route signal interconnects, for which routing congestion is well known to be a serious concern, or, it can be utilized efficiently for multi voltage designs, for which multiple V_{dd} rails are required. To sustain this claim, Figure 8 plots the pairs $\{L_{seg}, W_{seg}\}$ for which the equivalent resistance of a GNR power-grid R_{GNR} shows the same equivalent resistance of a power-grid implemented with copper. Two copper configurations are considered as reference: $\{L_{seg}, W_{seg}\}$=$\{28.07,\ 3.96\}\mu$m (solid line), $\{L_{seg}, W_{seg}\}$=$\{22.96,\ 3.96\}\mu$m (dotted line). The plot clearly shows that the same R_{eq} can obtained using GNR power-grids made up of segments with larger L_{seg} and smaller W_{seg}. The leftmost point of the solid line, for instance, indicates that a GNR power-grid with $L_{seg} = 32.3\mu m$ and $W_{seg} = 0.65\mu m$ shows the same R_{eq} of that of copper with $L_{seg} = 28.07.3\mu m$ and $W_{seg} = 3.69\mu m$. This traduces in less

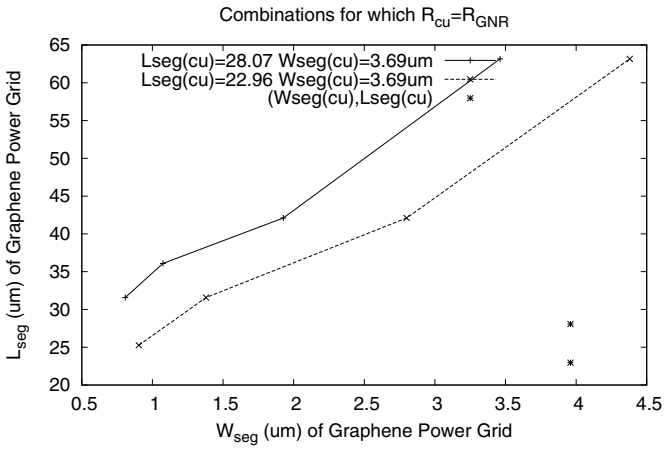

Fig. 8. $\{ L_{seg}, W_{seg} \}$ for which resistance of GNR grids equals that of copper; thickness of the wires are kept constant, t=1.04μm

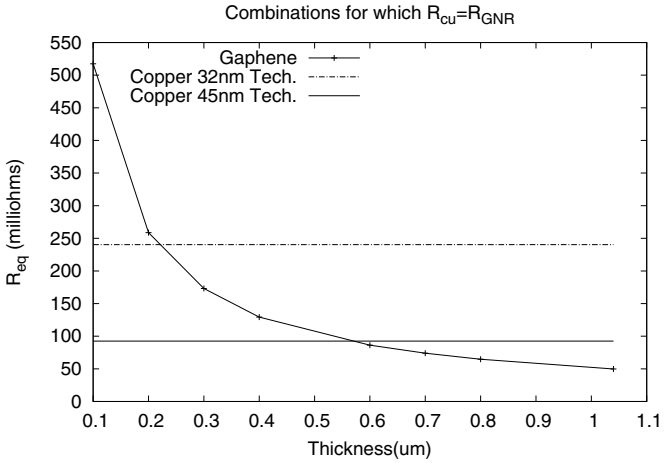

Fig. 9. Equivalent resistance of equalized grids L_{seg}=42.1μm and W_{seg}=3.7μm implemented with GNRS and copper at 45nm and 32nm technology nodes

dense power-grids, which in turn means more available free space that can be used for other purposes.

As final remark we would like to provide a projection of these results for the next technology nodes. Figure 9 shows the equivalent resistance of copper grids at 45nm and 32nm nodes (horizontal lines) against GNRs. As one can see, due to scaled geometries, copper grids of next generations will show larger R_{eq}, therefore shifting the crossing with GNR toward thinner ribbons.

V. Conclusions

Whatever will be the emerging technology that replaces copper wires, it is important to understand which are the potential benefits the new material can offer.

In this paper we addressed this issue at the power distribution level. Using compact conductance models embedded into an in-house simulation framework, we have shown that using multi-layer GNR as routing material for two-level power-grids can help to achieve smaller V_{dd} to ground equivalent resistance. This results in lower voltage drops, i.e., better performance, while intrinsically increasing the reliability, i.e., immunity to electromigration. The achieved savings in terms of voltage drop can be used to make chips faster and less power-hungry, or, to reduce power-grids routing density in order to create more available space. The latter can be used for signal interconnects or multi-V_{dd} grids. Using projection data of future nodes (32nm and 22nm), superiority of GNRs has also been showed for next generation of ICs.

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