DATE 16

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University Booth

Organisation

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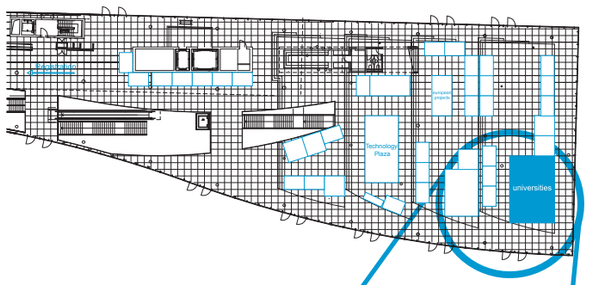
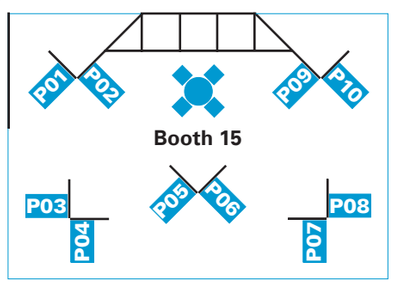
TECHNISCHE UNIVERSITÄT DRESDEN





Thursday March 17, 2016

EDA Prototypes

10:00 12:00 14:30
12:00 14:30 16:30
UB09 UB10 UB11

P: Presenter | A: Author

PSMGen: Automatic generation of power state machines
P: Alessandro Danese[1] | A: Alessandro Danese[1], Graziano Pravadelli[1] and Daniel Lorenz[2]; [1]U of Verona, IT; [2]OFFIS - Institute for Information Technology, DE

A Circuit Extraction Tool for Full Custom Designed MEMS Sensors
P: Axel Hald[1] | A: Axel Hald[1], Johannes Seelhorst[1], Mathias Reimann[1], Juergen Scheible[2] and Jens Lienig[3]; [1]Robert Bosch GmbH, DE; [2]Reutlingen U, DE; [3]TU Dresden, DE

CLaSH: Digital circuits in CλaSH
P: Christiaan Baaij | A: Christiaan Baaij and Jan Kuper, U of Twente, NL

AGAMID: A TLM framework for evaluation of hardware-enhanced many-core run-time management
P: Daniel Gregorek | A: Daniel Gregorek and Alberto Garcia-Ortiz, U of Bremen, DE

Workcraft: framework for interpreted graphs
P: Danil Sokolov | A: Danil Sokolov, Newcastle U, GB

CONTREP: A single-source framework for UML-based Modelling and Design of Mixed-Criticality Systems
P: Fernando Herrera | A: Fernando Herrera and Eugenio Villar, U of Cantabria, ES

Automated Refinement of Analog/Mixed-Signal SystemC Models by Non-Functional Effects
P: Georg Gläser[1] | A: Georg Gläser[1], Hyun-Sek Lukas Lee[2], Eckhard Hennig[3], Markus Olbrich[2] and Erich Barke[2]; [1]IMMS, DE; [2]Leibniz U Hannover, DE; [3]Reutlingen U, DE

Formal Verification of Clock Domain Crossing using Gate-level Models of Metastable Flip-Flops
P: Ghaith Tarawneh | A: Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev, Newcastle U, GB

D-VASim: Timing Analysis of Genetic Logic Circuits using D-VASim
P: Hasan Baig | A: Hasan Baig and Jan Madsen, Technical U of Denmark, DK

AHLS_Desync: Desynchronization Tool for High-Level Synthesis of Asynchronous Circuits
P: Jean Simatic | A: Jean Simatic, Rodrigo Possamai Bastos and Laurent Fesquet, TIMA Laboratory, FR

UCAF Tool: An Optimization-Based Design Methodology for Ultra-Low Voltage Analog Integrated Circuits
P: Lucas Severo[1] | A: Lucas Severo[1] and Wilhelmus Noije[2]; [1]Federal U of Pampa, BR; [2]U of São Paulo, BR

AIPHS: AdaptIve Profiling Hardware Sub-system
P: Luigi Pomante | A: Luigi Pomante, Giacomo Valente and Vittoriano Muttillo, Università degli Studi dell'Aquila, IT

In-node processing: Modelling Framework for In-Node Processing in Industrial Sensor and Actuator Networks.
P: Qaiser Anwar | A: Qaiser Anwar, Muhammad Imran and Mattias O´Nils, Mid Sweden U, SE

IDDD: An Interactive Dependability Driven Design Space Exploration
P: Stefan Scharoba, Brandenburg | A: Stefan Scharoba, Jacob Lorenz and Heinrich T. Vierhaus, Brandenburg U of Technology Cottbus-Senftenberg, DE

Electro-, Stress- and Thermomigration: Three Forces, One Problem
P: Steve Bigalke | A: Steve Bigalke and Jens Lienig, TU Dresden, DE

Secure System Prototypes

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ReSecu_4_AmBRAMs: Towards Increased Reliability and Hardware Security Using AmBRAMs
P: Petr Pfeifer | A: Petr Pfeifer, TU Liberec, CZ

Hardware Design & Test Prototypes

10:00 12:00 14:30
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MicroTESK ARMv8 Edition: Specification-Based Test Program Generator
P: Andrei Tatarnikov | A: Andrei Tatarnikov, Alexander Kamkin and Artem Kotsynyak, Russian Academy of Sciences (RAS), RU

High-End 122GHz Miniature Radar Sensor for Autonomous Aircrafts
P: Federico Nava[1] | A: Federico Nava[1] and Christoph Scheytt[2]; [1]Heinz Nixdorf Institute - U Paderborn, DE; [2]Heinz Nixdorf Institute - Paderborn, DE

ChImpAnC: Change Management using ChImpAnC
P: Jannis Stoppe | A: Jannis Stoppe, Martin Ring and Rolf Drechsler, DFKI and U of Bremen, DE

BioViz: An Interactive Visualization Engine for Microfluidic Biochips
P: Oliver Keszöcze[1] | A: Oliver Keszöcze[1], Jannis Stoppe[2], Robert Wille[3] and Rolf Drechsler[2]; [1]U of Bremen, DE; [2]DFKI and U of Bremen, DE; [3]Johannes Kepler U, AT, DFKI and U of Bremen, DE

Retrascope: Toolkit for Analysis and Verification of HDL Designs
P: Sergey Smolov | A: Sergey Smolov, Alexander Kamkin and Mikhail Lebedev, Russian Academy of Sciences (RAS), RU

Automotive System Prototypes

10:00 12:00 14:30
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UB09 UB10 UB11

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COMPSOC: Virtualising Control Applications on a Distributed CompSOC Platform
P: Kees Goossens | A: Kees Goossens, Eindhoven U of Technology, NL

5G, 3D Design or IoT Prototypes

10:00 12:00 14:30
12:00 14:30 16:30
UB09 UB10 UB11

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LISA: Enabling Layered Interoperability for Internet of Things Through LISA
P: Behailu Shiferaw Negash[1] | A: Behailu Shiferaw Negash[1], Amir-Mohammad Rahmani[1], Tomi Westerlund[1], Pasi Liljeberg[1] and Hannu Tenhunen[2], [1]U of Turku, FI; [2]U of Turku, FI and Royal Institute of Technology (KTH), SE

6Ch-SDR-Platform: 6 Channel SDR Prototyping Platform for vehicle self-localization
P: Marko Rößler[1] | A: Marko Rößler[1], Ulrich Heinkel[1], Daniel Fross[1] and Ahmad El-Assaad[2], [1]TU Chemnitz, DE; [2]Novero GmbH, DE

DATE 16

University Booth

University Booth at DATE 2016

DATE, the Design, Automation and Test Conference and Exhibition is the unique European event bringing together researchers, user and vendors as well as specialists in the design, test and manufacturing of electronic circuits and systems.

The University Booth is organised during DATE and will be located in booth 15 of the exhibition area. All demonstrations will take place from Tuesday, March 15 to Thursday, March 17, 2016 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 49 demonstrations from 18 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover the topics:

- 5G wireless network Prototypes
- 3D-IC integration Prototypes
- FD-SOI Prototypes
- IoT Prototypes
- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Automotive System Prototypes
- Secure System Prototypes

The University Booth at DATE 2016 invites you to booth 15 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information can be found online at http://www.date-conference.com/exhibition/u-booth.

See you at the University Booth (Booth 15)!

Jens Lienig and Andreas Vörg (University Booth Co-Chairs)

Tuesday March 15, 2016

EDA Prototypes

10:30 12:30 15:00 17:30
12:30 15:00 17:30 19:30
UB01 UB02 UB03 UB04

P: Presenter | A: Author

AGAMID: A TLM framework for evaluation of hardware-enhanced many-core run-time management
P: Daniel Gregorek | A: Daniel Gregorek and Alberto Garcia-Ortiz, U of Bremen, DE

Workcraft: framework for interpreted graphs
P: Danil Sokolov, | A: Danil Sokolov, Newcastle U, GB

CONTREP: A single-source framework for UML-based Modelling and Design of Mixed-Criticality Systems
P: Fernando Herrera | A: Fernando Herrera and Eugenio Villar, U of Cantabria, ES

Analysis and Verification of Communication Fabrics
P: Frank Burns | A: Frank Burns, Danil Sokolov and Alex Yakovlev, Newcastle U, GB

Formal Verification of Clock Domain Crossing using Gate-level Models of Metastable Flip-Flops
P: Ghaith Tarawneh | A: Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev, Newcastle U, GB

PFPSim: A Programmable Forwarding Plane Simulator
P: Gordon Bailey | A: Gordon Bailey, Concordia U, CA

D-VASim: Timing Analysis of Genetic Logic Circuits using D-VASim
P: Hasan Baig | A: Hasan Baig and Jan Madsen, Technical U of Denmark, DK

AIPHS: Adaptlve Profiling Hardware Sub-system
P: Luigi Pomante | A: Luigi Pomante, Giacomo Valente and Vittoriano Muttillo; Università degli Studi dell'Aquila, IT

eTeak: Asynchronous Dataflows Synthesis onto FPGAs Using the eTeak Framework
P: Mahdi Jelodari Mamaghani | A: Mahdi Jelodari Mamaghani, Jim Garside and Steve Furber, The U of Manchester, GB

RT-PowMods: Run-Time CPU Power Models from Real Data
P: Matthew Walker[1] | A: Matthew Walker[1], Stephan Diestelhorst[2], Andreas Hansson[2], Geoff Merrett[1] and Bashir Al-Hashimi1; [1]U of Southampton, GB; [2]ARM Ltd., GB

gPCDS: An Interactive Tool for Creating Schematic Module Generators in Analog IC Design
P: Matthias Greif | A: Matthias Greif and Juergen Scheible, Reutlingen U, DE

GRIP: Graph-Rewriting-Based IP-Integration (GRIP) - An EDA Tool for Software Defined SoC Design
P: Munish Jassi | A: Munish Jassi, Yong Hu, Jian Lyu, Daniel Mueller-Gritschneder and Ulf Schlichtmann, TU München, DE

ALPT: A Fast Prototyping Methodology with Constrained Floorplaning on Analog Layout Generation
P: Po-Cheng Pan | A: Po-Cheng Pan, Hung-Wen Huang and Hung-Ming Chen, National Chiao Tung U, TW

In-node processing: Modelling Framework for In-Node Processing in Industrial Sensor and Actuator Networks.
P: Qaiser Anwar | A: Qaiser Anwar, Muhammad Imran and Mattias O´Nils, Mid Sweden U, SE

Extra-functional Property Simulation with Virtual Platforms
P: Ralph Görgen | A: Ralph Görgen, Kim Grüttner and Sören Schreiner, OFFIS - Intitute for Information Technology, DE

IDDD: An Interactive Dependability Driven Design Space Exploration
P: Stefan Scharoba | A: Stefan Scharoba, Jacob Lorenz and Heinrich T. Vierhaus, Brandenburg U of Technology Cottbus-Senftenberg, DE

Electro-Thermal Simulator for Chip Design
P: Vladyslav Ladonkin | A: Vladyslav Ladonkin and Juergen Scheible, Reutlingen U, DE

P05 P08 P02 P10 P07 P09 P03 P08 P09 P05 P03 P02 P08 P08 P08 P04 P03 P10 P01 P02 P02 P06 P06 P06

Hardware Design & Test Prototypes

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MicroTESK ARMv8 Edition: Specification-Based Test Program Generator
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High-End 122GHz Miniature Radar Sensor for Autonomous Aircrafts
P: Federico Nava | A: Federico Nava and Christoph Scheytt, Nixdorf Institute - Paderborn, DE

A-LOOP: AMP system with a dual-core ARM Cortex A9 processor with Linux operating system and a quad-core Leon3 processor with Linux Operating system, OpenMP library and hardware profiling system
P: Giacomo Valente | A: Giacomo Valente and Vittoriano Muttillo, Università Degli Studi Dell'Aquila, IT

NeuroDSP: A Multi-Purpose Energy-Optimized Accelerator For Neural Networks
P: Jean-Marc PHILIPPE | A: Jean-Marc PHILIPPE, Alexandre CARBON and Renaud SCHMIT, CEA LIST, FR

Digitally Driven Top-Down Methodology for Mixed Signal Circuit Design
P: Markus Mueller | A: Markus Mueller, Maximilian Thuermer and Ulrich Bruening, U of Heidelberg, DE

BioViz: An Interactive Visualization Engine for Microfluidic Biochips
P: Oliver Keszöcze[1] | A: Oliver Keszöcze[1], Jannis Stoppe[2], Robert Wille[3] and Rolf Drechsler[2]; [1]U of Bremen, DE; [2]DFKI and U of Bremen, DE; [3]Johannes Kepler U, AT, DFKI and U of Bremen, DE

RC3E: Design and Test Automatization in the Cloud
P: Patrick Lehmann | A: Patrick Lehmann, Oliver Knodel, Martin Zabel and Rainer G. Spallek, TU Dresden, DE

Retrascope: Toolkit for Analysis and Verification of HDL Designs
P: Sergey Smolov | A: Sergey Smolov, Alexander Kamkin and Mikhail Lebedev, Russian Academy of Sciences (RAS), RU

Continuous CHF Monitoring: An Integrated, Low-Power Platform for Continuous Congestive Heart-Failure Monitoring
P: Shahzad Muzaffar | A: Shahzad Muzaffar, Ibrahim (Abe) M. Elfadel and Jerald Yoo, Masdar Institute, AE

P04 P01 P01 P06 P05 P05 P09 P07 P07 P04 P09

Automotive System Prototypes

10:30 12:30 15:00 17:30
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UB01 UB02 UB03 UB04

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COMPSOC: Virtualising Control Applications on a Distributed CompSOC Platform
P: Kees Goossens | A: Kees Goossens, Eindhoven U of Technology, NL

P03

5G, 3D Design or IoT Prototypes

10:30 12:30 15:00 17:30
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UB01 UB02 UB03 UB04

P: Presenter | A: Author

LISA: Enabling Layered Interoperability for Internet of Things Through LISA
P: Behailu Shiferaw Negash[1] | A: Behailu Shiferaw Negash[1], Amir-Mohammad Rahmani[1], Tomi Westerlund[1], Pasi Liljeberg[1] and Hannu Tenhunen[2]; [1]U of Turku, FI; [2] U of Turku FI + Royal Institute of Technology (KTH), SE

6Ch-SDR-Platform: 6 Channel SDR Prototyping Platform for vehicle self-localization
P: Marko Rößler[1] | A: Marko Rößler[1], Ulrich Heinkel[1], Daniel Fross[1] and Ahmad El-Assaad[2]; [1]TU Chemnitz, DE; [2]Novero GmbH, DE

P04 P10

Wednesday, March 16, 2016

EDA Prototypes

10:00 12:00 14:00 16:00
12:00 14:00 16:00 18:00
UB05 UB06 UB07 UB08

P: Presenter | A: Author

LoopInvader: A Compiler for Tightly Coupled Processor Arrays
P: Alexandru Tanase | A: Alexandru Tanase, Michael Witterauf, Ericles Sousa, Vahid Lari, Frank Hannig and Jürgen Teich, U Erlangen-Nürnberg, DE

COSSIM: A Novel, Comprehensible, Ultra-Fast, Security-Aware CPS Simulator
P: Antonios Nikitakis | A: Antonios Nikitakis and Andreas Brokalakis, Technical U of Crete, GR

A Circuit Extraction Tool for Full Custom Designed MEMS Sensors
P: Axel Hald[1] | A: Axel Hald[1], Johannes Seelhorst[1], Mathias Reimann[1], Juergen Scheible[2] and Jens Lienig[3]; [1]Robert Bosch GmbH, DE; [2]Reutlingen U, DE; [3]TU Dresden, DE

DAC Generator: A DAC Stage Analog Circuit Generator for UDSM and FD-SOI Technologies
P: Benjamin Prautsch | A: Benjamin Prautsch, Sunil Rao, Uwe Eichler, Ajith Puppala and Torsten Reich, Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS, DE

CLaSH: Digital circuits in CλaSH
P: Christiaan Baaij | A: Christiaan Baaij and Jan Kuper, U of Twente, NL

AGAMID: A TLM framework for evaluation of hardware-enhanced many-core run-time management
P: Daniel Gregorek | A: Daniel Gregorek and Alberto Garcia-Ortiz, U of Bremen, DE

Hyperdimensional Computing for Text Classification: An Efficient Software Implementation
P: Fateme Rasti Najafabadi[1] | A: Fateme Rasti Najafabadi[1], Abbas Rahimi[2], Pentti Kanerva[2] and Jan Rabaey[2]; [1]Sharif U of Technology, IR; [2]U of California, Berkeley, US

CONTREP: A single-source framework for UML-based Modelling and Design of Mixed-Criticality Systems
P: Fernando Herrera | A: Fernando Herrera and Eugenio Villar, U of Cantabria, ES

D-VASim: Timing Analysis of Genetic Logic Circuits using D-VASim
P: Hasan Baig | A: Hasan Baig and Jan Madsen, Technical U of Denmark, DK

AHLS_Desync: Desynchronization Tool for High-Level Synthesis of Asynchronous Circuits
P: Jean Simatic | A: Jean Simatic, Rodrigo Possamai Bastos and Laurent Fesquet, TIMA Laboratory, FR

VisualNoC: Visualization Network-on-Chip Design Framework
P: Junshi Wang[1] | A: Junshi Wang[1], Letian Huang[1], Guangjun Li[1] and Axel Jantsch[2]; [1]University of Electronics Science and Technology of China, CN;[2]Technology U of Vienna, AT

eTeak: Asynchronous Dataflows Synthesis onto FPGAs Using the eTeak Framework
P: Mahdi Jelodari Mamaghani | A: Mahdi Jelodari Mamaghani, Jim Garside and Steve Furber, The U of Manchester, GB

RT-PowMods: Run-Time CPU Power Models from Real Data
P: Matthew Walker[1] | A: Matthew Walker[1], Stephan Diestelhorst[2], Andreas Hansson[2], Geoff Merrett[1] and Bashir Al-Hashimi1; [1]U of Southampton, GB; [2]ARM Ltd., GB

GRIP: Graph-Rewriting-Based IP-Integration (GRIP) - An EDA Tool for Software Defined SoC Design
P: Munish Jassi | A: Munish Jassi, Yong Hu, Jian Lyu, Daniel Mueller-Gritschneder and Ulf Schlichtmann, TU München, DE

InvadeSIM: A Simulator for Heterogeneous Multi-Processor Systems-on-Chip
P: Sascha Roloff | A: Sascha Roloff, Frank Hannig and Jürgen Teich, F.-Alexander-U Erlangen-Nürnberg, DE

t-RIDE : A Mobile-Health Neurodiagnostic System based on Spatio-Temporal P300 Monitoring: Design, Development and Test in vivo
P: Valerio Francesco Annese | A: Valerio Francesco Annese, Giovanni Mezzina and Daniela De Venuto, Politecnico di Bari, IT

Electro-Thermal Simulator for Chip Design
P: Vladyslav Ladonkin | A: Vladyslav Ladonkin and Juergen Scheible, Reutlingen U, DE

P03 P08 P01 P10 P09 P04 P03 P06 P08 P08 P02 P01 P01 P03 P04 P02 P02 P05 P05 P07 P04

Secure System Prototypes

10:00 12:00 14:00 16:00
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UB05 UB06 UB07 UB08

P: Presenter | A: Author

SRAM-based physical unclonable keys for BLE smart lock systems
P: Iluminada Baturone and Miguel Ángel Prada-Delgado[1] | A: Iluminada Baturone[1], Miguel Ángel Prada-Delgado[1], Alfredo Vázquez-Reyes[1], Laurentiu Acasandrei[2], Diego Fernández-Barrera[2] and Javier Prada-Delgado[2], [1]U of Seville, ES; [2]OCLOSE S.L., ES

P02 P07

Hardware Design & Test Prototypes

10:00 12:00 14:00 16:00
12:00 14:00 16:00 18:00
UB05 UB06 UB07 UB08

P: Presenter | A: Author

A-LOOP: AMP system with a dual-core ARM Cortex A9 processor with Linux operating system and a quad-core Leon3 processor with Linux Operating system, OpenMP library and hardware profiling system
P: Giacomo Valente | A: Giacomo Valente and Vittoriano Muttillo, Università Degli Studi Dell'Aquila, IT

ChImpAnC: Change Management using ChImpAnC
P: Jannis Stoppe | A: Jannis Stoppe, Martin Ring and Rolf Drechsler, DFKI and U of Bremen, DE

NeuroDSP: A Multi-Purpose Energy-Optimized Accelerator For Neural Networks
P: Jean-Marc PHILIPPE | A: Jean-Marc PHILIPPE, Alexandre CARBON and Renaud SCHMIT, CEA LIST, FR

Digitally Driven Top-Down Methodology for Mixed Signal Circuit Design
P: Markus Mueller | A: Markus Mueller, Maximilian Thuermer and Ulrich Bruening, U of Heidelberg, DE

BioViz: An Interactive Visualization Engine for Microfluidic Biochips
P: Oliver Keszöcze[1] | A: Oliver Keszöcze[1], Jannis Stoppe[2], Robert Wille[3] and Rolf Drechsler[2]; [1]U of Bremen, DE; [2]DFKI and U of Bremen, DE; [3]Johannes Kepler U, AT, DFKI and U of Bremen, DE

RC3E: Design and Test Automatization in the Cloud
P: Patrick Lehmann | A: Patrick Lehmann, Oliver Knodel, Martin Zabel and Rainer G. Spallek, TU Dresden, DE

Continuous CHF Monitoring: An Integrated, Low-Power Platform for Continuous Congestive Heart-Failure Monitoring
P: Shahzad Muzaffar | A: Shahzad Muzaffar, Ibrahim (Abe) M. Elfadel and Jerald Yoo, Masdar Institute, AE

Q27: Putting Queens in Carry Chains
P: Thomas Preußer | A: Th. Preußer, TU Dresden, DE

P05 P08 P09 P06 P09 P06 P04 P07

Automotive System Prototypes

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LLBMC / QPR-Verify: High-Precision Bounded Model Checking for Automotive Software
P: Carsten Sinz | A: Carsten Sinz, David Farago, Florian Merz and Reimo Schaupp, Karlsruhe Institute of Technology (KIT), DE

MCC: Contract-based automated integration for component-based critical systems
P: Johannes Schlatow | A: Johannes Schlatow, Marcus Nolte, Rolf Ernst and Markus Maurer, TU Braunschweig, DE

P10 P10 P07 P06

5G, 3D Design or IoT Prototypes

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LISA: Enabling Layered Interoperability for Internet of Things Through LISA
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P05

DATE 16

Booth University