Design and Analysis of Via-Configurable Routing Fabrics for Structured ASICs

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***Abstract*—This paper presents a simple method for design and analysis of a via-configurable routing fabric formed by an array of routing fabric blocks (RFBs). The method simply probes into an RFB rather than resorts to full-chip routing to collect some statistics for a metric used to qualify the RFB. We find that the trade-off between wire length and via count is a good metric. This metric has been validated by full-chip routing and used successfully to create better routing fabrics.**

Keywords-structured ASIC; regular fabric; via configurable; routing; design for manufacturity

I. INTRODUCTION

Structured ASIC emerged as a new design alternative [1-5] in a few years ago as designers tried to curtail the ever increasing design and manufacturing costs of integrated circuits (IC). Structured ASIC consists of prefabricated transistors and prefabricated masks for some metal layers. Designers can customize a few mask layers such as via layers between upper level metals to realize a circuit. Designers need only pay for a few customized masks and share the cost of prefabricated masks. As such, structured ASIC has a much lower non-recurring engineering (NRE) cost compared to conventional ASIC. A more prominent feature of structured ASIC is its layout regularity. A via-configurable structured ASIC consists of via-configurable logic block (VCLB) arrays and routing fabric block arrays [4-8]. Its layout regularity will not only simplify the set of restricted design rules [9], but also greatly enhance the effects of various reticle enhancement techniques for improving manufacturability [10-13]. It is encouraging to see that Jhaveri et al. [11-12] are able to achieve comparable timing and area utilization for an ARM926EJ implementation exploiting only a small set of layout primitives for forming regular layouts.

Routing is one of the most important tasks for designing a via-configurable structured ASIC. We need deal with two routing issues. One is routing per se and it is done by a structured ASIC router. The other is about designing a routing fabric which normally consists of regular routing fabric blocks (RFBs) formed by wire segments on upper metal layers. A structured ASIC router customizes a few via layers on a predefined routing fabric to implement connections among logic blocks. In the past, a few structured ASIC routers [7,14,15] were designed only for evaluating a structured ASIC technology. A more comprehensive structured ASIC router was presented in [16]. Some routing fabrics (fabric blocks) [4-6,14-17] were presented along with these works. Only the work in [16] investigates the issue of quantifying a routing fabric. However, none of the previous work discussed how to qualify a routing fabric and what constitutes a good routing fabric. Typically, we usually resort to full-chip routing for evaluating a routing fabric. This is a time-consuming process. Hence, we propose a simple method to qualify a routing fabric formed by repetitive RFBs. Our main contributions are as follows.

- Our method greatly simplifies the task of qualifying an RFB because we look into an RFB rather than a full-chip to determine the quality of a routing fabric.
- We illustrate a way of evaluating the influence of routing internal nets completely inside an RFB on the resource quantity provided by the underlying RFB.
- We find out that the trade-off between via count and wire length is an effective metric to evaluate an RFB quality.

This article is organized as follows. Section II gives a problem definition. Section III elaborates on how to design and analyze an RFB. Section IV conducts an experimental validation. Section V draws a conclusion.

II. PROBLEM DEFINITION

Our structured ASIC technology contains arrays of via-configurable logic blocks (VCLB) and via-configurable routing fabrics. In this work, we use a VCLB as shown on the left of Fig. 1 from [18] and a routing fabric containing arrays of routing fabric blocks (RFBs) formed by wire segments on M3 through M5. If an RFB refers to a particular layer such as M3, it is called M3 RFB. On the right of Fig. 1 shows part of an M3 RFB laid over a VCLB. An RFB usually has a size of an m-by-n VCLB array. For example, the RFB in Fig. 2 has a size of a 4-by-4 VCLB array, which contains M3, M4, and M5 RFBs. Now, we define our problem as follows.

Given a routing fabric which is formed by an array of routing fabric blocks (RFBs), determine whether the given routing fabric is better than other routing fabrics.

To the best of our knowledge, we are the first to investigate this issue. We virtually cannot solve this problem analytically because an RFB contains only predefined yet segmented wires. Hence, we will tackle this problem experimentally.

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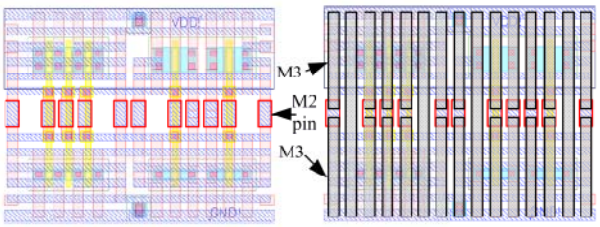

Figure 1. A VCLB (left) overlaid with part of M3 RFB (right).

III. Routing Fabric Design and Analysis

A. Routing Fabric Design Issues

There are three basic RFB design issues: layout design issue, wire length issue, and RFB size issue. The basic layout design principle is to avoid creating an isolated wire segment or a dangling wire segment. Layout design should consider many other things such as power strap deployment, pin accesses, etc. For example, metal fabric just right above a pin layer should be designed in such a way of easing pin access. As shown in Fig. 1, we lay two M3 wire segments on a track where there is a M2 pin for easing pin accesses from M3. Wire length issue is about the length of wire segments on an RFB. Long wire segments tend to leave a large unused part and thus increase total wire length whereas short wire segments tend to increase via count but result in smaller total wire length. This creates a difficult situation. A compromise between via count and total wire length seems unavoidable. Determining RFB size is a tricky problem, similar to the problem of determining global bin size for global routing. For simplicity, we assume in this work that an RFB is equivalent to a global bin. A side of a global bin in industrial practice typically encompasses 15 to 50 tracks [19]. In our work, 50 to 60 tracks, equivalent to a 4-by-4 VCLB array, are used because an RFB usually provides fewer available tracks than the nominal number of tracks on a side. Another minor issue is about using a heterogeneous routing fabric which employs different RFBs in different regions of a structured ASIC. In our structured ASIC technology, we use one RFB for core region and another RFB for IO to core region. For simplicity, we focus our study on RFBs in core region.

B. Routing Fabric Blocks (RFBs)

We study five RFBs, each of which consists of its own M3 RFB, M4 RFB, and M5 RFB. These five RFBs are respectively called *BaseRF*, *New1RF*, *New2RF*, *XbarRF*, and *eASICRF*. We have considered the issues presented in III.A while designing these RFBs. Figure 2 shows the layout of *BaseRF*. BaseRF was originally used in [16]. Short jumpers on M4 RFB are used to connect vertical wires on M3 and M5 whereas those on M5 RFB are used for connecting horizontal wires on M4. Besides, BaseRF has a long wire running across three RFBs. Figure 3 shows *New1RF*, derived from chopping some long M4 wires in BaseRF into some shorter wires. Accordingly, we need also modify M5 RFB by adding some jumpers at the places where the long wires are broken. M3 RFB is the same as that for BaseRF. Figure 4 shows *New2RF*, obtained by replacing some short vertical wires of M3 RFB and M5 RFB of New1RF with long vertical wires. Figure 5 shows *XbarRF* formed by short wires on adjacent metal layers neatly orthogonal to each other. Figure 6 shows *eASICRF* [20]. We have slightly modified the original eASIC's RFB by adding some jumper wires on M4 RFB and M5 RFB to improve accessibility to the internal wires in eASICRF. Note that eASICRF also employs the M3 RFB shown in Fig. 2.

C. Routing Resource Analysis

We employ the statistical approach presented in [16] for analyzing an RFB experimentally. Given an RFB, we statistically find out the number of distinct routes, each of which starts from a specific side and terminated at any of the other three sides. We repeat this task for a specific side a

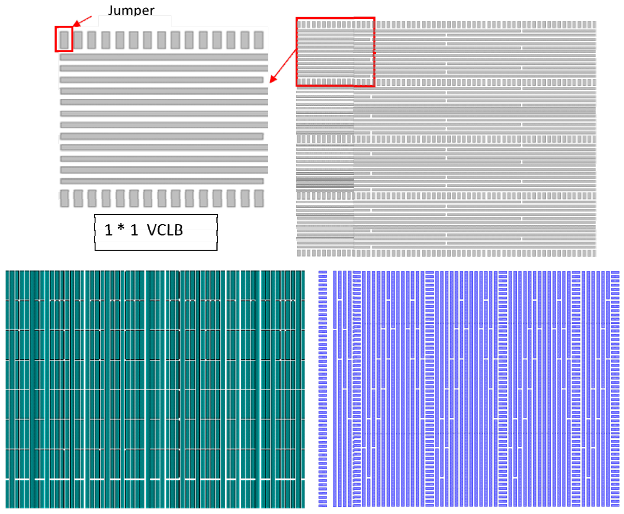

Figure 2. ***BaseRF***, M4 RFB (top), M3 RFB (lower left), and M5 RFB.

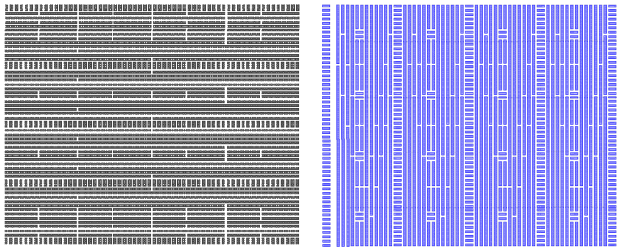

Figure 3. New1RF, M4 RFB (left) and M5 RFB.

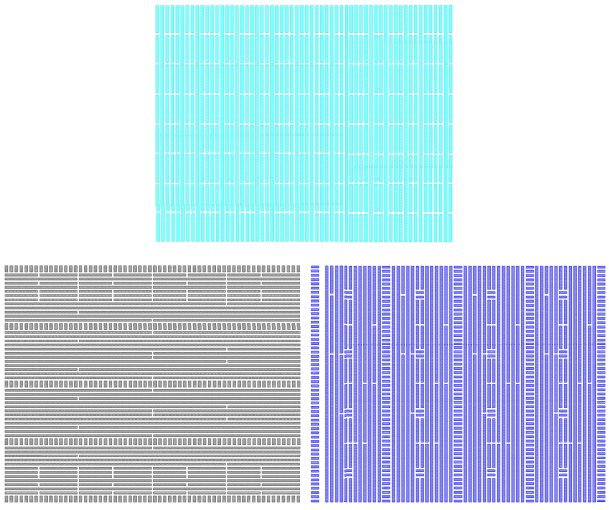

Figure 4. New2RF, M3 RFB (top), M4 RFB (lower left), and M5 RFB.

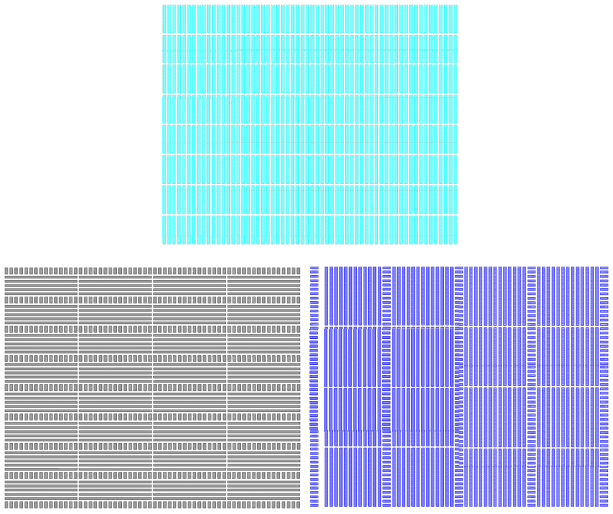

Figure 5. XbarRF, M3 RFB (top), M4 RFB (lower left), and M5 RFB.

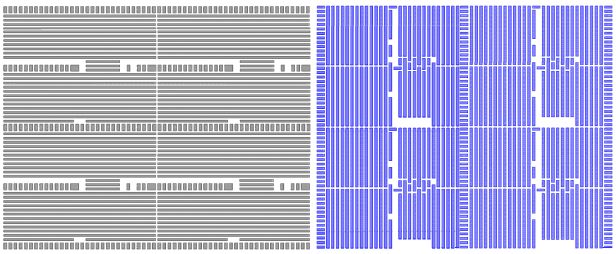

Figure 6. eASICRF, M4 RFB (left) and M5 RFB.

large number of times, said 3000 times in our case. We thus have statistics about the maximum, average, and minimum numbers of routes starting from a side. We perform the above task for each of the four sides of an RFB. Table I shows the number of routes supplied by the five RFBs studied in this work. Each entry has a form of Max/Ave/Min which respectively gives the maximum, average, and minimum number of routes. The sum of the average number of routes on the four sides of an RFB is denoted by TR_F. The normalized number of routes with respect to that provided by XbarRF is denoted by TRN_F. As one can see, XbarRF provides more routes starting from the north or south side. However, the above analysis does not consider the influence of routing the internal nets completely inside an RFB. In an RFB with a size of a 4-by-4 VCLB array, the number of internal two-pin nets can be up to 12. In this work we modify the statistical approach in [16] to consider internal nets. Table II shows the average number of routes reduced per internal net. It turns out that the reduction in the number of routes per internal net is a good indicator for gauging an RFB's quality.

TABLE I. ROUTING RESOURCES

	BaseRF	*New1RF*	*New2RF*	*XbarRF*	*eASICRF*
N	50/41.99/33	54/47.06/38	55/47.80/37	59/51.69/43	51/43.54/35
S	50/41.77/34	55/47.28/39	56/48.42/38	59/50.86/40	50/40.50/33
W	39/33.49/27	44/39.58/34	44/40.40/35	42/38.93/35	45/40.08/34
E	40/35.23/30	44/39.66/34	45/40.37/36	42/38.92/35	45/39.98/33
TR_F	152.48	173.58	176.99	180.4	164.1
TRN_F	0.85	0.96	0.98	1.00	0.91

TABLE II. REDUCTION IN ROUTING RESOURCE PER INTERNAL NET

	BaseRF	*New1RF*	*New2RF*	*XbarRF*	*eASICRF*
N	0.40	0.32	0.34	0.56	0.68
S	0.43	0.34	0.37	0.55	0.58
W	0.49	0.49	0.55	0.71	0.72
E	0.51	0.49	0.54	0.69	0.72
Total	1.83	1.64	1.80	2.51	2.70

D. Metrics for RFB Qualification

The total number of routes supplied by an RFB is an important metric for RFB qualification. However, simply looking into the number of routes provided by an RFB is not enough to determine an RFB's quality because the routes may use excessive numbers of vias or have large wire lengths. Hence, we need also consider the number of vias employed by the routes. Table III gives the sum of the average number of vias per route (denoted by TV_F) and the sum of the average wire length per route (denoted by TWL_F). It also gives their normalized via counts and wire lengths with respect to that for XbarRF, denoted by TVN_F and TWLN_F respectively. We have three sets of data in Table III, respectively collected from from routing only the first 10, 20, and all the routes. The reason why we present the data for the first 10 and 20 routes is because the majority of RFBs on a chip use much fewer routes than the maximally allowable routes. Looking into Table III, we find that XbarRF has the smallest TWL_F and the largest TV_F. Hence, the data for XbarRF can serve as a good reference for calculating the trade-off between wire length and via count. We define a metric based on this trade-off as follows.

$$\text{Metric\_F(MRF)} = \frac{\text{TVN\_F(XbarRF)} - \text{TVN\_F(MRF)})}{\text{TWLN\_F(MRF)} - \text{TWLN\_F(XbarRF)}} \quad (1)$$

Where TVN_F(MRF) denotes the normalized via count incurred by an RFB called MRF which can be either of the five RFBs except XbarRF. TWLN_F(MRF) is defined similarly. Metric_F(MRF) is a trade-off between wire length and via count. A larger number is better. Based on Metric_F of the first 10 and 20 routes shown in Table III, New1RF ranks first, New2RF ranks second, eASICRF ranks third, and BaseRF ranks fourth. However, eASICRF becomes more competitive if ranking is based on the third set of data.

TABLE III. METRICS DEFINED BY VIA COUNTS, WIRE LENGTHS, AND ROUTES OBTAINED FROM ROUTING A SINGLE RFB

		BaseRF	*New1RF*	*New2RF*	*XbarRF*	*eASICRF*
First 10 routes	**TV_F**	18.6	26.32	22.61	42.51	24.86
	TVN_F	0.44	0.62	0.53	1.00	0.58
	TWL_F(um)	1185.8	1021.6	1061.8	896.6	1040.2
	TWLN_F	1.32	1.14	1.18	1.00	1.16
	Metric_F	1.74	2.73	2.54	1.00	2.59
	Rank	4	1	2	5	3
First 20 routes	**TV_F**	18.82	26.14	22.22	42.35	24.86
	TVN_F	0.44	0.62	0.52	1.00	0.59
	TWL_F(um)	1198.95	1029.7	1071.4	897.05	1054.65
	TWLN_F	1.34	1.15	1.19	1.00	1.18
	Metric_F	1.65	2.59	2.45	1.00	2.35
	Rank	4	1	2	5	3
All routes	**TV_F**	20.89	27.85	23.04	44.21	26.84
	TVN_F	0.47	0.63	0.52	1.00	0.61
	TWL_F(um)	1208.58	1074.09	1109.84	900.93	1067.02
	TWLN_F	1.34	1.19	1.23	1.00	1.18
	Metric_F	1.54	1.93	2.07	1.00	2.13
	Rank	4	3	2	5	1

IV. EXPERIMENTAL VALIDATIONS

We will validate that Metric_F is indeed effective by performing full-chip routing for some ITC99 benchmark circuits using our structured ASIC technology. A router Rover [16] routes a circuit using the underlying routing fabric. Table IV shows Metric_C that corresponds to Metric_F obtained from exploring an RFB. Since Metric_C is obtained from full-chip routing, a suffix C is used. A larger Metric_C is better. Hence, New1RF would rank first and New2RF ranks second. Comparing such a ranking with that based on the data in Table III, the ranking of New1RF and New2RF is consistent. However, the ranks of BaseRF and eASICRF are comparable. The reason for this is that BaseRF has a much smaller reduction in routing resource per internal net as shown in Table II. Generally, Metric_F used for ranking RFBs is effective because the ranking based on full-chip routing is quite consistent with that based on routing a single RFB with less than 50% (the first 20 routes) of the total routes being routed.

One more issue yet to be investigated is about routability. Will chips based on New1RF be more routable than those based on New2RF? This might not be true if we look into Table I which shows that New2RF offers more routing resources than New1RF does. We run some experiments to study this issue. What we do is to set as a higher core utilization as possible for floorplanning to make as a smaller chip as possible so that the routing resources on a chip can be reduced to a minimum. In this way, we hope that we would create some failed nets during routing. We test the above approach for the three largest designs. Table V shows the routability check results. New1RF and New2RF do not have a failed net. The runtimes taken by Rover for them are also smaller. This implies that New1RF and New2RF indeed enable higher routability. Note that Metric_C's values for New1RF are still larger than that for New2RF. Also note that failed nets could be possibly due to using a poor routing tool.

TABLE IV. UISNG METRIC_C TO VALIDATING METRIC_F

	BaseRF	*New1RF*	*New2RF*	*XbarRF*	*eASICRF*
b14	2.11	**7.67**	3.10	1.00	2.07
b15	2.35	**5.00**	3.50	1.00	2.58
b17	1.85	**3.83**	2.91	1.00	1.69
b18	2.41	**5.91**	4.19	1.00	2.64
b19	2.05	**4.80**	3.30	1.00	2.07
b20	1.80	**5.25**	2.73	1.00	1.53
b21	1.85	**4.40**	2.91	1.00	1.80

TABLE V. ROUTABILITY CHECKS

		BaseRF	*New1RF*	*New2RF*	*XbarRF*	*eASICRF*
b17	**Failed nets**	1	0	0	1	4
	Metric_C	2.06	**5.31**	3.46	1.00	1.96
	Runtime	50m	17m	17m	33m	2h10m
b18	**Failed nets**	2	0	0	1	438
	Metric_C	2.09	**5.91**	3.55	1.00	2.02
	Runtime	2h10m	56m	53m	1h10m	5h08m
b19	**Failed nets**	0	0	0	0	0
	Metric_C	2.14	**6.39**	3.72	1.00	2.15
	Runtime	1h10m	55m	51m	1h11m	1h15m

V. CONCLUSIONS

This paper presents an approach to design and analysis of via-configurable routing fabric. A metric based on the trade-off between wire length and via count is used along with the degree of reduction in routing resource per internal net to determine which RFB is better than the others. The proposed method and metric enable us to design a better routing fabric.

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