Towards A Wireless Medical Smart Card

(Invited Paper)

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***Abstract*—Wireless data transmission has become an integral part of modern society and plays an increasingly important role in health care. Technology scaling is continuously increasing wireless data rates, thus allowing for more flexible high-speed interfaces, e.g., between medical imaging equipment and mass storage devices. However, one issue remains: The power consumption of high-speed wireless transceivers and non-volatile memory grows with the data rate. This prevents from innovations using these high-speed wireless interfaces in ultra-low power (or even energy-passive) medical equipment that can be used by patients without a heavy power source. Clear efforts are required to close this gap, i.e., to provide high-speed wireless solutions with reduced energy consumption per transmitted bit. As a very example, this work presents the concept of a wireless medical smart card that combines near field communication for authentication and low-speed signaling together with a 60GHz interface for fast wireless memory access in a single patient-owned ID card. The basic architecture, functionality and prospects of the concept are discussed. A power budget is calculated based on state-of-the-art technologies. To put the concept into practice, some necessary developments for a reduction of the power consumption are outlined.**

I. Introduction

Wireless data transmission has seen great success during the last decades. It has led to countless applications that improve everyday life, and it is also finding its way into various health care applications. Latest technology advancements are enabling short-range wireless interfaces with data rates of multiple Gbps at a power consumption that is still reasonable for battery driven devices. As a continuation of these advancements, this paper discusses the prospects and challenges of a wireless medical smart card which is not just a patient-owned contactless ID card, but which can also store the patients medical record as well as any kind of medical image, audio or video data of the patient.

Several concepts for medical smart cards have been under consideration in recent years. An early discussion of general requirements can be found in [1]. Most solutions are not contactless and have a memory size which is less than 1Gbyte. Clearly, the latter will not be sufficient to store a multitude of high-definition images or video data files on the card. Another common property is that existing concepts use only a single interface for patient identification and to transfer the patient's medical data. Most of these concepts build on a Universal Serial Bus (USB) interface (see for example [2] and [3]). A recent comparison of commercially available health record devices with USB interface (not all of them having the size of a credit card) can be found in [4]. With the advancements of wireless technology it may become possible to achieve the same functionality (and even higher data transfer rates) with a high-speed wireless interface and inductive energy transfer, thus enabling a high-performance contactless medical smart card. A discussion of the technical feasibility of this concept is in the focus of this paper. The proposed concept combines inductive coupling with a near field communication (NFC) interface for low-speed data transfer (e.g. for patient authentication) and a 60GHz interface for high-speed wireless data transfer to/from a large non-volatile memory on the card.

One alternative to storing the patient's medical data on a personally-owned device is centralized data storage with some kind of network infrastructure (e.g. the Internet) to let authorized health care professionals access the patient's data from different places. However, privacy will then be a major concern of patients [3]. Furthermore, the data will hardly be accessible without a broadband network access. The latter can be critical in rural areas and at less-developed places, where a personally-owned smart card with all data stored on a sufficiently large memory is clearly favorable. Other advantages of a completely wireless, energy-passive smart card are its mechanical robustness, its user-friendliness and its infinite lifetime without an internal power source.

The remainder of the paper is organized as follows: Section II describes the basic architecture and the general functionality of the wireless medical smart card. The necessary hardware modules are discussed in more detail in Section III. Based on a rough calculation of a power budget with state-of-the-art technologies, it is shown that one of the main technological challenges is the power consumption of the card's non-volatile memory. Section IV concludes the paper with a summary of research directions and future developments that are required to bring the wireless smart card concept into practice.

II. The Technical Concept

The anticipated application of a wireless medical smart card is depicted in Fig.1. The smart card is an energy-passive device with a large memory, which can be accessed through a remote station that is connected to a power supply and a personal computer (PC) or laptop. The smart card will have to be placed on top of the remote station with a maximum distance of 10cm. This ensures that a sufficient amount of energy can be transferred from the remote station to the smart card by means of inductive coupling. For this purpose, both devices have an

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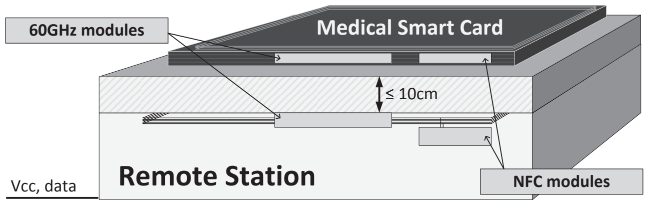

Fig. 1: Application scenario.

integrated coil, which is well-known for conventional NFC cards. The remote station is commonly referred to as proximity coupling device (PCD), and the energy-passive card is known as proximity integrated circuit card (PICC). The proposed medical smart card and the remote station have two wireless data interfaces: a low-speed NFC interface, which operates on the inductive coupling and an additional 60GHz interface for high-speed data transfer, which will be controlled through the NFC interface. The intended data rate of the 60GHz interface is 5Gbps. The architecture and functionality of the wireless medical smart card are described in the following.

A. Principle Architecture

Fig. 2 illustrates the functional units of the wireless medical smart card: a coil, a power supply unit, non-volatile memory of several GBytes, an NFC module and a 60 GHz module. The latter consists of an analog frontend part with patch antennas and a dedicated digital baseband processor. To conform with the ISO 7810 ID-1 standard ("credit card" size), the card has a length of 85.6 mm, a height of 54 mm and a thickness of 0.76 mm [5].

Each of the functional units may require a different supply voltage that has to be generated by the power supply unit: Vcc_{Mem} for the memory, Vcc_{NFC} for the NFC module, Vcc_{BB} and Vcc_{AFE} for the 60GHz module. To minimize the power consumption of the card, it is reasonable to turn on the memory and the 60GHz module of the card only by request. This is controlled by the NFC module, which will always be turned on as long as enough energy is coupling into the card's coil.

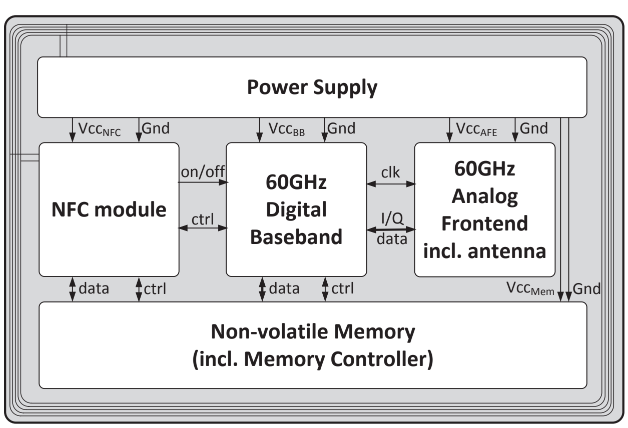

Fig. 2: Principle architecture.

B. General Functionality

Regarding the card's capabilities for wireless data transfer, there are three main use cases, as illustrated in Fig. 3. In general, the card should be accessible for authorized medical staff, paramedical staff and the patient. To ensure privacy of the stored data, some type of access control will be required. Parts of the memory should be accessible only for certain user groups. This can be realized with a user authentication based on the low-speed NFC interface. The NFC interface can also be used to retrieve general information and textual medical records of the patient. The 60GHz interface is intended for transmitting larger amounts of data to/from the card's memory, e.g., high-definition image, audio or video data of the patient.

To enable an energy-passive device that can obtain the required energy through inductive coupling, it is important that the design aims at lowest power consumption. For the high-speed data transfer, this can be approached with a separation of low-rate control signaling using the NFC interface (e.g. the protocol stack of the wireless memory access) and wideband transmission of the true data using the 60GHz interface. This minimizes the usage of the 60GHz modules, which are more power hungry. The respective procedure of a high-speed data transfer is illustrated in Fig. 4. A memory write access is considered, i.e., the card operates in receive mode. At first, only the NFC module is turned on. The request for the memory access is always initiated by the remote station (PCD). If the smart card (PICC) accepts the request, which requires a valid user authentication, protocol data will be exchanged and the memory as well as the receiver part of 60GHz unit will be turned on. Then, packets of the true data will be sent over the 60GHz interface and stored in the respective part of the card's memory. Once the data transmission has been completed, the non-volatile memory and the 60GHz interface of the card will be turned off, and the NFC interfaces finalizes the access. In

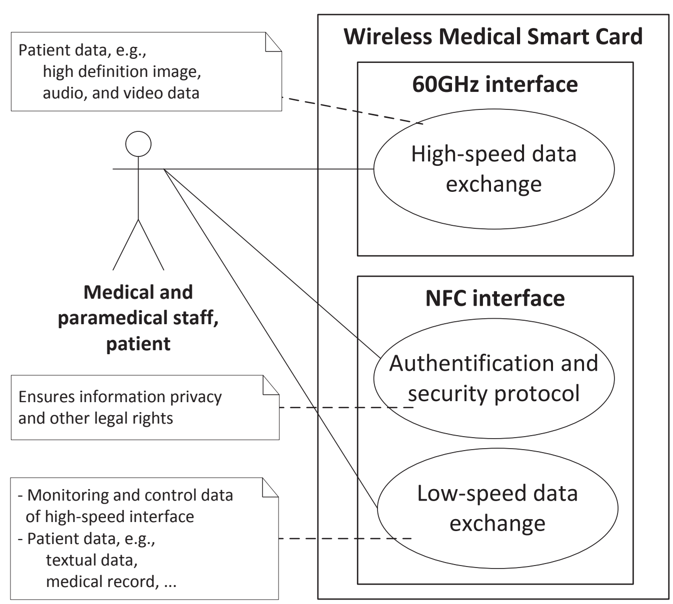

Fig. 3: Main use cases.

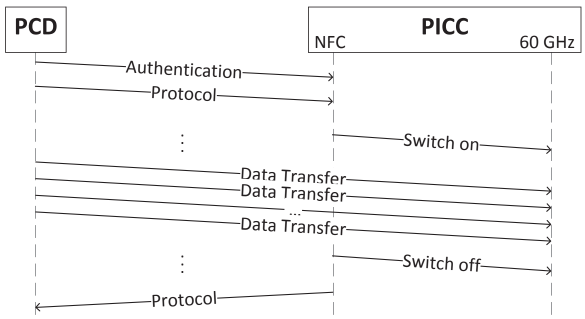

Fig. 4: Sequence diagram for a high-speed data transfer (write access).

case of a read access, the transmitter part of the card's 60GHz module will be turned on, and data will be transmitted from the card's memory to the remote station. In both cases, redundancy checks can be performed at the receiver side to confirm an error-free reception or request a retransmission.

III. Hardware Modules and Power Budget

The wireless smart card concept strongly relies on the fact that enough energy is provided through the inductive coupling to run the NFC interface, the 60GHz interface and the memory, respectively. To assess the feasibility of the concept with a rough power budget, this section reviews state-of-the-art solutions for the different hardware modules.

A. Inductive Coupling: Power Supply and NFC Interface

The power supply unit, which is connected to the coil and comprises circuits for voltage transformation and protection, is one of the key elements of the energy-passive smart card. It has to provide all the energy that is consumed by the smart card from the magnetic field that is generated at the remote station (PCD). The inductive energy transfer relies on the principle of a loosely coupled transformer. Inductive coupling factors between PCDs and PICCs are typically in the range of 1% to 20% [6]. The coupling requires a high current level, which is achieved by resonators in the PCD and PICC that have the same frequency f_r. The quality factor Q of the resonators has an influence on the bandwidth $B_\mathrm{NFC} = f_\mathrm{r}/Q$ of the NFC interface, which is operating on top of the inductive energy transfer [7]. A high Q typically allows a good energy transfer but only at the price of smaller NFC data rates and vice versa. Hence, the NFC data rate and the energy that can be transferred have to be well adapted to the smart card requirements. A standard resonator frequency is $f_\mathrm{r} = 13.56\,\mathrm{MHz}$. Then, cards of ISO 7810 ID-1 size have coils with 3 to 10 winds and work with magnetic field strengths on the order of 1.5 to $7.5\,\frac{A}{m}$ [5].

Fluctuations of the induced voltage, which may arise from distortions or slight variations of the distance between the PCD and PICC, have to be taken into account for the power supply unit of the PICC. Therefore, a voltage protection circuit is most often attached to the impedance matching network of the coil. A voltage converter follows in the next stage of the power supply unit. It generates the different required DC voltages of the PICC. The modulated amplitude of the NFC interface is only a small fraction of the signal swing in the coil. It is typically 80 dB below the signal swing of the resonant signal which is intended for the energy transfer. To separate between both signals, the NFC data transmission typically uses two sidebands that can be bandpass filtered at the receiver and then demodulated.

Following the ISO/IEC 14443 standard for inductive coupling with a maximum distance of 10cm between the PCD and PICC, the power that can be transferred is at most 150mW. The standard also includes a definition of the required communication layers for an NFC data transmission. A data rates of up to 424kbps can be achieved. Integrated NFC chips that support this standard, such as NXP's PN512 [8], typically have a power consumption on the order of 50mW.

B. 60 GHz Analog Frontend and Digital Baseband Processor

The 60GHz frequency band provides an unlicensed bandwidth of up to 9GHz, depending on the country's frequency regulations. Most existing hardware solutions for high-speed data transmission at 60GHz use a bandwidth of 2.16 GHz or 4.32 GHz, according to the channelization plans of the evolving 60GHz standards [9] [10]. A number of low-power CMOS-integrated 60GHz transceiver frontends has been designed and published in recent years. However, to the best knowledge of the authors, a monolithic transceiver frontend that combines the radio frequency components and the functionality of the digital baseband processing is not yet available. Hence, a reasonable estimate on the power consumption can only be made for a hybrid 60GHz module that consists of an analog frontend part and a digital baseband processor.

The 60GHz radio link between the medical smart card and a remote station accessing the card will be a line-of-sight link without multi-path propagation. The 60GHz data transmission can hence use single-carrier modulation techniques without channel equalization. This simplification does inherently solve one of the main design issues of wideband transceivers, i.e., the coarse resolution of wideband data converters. In fact, it has been shown in [11] and [12] that low-resolution data conversion and low-order single-carrier modulation are most energy efficient for wideband line-of-sight transmission. Fully-integrated 60GHz CMOS transceiver frontends that have been designed for low-order single-carrier modulation and low-resolution data converters are, e.g., reported in [13] and [14]. The power consumption of these designs ranges from 100mW to 190mW to achieve data rates on the order of 5Gbps. The power consumption depends on the particular design and on the operation mode (transmit or receive). In transmit mode, major parts of the power are consumed by the transmit power amplifier, which is in [13] and [14] designed for a wireless coverage above 10cm. This is not required for a wireless medical smart card, which implies that the power consumption of an optimized 60GHz frontend might be less than the values stated above. Irregardless of this fact, the power consumption of a state-of-the-art 60GHz analog frontend in a wireless smart card can be well estimated as 150mW (1).

(1) The power consumption estimates given in this paper are rounded to the nearest multiple of 50mW.

To assess the power consumption of a 60GHz digital baseband processor that supports data rates of 5Gbps, the design proposed in [15] and [16] is considered. It consists of a transmitter and receiver data path as shown in Fig. 5. Both data paths are based on a strongly parallelized, linear data flow structure. They are clocked at 108MHz. In transmit mode, data words of 64 bit are read from the memory and fed into 64 parallel convolutional encoders. They generate two 96-bit output words, which are de-multiplexed according to a puncturing pattern and further processed by a differential QPSK (DQPSK) modulation unit. A framing module adds a preamble and an encoded signaling field to each data frame. At each clock cycle, 32 bits of this frame are forwarded to each of the two parallel-to-serial converters (1-bit data converters) that interface the analog frontend. In receive mode, the receiver data path realizes complementary functionality. 64 parallel Viterbi decoders are used to decode the received data streams with a data rate of 5 Gbps. Further information and a detailed explanation of an FPGA implementation of this digital baseband design can be found in the references mentioned above. Based on the FPGA implementation, it is possible to assess the power consumption of the transmitter and receiver data paths, using an early power consumption estimator of ALTERA [17]. The obtained estimates are scaled down from 65 nm-CMOS FPGA (ALTERA Stratix III) technology to 65 nm CMOS standard cell ASIC technology according to [18]. A factor of 12 has been considered for the dynamic power consumption, and the static power consumption has been scaled down by a factor of 50. Thus, the total power consumption of an ASIC that comprises both data paths would be on the order of 350mW. The transmitter data path would consume only around 50mW, whereas the receiver data path would consume 300mW, which is mostly due the parallel Viterbi decoders. The power consumption of any controllers is neglected in these estimates.

It is important to note that almost 60% of the power consumption of the transmitter data path and even 70% of the power consumption of the receiver data path are due to the encoding and decoding, respectively. Hence, if one could get along without encoding and decoding on the smart card, the power consumption of the 60GHz interface could be significantly reduced.

C. *Non-volatile Memory*

Flash technology is considered to estimate the power consumption of state-of-the-art non-volatile memory. Assuming a memory access data rate of 5Gbps, the typical power consumption of today's Flash solid-state disks (SSDs) is on the order of 20W [19]. This is clearly unreasonable for the proposed wireless smart card concept. Phase change memory (PCM) can be considered as the most promising and mature technology for reducing the power consumption of non-volatile memory. PCM prototypes with a feature size of 3nm have already been successfully fabricated [20]. Aiming at a reduced cost-per-bit of PCM, multilevel-cell (MLC) storage has recently been introduced with modulation coding. The MLC PCM is 100 times faster with significantly improved reliability as compared to today's Flash devices [21]. For an access data rate of 5Gbps and current PCM technology, PCM SSD can be projected to reach a power consumption of about 150mW for read access and 1500mW for write access [19]. Even more recently, a significant reduction of the power consumption has been demonstrated using carbon nanotubes (CNT) as electrodes in PCM. This will allow to lower the memory programming currents to less than 10uA, i.e., two orders of magnitude less than of state-of-the-art PCM [22]. In addition, CNTs enable a 7 nm^2 contact area, which is at least one order of magnitude lower than in conventional memory cells [23]. Hence, CNTs are showing an excellent power reduction and scaling potential.

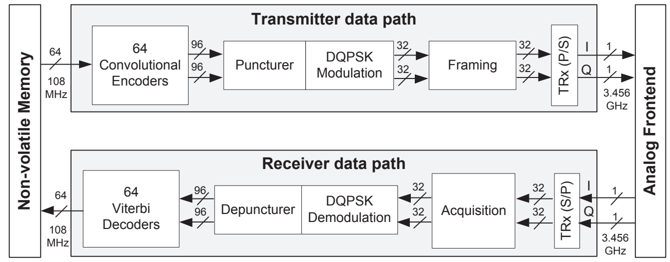

Fig. 5: 5Gbps digital baseband transmitter and receiver data paths.

D. *Overall Power Budget*

Summarizing the power consumption of the individual smart card units, the following rough power budgets can be calculated for a high-speed data transfer to/from the card's memory:

Receive mode (memory write access):

- NFC unit: 50mW
- 60 GHz analog frontend: 150mW
- 60 GHz digital baseband: 300mW
- Non-volatile memory (PCM): 1500mW
- Total power consumption: 2000mW

Transmit mode (memory read access):

- NFC unit: 50mW
- 60 GHz analog frontend: 150mW
- 60 GHz digital baseband: 50mW
- Non-volatile memory (PCM): 150mW
- Total power consumption: 400mW

The overall power budget is also illustrated in Fig. 6. Comparing the values of the estimated total power consumption to the power that can be provided through inductive coupling (150 mW), it has to be concluded that the wireless smart card concept is not yet feasible with state-of-the-art technologies. The estimated power consumption for a high-speed wireless data transfer exceeds the power that can be made available through inductive coupling by 250mW (167%) in transmit mode and even by 1850mW (1233%) in receive mode. In both modes, large parts of the power are consumed by the non-volatile memory. This is most interesting, as the high-speed 60GHz interface is not the only limiting factor. That is, even when the power consumption of the high-speed wireless

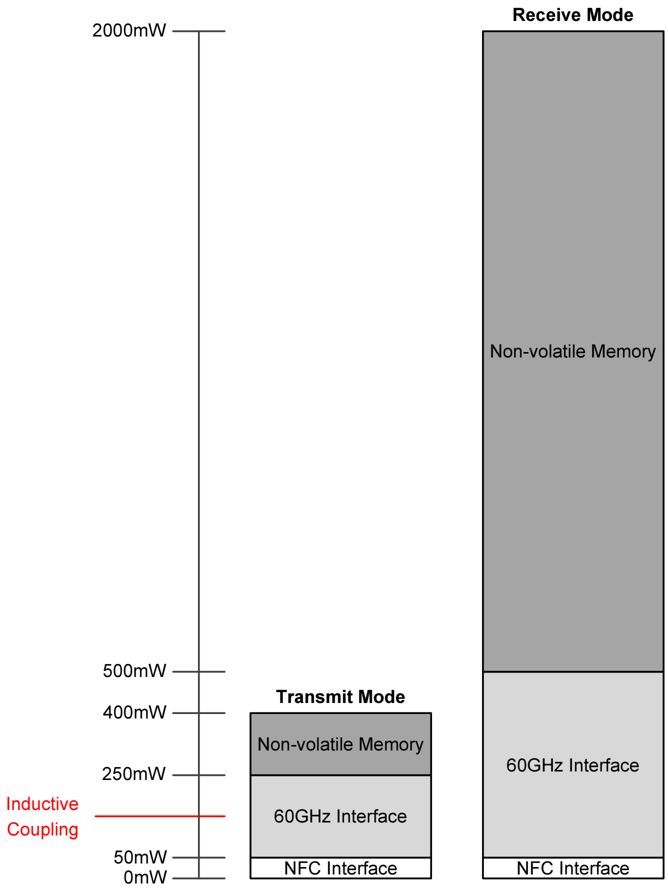

Fig. 6: State-of-the art power budget: transmit and receive mode.

interface could be significantly reduced by CMOS technology scaling or architecture simplification, the concept would still remain infeasible due the power consumption of the memory. Hence, to enable the concept, either a wired power supply or further significant technology improvements are required.

IV. Conclusions

This paper has presented the concept of an energy-passive smart card that has a large memory to store the medical data of a patient. The concept combines energy-transfer through inductive coupling with an NFC interface for authentication and low-speed data transmission and a 60GHz interface for high-speed memory access at a rate of 5Gbps. The feasibility of the concept with state-of-the-art technologies has been discussed from a power budget perspective. It has been found that not only the power consumption of the 60GHz interface would exceed the maximum power that can be provided through inductive coupling. It is mainly the power consumption of the non-volatile memory which makes the concept infeasible today. Considering a maximum power dissipation of 150mW to achieve a data rate of 5Gbps, an energy consumption of 30pJ per transmitted data bit could be allowed at most. Hence, it is not only reasonable to further increase wireless data rates while keeping the power dissipation as of today's circuits, which will lead to an energy consumption on the order of 1pJ per transmitted bit [24]. Instead, clear efforts are required to achieve the same improvement of energy efficiency also for (slightly) lower data rates. Thus, a variety of promising wireless applications can be made feasible in practice.

In particular for reducing the power consumption of non-volatile memory, CNT technology appears to be a promising candidate to satisfy the demanding requirements in 5 to 10 years from now.

A very promising solution to limit the power consumption of the 60GHz modules of the smart card is to omit the encoder and decoder in the data paths of the digital baseband processing. That is, it is possible to reduce the 60GHz digital baseband processing on the smart card to the functionality of detecting / transmitting encoded data which is written to / read from the card's memory, while all parts of the encoding and decoding are performed at the remote station. In other words, in receive mode, the received data is just written to the card's memory without decoding. Similarly, in transmit mode, the data which is read from the memory (and which has been encoded at the remote station that sent the data to the card) are just transmitted without further encoding. This simplification of the 60GHz interface comes at the cost of a larger memory usage and higher memory access rate for the same amount of information to be stored on the card, because the stored data remains encoded. The increase in memory usage and access rate can be calculated as $1/R - 1$, where R denotes the code rate. For example, in case of $R = 3/4$, the memory access rate and capacity would have to be increased by 33%. This increase of memory access rate and capacity will in turn lead to a higher power consumption of the memory. Hence, it has to be carefully traded-off with the power savings that can be expected from the simplification of the 60GHz interface. Future work will have to evaluate the power savings and the performance of the data transfer for this modified smart card concept in more detail.

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