Fixed Origin Corner Square Inspection Layout Regularity Metric

Marc Pons*, Marc Morgan† and Christian Piguet†
*Universitat Politècnica de Catalunya, Electronic Engineering
†CSEM SA - Centre Suisse d'Électronique et de Microtechnique

***Abstract*—Integrated circuits suffer from serious layout printability issues associated to the lithography manufacturing process. Regular layout designs are emerging as alternative solutions to help reducing these systematic subwavelength lithography variations. However, there is no metric to evaluate and compare the layout regularity of those regular designs and there is no methodology to link layout regularity to the reduction of process variations. In this paper we propose a new layout regularity metric called Fixed Origin Corner Square Inspection (FOCSI). We also provide a methodology using the Monte Carlo analysis to evaluate and understand the impact of regularity on process variability.**

I. Introduction

Optical lithography manufacturing process needs new solutions to manufacture integrated circuits at low cost [1]. 193 nm Argon Fluoride light sources are still used for the technology nodes of 32 nm and 22 nm resulting in geometrical layout variability that leads to variations on the electrical characteristics of the devices and interconnections. Lithography enhancement techniques like subresolution assist features, double patterning or optical proximity correction improve layout patterns fidelity at the Rayleigh's optical resolution limit. Alternating phase shift mask and off-axis illumination can help going beyond this resolution limit. However, these techniques are computationally expensive and time consuming for huge circuits with arbitrary layout patterns [2].

This issue is addressed by means of new design for manufacturability techniques. In particular, regular layout designs with a reduced amount of layout patterns and with predictable layout neighborhood show to be highly beneficial [3]–[5]. However, there is a tradeoff that must be studied between area, delay, energy consumption and the regularity imposed. Usually regular techniques offer worse area, delay and energy consumption than the non-regular design approaches but, according to the degree of regularity, they reduce cost and time associated to lithography enhancement techniques and therefore systematic yield loss. Area is measured directly from the layout design, and delay and energy consumption can be predicted by simulation. However, there is not a clear method to measure layout regularity nor its impact on variability.

From the layout designers point of view, the measure of the layout regularity of their designs can be a useful information to adjust and optimize in a comprehensive way the degree of layout regularity while considering the energy, delay and area tradeoffs. This way designers can also compare a pair of layouts in terms of regularity.

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In this paper we propose a new layout regularity metric called FOCSI based on [6] that quantifies regularity allowing an accurate, deterministic and unambiguous comparison of layout designs. Then, we propose a methodology using the Monte Carlo analysis to use FOCSI results to evaluate the benefits of layout regularity in terms of variability.

The structure of the paper is as follows. In section II we present the problem addressed, we provide a definition of regularity and we propose and formulate FOCSI layout regularity metric from the single layout layer to the complete layout. In section III we briefly describe the standard cell libraries that we use for our regularity measurements and we provide the results obtained for the ISCAS'85 benchmark circuits. In section IV we present the methodology using FOCSI results and the Monte Carlo analysis to evaluate the benefits of layout regularity in terms of variability. Finally, in section V we provide conclusions.

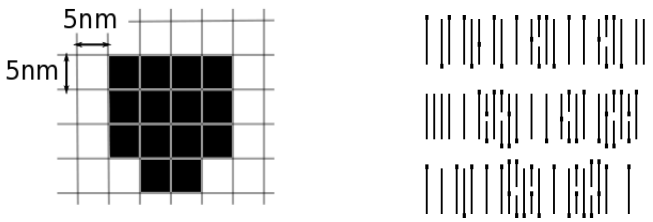
II. FOCSI Layout Regularity Metric

A. Problem Statement

As stated before, there is the need to develop a layout regularity metric that allows circuit designers to compare in a deterministic and unambiguous manner any pair of layouts in terms of regularity. A metric is by definition a system of related measures that facilitates the quantification of some particular characteristic. In our case the characteristic to quantify is the amount of layout regularity. The metric function has to give to a layout a value indicating how much regular it is. Then, for any two layouts, it can determine which of them has higher regularity.

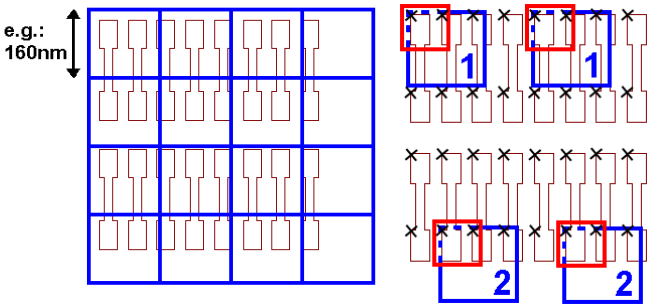
To the best of our knowledge, the only method that has already been used for this purpose is a visual comparison of a two-dimensional Fourier transform. In [4] it has been used to compare the degree of regularity of: (a) a polysilicon layer of an SRAM array, (b) logic implemented using standard cells and (c) logic implemented using a regular fabric. Since a regular layout utilizing a small number of layout patterns is expected to have a finite number of frequency components the comparison is based on the number of frequency components obtained by the Fourier transform. By graphical inspection it can be seen that the SRAM and regular fabric layouts are more regular than the standard cells. However, the graphical inspection of the Fourier graphs does not give enough information to find out which of the two regular layouts is more regular than the other because the two frequency responses are similar.

The two-dimensional Fourier transform does not quantify regularity. We give examples in next sections. It is a graphical representation giving an intuitive and qualitative measure of



(a) Manufacturing grid (b) Complete layout layer

Fig. 1. Granularity extremes.



(a) Contiguous square LAs (b) FOCSI methodology

Fig. 2. Regularity inspection.

regularity. It can be used to compare regular versus non-regular layouts but it is difficult to use it to compare similar layouts in terms of regularity like for instance two layouts developed with regular design techniques. That is why we propose FOCSI: a new layout regularity metric that allows a deterministic and unambiguous regularity comparison for any pair of layout designs. We show in next sections that our metric can determine which of the layouts under study is more regular even if they have similar degrees of regularity. We present the broadest definition of FOCSI in order to illustrate the possibilities offered by our metric.

B. Layout Regularity Definition

We define layout regularity for a given layout layer as the property of this layer to be generated by a reduced number of different layout areas of a given shape and size (e.g., squares of 160 nm x 160 nm). We will refer to these layout areas as LAs, and to the different types of LAs in the layer as layout generators. Therefore, the lower is the number of generators that can be found amongst the LAs the higher the regularity is. The maximum regularity will be achieved when a single generator can be used to generate the whole layer by repeating it along all the layer. On the other hand, the minimum regularity will occur when all LAs are unique, and therefore, there is no repetition at all (all LAs are generators).

Regularity can be studied at different granularities depending on the size considered for LAs inspected. On one hand, the smallest LA that can be considered is defined by the manufacturing grid (5 nm for the 65 nm technology used in this work) so that the LA considered will be a square with this manufacturing grid as both dimensions (Figure 1a). Possible LAs are in this case binary. We can only find in the layout two different generators: one containing the material of the layer inspected and the other containing nothing. Therefore all layouts inspected will have the same regularity and that is why we are not interested in using this extreme. On the other hand, the highest LA that can be considered is the complete layout layer (Figure 1b). Again, all layouts will present the same regularity being generated by a single generator. Thus, regularity must be evaluated using LAs of a size between these two extremes. In particular we propose the use of square areas as LAs. The choice of the size of these square areas will be explained in next sections.

C. Metrics Studied Before FOCSI

In order to explore a layout layer to find out the number of square area generators, our first approach was to divide the complete layout in contiguous squares of sides size multiple of the manufacturing grid (e.g., side of 160 nm = 32 times the 5 nm manufacturing grid) and then to compare one to each other noting the number of different ones. However this option was inadequate because even if the layer was composed by only one layout pattern, low repetition and a high number of generators were observed, and thus very low regularity. Figure 2a shows how regularity is not captured by using this method because all the LAs are different while the visual inspection of the layer shows an important degree of regularity.

The first modification to capture the amount of regularity was to allow two LAs to be noted as the same generator even if they have a given fraction of the area different, being such fraction a threshold to be chosen (e.g., 5%). This way LAs like the first and the third one of the upper row in Figure 2a were considered equal. However this comparison threshold also led to mistakes. Since irregular layouts sometimes have a low number of patterns in some layout layers, depending on the threshold considered, some really different LAs were considered equal and thus the resulting regularity was higher than expected. The real problem was to find the way to align the LAs and the patterns in the layout.

D. FOCSI Proposal

The Fixed Origin Corner Square Inspection (FOCSI) proposal arises from the previous observations. FOCSI first explores the layout layer in order to detect all upper left pattern corners and then considers these corners as the origins of the square LAs to be compared. In that way FOCSI ensures that regularity is captured because LAs are aligned to layout patterns. Figure 2b depicts how FOCSI works for the same example shown before. Black crosses indicate all the corners considered. In this case, types 1 and 2 generators can be detected. Note that in this figure different LA sizes are also illustrated with red and blue squares. Once the corners are fixed, various sizings can be applied to squares in order to evaluate different granularities of regularity. In fact FOCSI is pattern oriented as it inspects at least one LA per pattern.

E. Single Layout Layer FOCSI Measurements

To implement the FOCSI proposal, we first export the layout layer as an image (e.g., TIFF format) and then treat each pixel as a sample. The codification used assigns a 0 value to the sample when the layout is empty and a 1 value to represent the layer material (e.g., polysilicon, oxyde diffusion). The whole layout layer is therefore codified as a matrix of 0's and 1's. Then, we find all upper left pattern corners from where LAs are defined. Finally, these LAs are compared sample by sample against each other in order to calculate the number of different generators the layout layer has. Two LAs are only considered identical if all their samples are identical. The result of this step of FOCSI metric is the number of different generators of the layout layer under study and for the LA sizing defined. We will refer to this number of generators as R_{layer} (e.g., R_{OD}, R_{PO} or R_{M1} for the number of generators in the oxide diffusion layer, in the polysilicon layer and in the metal 1 layer respectively). Therefore the lower R_{layer} is the higher regularity is for this layer. FOCSI also records the number of occurencies of each of the generators of the layer.

F. Complete Layout FOCSI Formulation

The final step to obtain a comprehensive complete layout regularity value (R_{layout}) is to combine all different layout layers regularity values (R_{layer}) calculated. Defining M as the number of layout layers considered, we propose to combine these M measurements assigning weights to each one of them. In general, the layout regularity R_{layout} can be then calculated as follows:

$$R_{layout} = \sum_{j=1}^{M} \beta_j . R_{layerj} \tag{1}$$

where β_j are layout layers weights and R_{layerj} are the regularities measured for the M layout layers considered. In order to enable the comparison of the R_{layout} measures from different layouts we propose that the β_j parameters also fullfill the following property:

$$\sum_{j=1}^{M} \beta_j = 1 \tag{2}$$

Each of the M layer regularities will have a different β_j weight depending on process conditions. We give examples in next sections. R_{layout} can be considered as the final FOCSI metric result. As for R_{layer}, the lower R_{layout} is the higher regularity is. Note that this final R_{layout} is not needed if the objective is the evaluation of a particular layer regularity at a concrete LA sizing. FOCSI can be adapted to measure regularity for different layers and granularities.

III. FOCSI Oriented to Variability Evaluation

A. FOCSI LA Sizing and Optical Interaction Length

Lithography enhancement techniques correct subwavelength lithography process variations taking into account a given layout area determined by the photolithography system used to manufacture the design. The corrected patterns need to be considered with their layout neighborhoods to obtain satisfactory results. Neighborhoods are bounded by the optical interaction length defined as the range of distance in which layout patterns have a non-negligible effect one on the other [7]. For our regularity measurements, in that case oriented to variability evaluation, LA sizing will be, therefore, also bounded by this optical interaction length.

According to [8] the radius of influence of lithography is 5 times the minimum technology feature size. In [9] we have found that it is 500 nm for the 65 nm technology node. Finally, in [10] they have determined that an interaction radius of 220 nm for the available 193 nm lithography will take into account a 93% of the neighborhood effects. In our examples in the 65 nm technology node, with a 193 nm illumination source, to ensure that most of the proximity effects are considered we will use a radius of influence of approximately 320 nm that translates into 640 nm square sides sizing for FOCSI LAs.

B. Standard Cell Layouts under Study

1) Standard Cell Layouts: Standard cell designs are based on the reuse of logical function layout cells (e.g, AND cell, OR cell) to implement the desired circuit. These layout cells have fixed height bounded by the power supplies. However they can have different widths and depending on the function implemented they can include transistors and interconnects in very dissimilar configurations. Moreover, standard cell libraries can include more than 1000 different cells, and therefore a huge number of placing and routing configurations are possible. Resulting standard cell layouts are therefore expected to have a low degree of regularity.

2) Robust Standard Cell Layouts: For this work, we have developed a standard cell library focusing on improving the regularity of the complete circuit layouts. First, to improve macro-regularity, we have chosen a reduced number of cells based on the library proposed in [11] so that the amount of placing and routing configurations compared to the classical standard cell library is reduced. The library contains 24 cells with 15 logic gates, 6 latches, 2 flip-flops and 1 full-adder. Moreover, to increase micro-regularity, all layers are oriented in only one dimension, shapes are placed at constant pitch and all transistors have the same sizing. Transistor fingering is used to obtain different sizes. We will refer to this new library as the Robust standard cell library.

3) ISCAS'85 Layout Generation: We will focus on combinational logic circuits like the ISCAS'85 benchmarks [12] to illustrate our regularity metric. In particular, we have developed the complete set of benchmarks layouts in the 65 nm technology node using a commercial standard cell library (STD) and the Robust standard cell approach (Robust).

C. Single Layout Layers FOCSI Results

Table I shows the results obtained for polysilicon (PO), oxide diffusion (OD) and metal 1 (M1) layers for the different ISCAS'85 layouts considering 640 nm x 640 nm square LAs. We have chosen these three layout layers because they are the

TABLE I
ISCAS'85 FOCSI REGULARITY AND VARIABILITY RESULTS CONSIDERING OD, PO AND M1 LAYERS

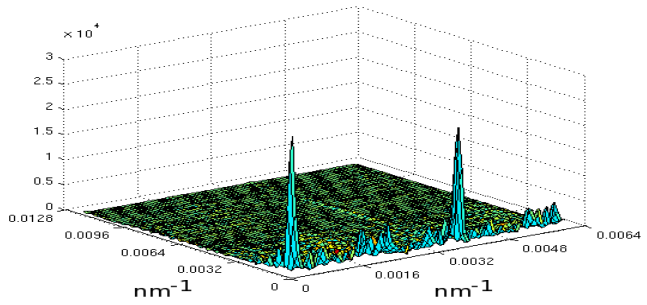
	Single layer: R_{layer}						Complete layout: R_{layout}			Variability reduction		
ISCAS layout	OD LAs	R_{OD} generators	PO LAs	R_{PO} generators	M1 LAs	R_{M1} generators	Layout is OD limited	Layout is PO limited	Layout is M1 limited	OD Layer	PO Layer	M1 Layer
c17 STD	17	17	22	21	37	35	22.70	23.30	26.30	1.69%	2.00%	1.08%
c432 STD	278	167	462	380	540	474	307.65	339.60	369.05	0.77%	0.15%	0.00%
c499 STD	814	283	1237	422	1542	794	452.45	473.30	554.65	0.62%	0.46%	0.31%
c880 STD	617	296	1097	716	1195	946	584.50	647.50	714.50	0.77%	0.15%	0.00%
c1355 STD	859	327	1235	492	1507	825	501.00	525.75	600.60	0.62%	0.31%	0.15%
c1908 STD	581	243	1010	539	1201	825	477.30	521.70	593.70	0.77%	0.15%	0.77%
c2670 STD	1052	485	1795	961	1913	1378	851.05	922.45	1029.65	0.62%	0.15%	0.15%
c3540 STD	1231	554	2433	1433	2586	1837	1138.45	1270.30	1395.05	1.08%	0.15%	0.00%
c5315 STD	2085	737	4350	1639	4480	2506	1449.85	1585.15	1803.65	1.08%	0.15%	0.00%
c6288 STD	6504	939	10332	1136	10652	2591	1411.10	1440.65	1741.50	1.08%	0.62%	0.31%
c7552 STD	2647	993	5168	2053	5763	3298	1887.25	2046.25	2348.25	0.92%	0.15%	0.00%
c17 Robust	22	5	36	15	75	35	15.50	17.00	21.50	23.54%	6.62%	4.00%
c432 Robust	366	9	686	46	1355	156	56.85	62.40	86.25	26.92%	3.38%	7.23%
c499 Robust	700	9	2222	64	3419	237	82.50	90.75	128.10	34.15%	2.62%	6.15%
c880 Robust	660	9	1614	64	2823	259	88.00	96.25	138.00	34.46%	2.77%	5.69%
c1355 Robust	690	9	2182	69	3345	219	79.50	88.50	121.5	36.92%	3.38%	7.23%
c1908 Robust	554	9	1606	65	2552	218	78.05	86.45	119.85	32.15%	3.69%	6.92%
c2670 Robust	1150	9	2817	90	4881	361	121.30	133.45	191.70	29.54%	2.92%	4.31%
c3540 Robust	1528	9	3456	86	6200	171	72.60	84.15	105.00	33.54%	3.38%	5.23%
c5315 Robust	2602	9	6402	92	10775	198	81.15	93.60	118.95	30.31%	2.92%	6.15%
c6288 Robust	5342	9	11287	63	20965	139	57.70	65.80	83.70	33.54%	2.77%	6.92%
c7552 Robust	3000	9	7688	90	12499	183	76.80	88.95	111.60	30.15%	3.23%	6.77%

most representative of the front-end and back-end process. On one hand PO and OD define the transistor active areas, and the polysilicon gate critical dimension variation has a tremendous impact on the timing and energy consumption of circuits. On the other hand M1 layer is representative of the interconnect structure. The total number of LAs inspected is given for each of the layers to show the complexity of the circuits.

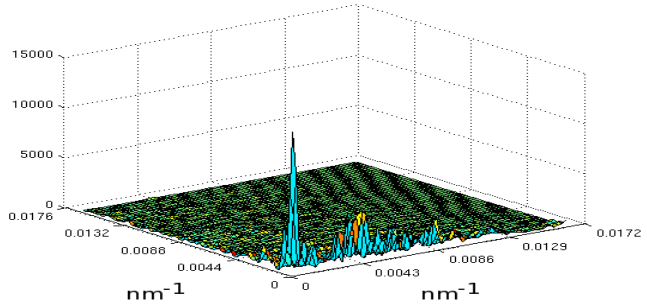
As expected, for layer regularity (R_{layer}), layouts developed with Robust standard cells are clearly more regular than the STD ones because we need fewer number of generators in all cases and for all layers even if the total number of LAs inspected is higher. The difference in regularity for more complex circuits is even higher (e.g., 9 versus 993 generators for the OD layer for c7552 circuit). More complexity implies the use of a higher number of different standard cells but for the Robust library the number of available cells is reduced. In fact layout generators remain almost constant for all layers for the Robust circuits (by construction of the library cells) while they increase importantly for the STD version, specially for PO and M1 layers.

Using the two-dimensional Fourier transform confirms regularity results for instance for the PO layer when comparing Robust and STD for c17 circuit (Figures 3a and 3b). While the STD c17 layout spatial analysis has more representative frequential components, Robust c17 layout presents a clear repetition peak indicating regularity. In those comparisons where one layout is regular and the other one is not, both the two-dimensional Fourier transform and FOCSI can be used to identify the most regular layout.

However, when comparing layouts with a similar degree of regularity the two-dimensional Fourier transform is ambiguous. For instance, if we compare the PO layer for STD c432 layout and c499 layout (Figures 4a and 4b), we obtain Fourier graphs that look almost the same. However, with our metric,



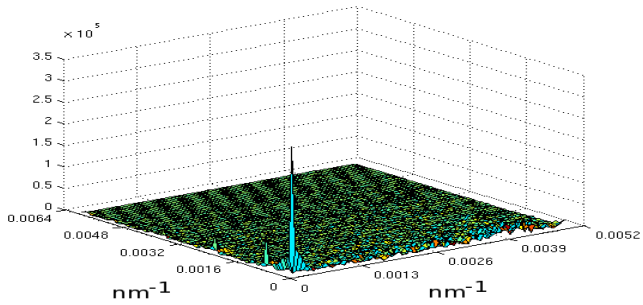
(a) Robust c17



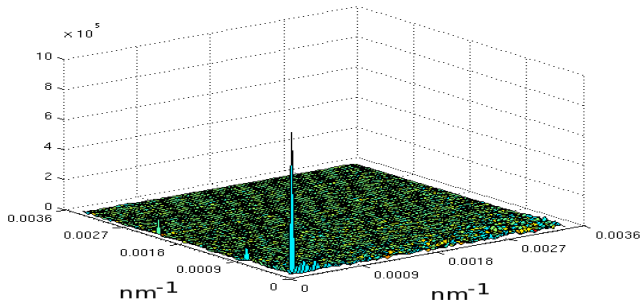
(b) STD c17

Fig. 3. 2D Fourier transform for polysilicon layers with different regularities

we can see that c432 is more regular than c499 (380 versus 422 generators respectively). In fact, since the same standard cell library is used for both designs, regularity is similar but not exactly the same. Therefore, in this case, our metric is able to compare two layouts with similar regularities while the graphical inspection of the two-dimensional Fourier transform cannot.



(a) STD c432



(b) STD c499

Fig. 4. 2D Fourier Transform for polysilicon layers with similar regularities

D. Complete Layout FOCSI Results

For FOCSI oriented to variability evaluation the different β_j weights depend on the criticality of the layer manufacturability. Using test structures for process control to monitor and control the fabrication line, manufacturers can know which of the layout layers is the most affected by systematic subwavelength lithography based failures. Provided that these results have statistical significance, these data can be used to select the weights. Simulations of the fabrication process can also be performed taking into account different lithography enhancement techniques. For instance, if the manufacturing process is weak on M1 layer, the highest weight will be for the M1 regularity. Usually, PO layer is the most critical, because the smallest features are printed on it, like critical gate dimension.

To illustrate our regularity metric proposal (see Table I) we present the calculation of the complete layout regularity (R_{layout}) for the ISCAS'85 studied in previous subsection for PO, OD and M1 layers (M = 3). Considering that the manufacturing process is PO limited we have used 0.45, 0.30 and 0.25 weights for PO, OD and M1 layers respectively. The case where OD is the most critical layer has been calculated using 0.30, 0.45 and 0.25 weights. Finally, the case where M1 is the most critical layer uses 0.30, 0.25 and 0.45 weights. Different results are obtained in each case, with small variations because only 3 layers are considered, however, as expected, Robust designs are more regular than STD ones with all these particular calculations and using these 3 layout layers. As shown in Table I, the regularity for STD and Robust designs decreases when M1 is the most limiting layer because both are more irregular in this layer than in the other ones as it is used for routing. The complete layout regularity value will be obtained by combining all of the layout layers involved in the designs and with more precise weighting values from the manufacturing process.

IV. Regularity and Variability

As explained before, layout regularity will help resolution enhancement techniques to become more effective, as less layout generators need to be corrected for instance by optical proximity correction, that can then be model-based instead of rule-based, or in general, because the whole manufacturing process can be optimized for a reduced set of layout patterns. However, higher layout regularity will not imply itself less process variations. The best example to illustrate it is a layout that can be generated by only one generator. If the printability of the generator is acceptable, the complete layout will have acceptable variations. However, if the printability of the generator is low (e.g., the patterns are placed at forbidden pitches), it will end up with a very regular layout but with a huge amount of variability. In this section we propose a methodology to understand and evaluate the impact of regularity on layout variability.

A. Variability model

To estimate variability in a layout layer for systematic sources of process variability, we propose to calculate the mean variation in the patterns of the layout. Defining N as the number of patterns in the layout and var_i the variation associated to pattern i, the mean variation in a layer can be written as:

$$\mu = \frac{\sum_{i=1}^{N} var_i}{N} \tag{3}$$

The systematic variation associated to each pattern will depend on the pattern itself and on the layout neighborhood inside of the radius of influence of the lithography, and this is exactly what is included in each of the LAs inspected by FOCSI. We assume that patterns with the same neighborhood will have the same variation for systematic variations associated to the manufacturing process. As each pattern of the layout will be represented at least by one FOCSI LA inspected because each pattern has at least on upper left corner, we propose to use FOCSI LAs to calculate the mean variability as follows:

$$\mu = \frac{\sum_{j=1}^{R_{layer}} n_j \cdot var_j}{N_{LA}} \tag{4}$$

where N_{LA} is the number of LAs inspected by FOCSI in the layer, R_{layer} is the number of generators identified by FOCSI in the layer under study, n_j is the number of occurencies of the generator j (information recorded by FOCSI), and var_j is the variation associated to generator j.

To solve Equation (4) we only need to obtain the values of var_j as all the other terms are known. Ideally, each of the

FOCSI generators can be simulated in terms of lithography to obtain these values, however, this will be time consuming and the results can vary depending on the lithography models used. We propose to use the Monte Carlo method assigning random values to var_j from a distribution, that can be given by the foundries (e.g., a gaussian distribution). This statistical methodology is already widely used for electrical simulations including process variations [9], [13].

B. Results for ISCAS'85 layouts

We have used the Monte Carlo analysis considering a gaussian distribution for variations of the patterns to calculate the mean variation for each layer of the STD and Robust ISCAS'85 layouts. We have repeated the Monte Carlo 1082 times to calculate the mean and the standard deviation of the mean variation with a confidence level of 95% and a width for the confidence interval 5% [14]. The final distribution of variations has the same mean than the original variation distribution but the standard deviation is reduced depending on layout regularity. The standard deviation reduction results are shown in Table I indicated as variability reduction. They are normalized so that they are independent of the actual mean and standard deviation of the distribution used in the Monte Carlo experiment.

On average for all STD layouts, the variability is only reduced 0.91% for OD, 0.41% for PO and 0.18% for M1. A very small reduction is obtained because STD layouts are irregular. However, for Robust designs, the reductions are 31.38%, 3.43% and 6.06% respectively showing in particular the OD regularity benefits (all transistors have the same size). In general, more regular layouts with less number of generators increase variations predictability by reducing its standard deviation (e.g., for M1, c2670 Robust has 361 generators and a 4.31% reduction, c3540 Robust has 171 generators and a 5.23% reduction). However, the number of generators is not the only factor affecting variability. The number of occurencies of the generators (its distribution) has also an important influence (e.g., for M1, c3540 Robust has 198 generators, so more than c2670 has, but has 6.15%, so more than c2670, because the repetition of the generators in c3540 is higher as c3540 has a total number of LAs of 10775 and c2670 has only 6200). Therefore, layout variability will be affected by layout regularity taking into account the number of generators as well as its distribution. Layout variability can be further reduced by optimizing the manufacturing process for the reduced set of layout generators, but it is not directly related to layout regularity. For regular layouts this will be particularly beneficial as the number of generators will be low.

V. Conclusion

FOCSI can calculate layout regularity for different granularities quantifying the number of layout generators and weighting them depending on layer criticality. We have shown that FOCSI provides an accurate comparison of layout layers even if their regularity is similar. Results for ISCAS'85 circuits developed with the STD approach have been compared to the same circuits developed with a new regular Robust standard cell library showing that FOCSI captures the higher regularity of the Robust version. Then, we have linked layout regularity and variability by means of a Monte Carlo analysis showing that the decrease of the standard deviation of the mean variations in a layer depends on layout regularity in a comprehensive way, taking into account the number of generators of the layout and also its distribution. The optimization of the manufacturing process for the reduced set of layout generators can then further increase the layout printability, but this is not directly related to layout regularity.

In future works, FOCSI can be used to reduce layout variability at different moments of the design flow. First, applied during the place step, it can provide the information required to modify the positions of the standard cells focusing on maximizing regularity. Second, FOCSI can be used in the routing step to maximize wire regularity. In both cases, the computational cost of FOCSI recalculation is expected to be reduced as only the LAs modified will need to be taken into account to obtain the new regularity. Once all LAs and generators are identified in the first run of FOCSI, optimization algorithms can be incrementally applied to maximize regularity and therefore minimize variability.

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