Efficiency Evaluation of Parametric Failure Mitigation Techniques for Reliable SRAM Operation

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***Abstract*—The efficiency of different assist techniques for SRAM cell functionality improvement under the influence of random process variation is studied in this paper. The sensitivity of an SRAM cell functionality metrics when using control voltage level assist techniques is analyzed in read and write operation modes. The efficiency of the assist techniques is estimated by means of parametric analysis. The purpose is to find the degree of functionality metric improvement in each operation mode. The Acceptance Region concept is used for parametric analysis of SRAM cell functionality under random threshold voltage variations. In order to increase the reliability of the SRAM several assist techniques, chosen among the most efficient ones for each operation mode, are considered. This analysis offers a qualitative indication of the cell's functionality improvement by means of the efficient computation of a metric in parameter domain analysis. The results are proven to have high correlation with the ones obtained by means of the classical Monte Carlo simulations with significant savings in comparing different assist techniques.**

Keywords-SRAM Cell; Voltage Level Assist Techniques; Spec Violation Metric;

I. INTRODUCTION

Over the years, several design techniques and circuit assist methods have been proposed for reliable SRAM operation [1]-[6]. Bias based circuit assist methods have been developed to improve the speed and reliability of the memory array, however write assist techniques are detrimental to read stability of the half-accessed cells, while read assist techniques increase power consumption [7], [8]. The half accessed cells are the ones that share the same row with the one undergoing the write operation and for these cells the word-line is asserted but the bit-lines are not pulled low [4]. Word line (WL) boosting has been proven to be the most efficient write-assist technique [4], [5] while increasing the array's supply voltage is the most efficient read-assist technique [8]. In this work several assist techniques for SRAM cell functionality improvement have been analyzed. They are explained in the first section of this chapter and their efficiencies compared.

The assist techniques are organized in three categories: transistor level, control voltage level and architectural level. At transistor level, the functionality of the SRAM cell could be improved by changing the transistor sizes or their threshold voltages, while at control voltage level, by adjusting the supply voltage, word line and bit line voltages. At architectural level, the size of the SRAM array is modified for SRAM cell functionality improvement. The architectural level assist techniques are implemented as changes in the word line and bit line capacitance, since they are directly related to the size and architecture of the array. The focus of this paper is on the control voltage level assist techniques since they have been proven by previous work to be effective and no changes in the cell's design are needed to implement them.

In the next section of this paper, a sensitivity analysis of the SRAM cell under control voltage level assist techniques is performed, in order to determine which of the control voltages has the best chance to improve the cell's reliability under process variations. In the third section, a method to compare different SRAM cells by means of parametric analysis is described. Based on this method, a new *Spec. Violation Metric (SVM)* is defined. This metric is used to evaluate the efficiency of different parametric failure mitigation techniques in the forth section of this paper. Finally, conclusions are drawn in the fifth section.

II. SRAM CELL'S SENSITIVITY TO CONTROL VOLTAGE LEVEL ASSIST TECHNIQUES

In order to evaluate the behavior of the SRAM cell (illustrated in Fig. 1a) in data retention read and write operation modes, functionality metrics are needed. In data retention mode, the cell's functionality is evaluated by means of static robustness, i.e. Static Noise Margin (*SNM*) – Fig. 1b. An assist technique which would improve the cell's functionality in data retention mode should increase the Static Noise Margin. The functionality in read operation mode is evaluated by means of Zero Level Degradation (*ZLD*) which gives a measure of the cell's robustness to read operation and by means of differential bit line voltage (*dBL*) which gives a measure of the accuracy with which the data stored by the cell can be read – Fig. 1c. An assist technique which will improve the cell's functionality in read operation should decrease the zero level degradation and increase the differential bit line voltage. The functionality in write operation mode is evaluated by means of write time defined as the time needed to flip the cell's state (*Tw*) – Fig. 1d. An assist technique which will improve the cell's functionality in write operation should decrease the write time.

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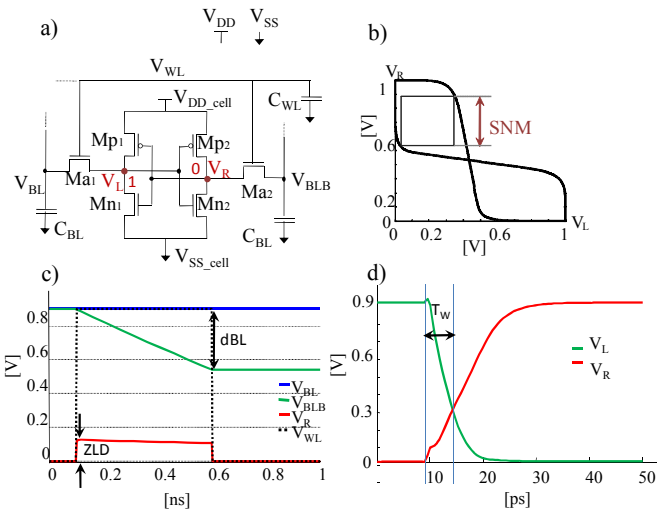

Figure 1 – Definitions of the functionality metrics: a) the standard 6T SRAM cell, b) Static Noise Margin (SNM) for data retention mode robustness characterization, c) Zero Level Degradation (ZLD) and differential bit line voltage (dBL) for read mode functionality characterization, d) Write time (Tw) for write mode functionality characterization

At control voltage level the functionality of the SRAM cell could be improved by adjusting the supply voltage, word line and bit line voltages [4], [7]. In this section, the sensitivity of the SRAM cell's functionality metrics is analyzed assuming different control voltage level assist techniques. For this analysis the voltage values changes are considered in range of ±20%.

A. *Supply Voltage*

The supply voltage can be modified locally, i.e. at cell level (at $V_{DD\text{-}cell}$ terminal) or globally, i.e. at all of the following terminals: $V_{DD\text{-}cell}$, V_{WL}, V_{BL} & V_{BLB} for read and V_{BL} or V_{BLB} for write.

Decreasing the global supply voltage leads to a decrease of the zero level degradation, since the strength of the access transistor is decreased by reducing its gate voltage (V_{WL}) when compared to the nominal case. The same effect has the variation of the global supply voltage on the differential bit line, only in this case an increased differential bit line means a more reliable read operation. Increasing the supply voltage at all terminals leads to a decrease in the write time.

When analyzing the zero level degradation under changes in cell level supply voltage ($V_{DD\text{-}cell}$) a decrease is observed when the supply voltage increases. This can be justified by the improved resilience of the cross coupled inverters at higher supply voltage. The differential bit line voltage obtained during read operation also increases when the cell's supply voltage increases. Due to the voltage difference between the '1' storing node and corresponding bit line, a current passes through the access transistor, charging the node capacitance and consequently increasing the voltage value on that bit line, hence increasing the voltage difference between the two bit lines. The time needed to write data to the cell (*Tw*) decreases when the cell's supply voltage decreases, leading to increase write functionality. This improvement is obtained by weakening the pull-up transistor with respect to the access transistor therefore facilitating the write operation.

B. *Word Line Voltage*

The zero level degradation increases with increasing the word line voltage since a higher V_{WL} leads more current flowing to the access transistor. In order to improve the robustness of the SRAM cell in read operation the word line voltage has to be reduced. Unfortunately, this leads to a decrease of the differential bit line voltage which translates in less reliable read operation. Boosting the word line voltage during write operation increases the gate voltage of the access transistor and hence increases its drive strength leading to faster write, i.e. decrease of *Tw*.

C. *Bit Line Voltage*

In order to write new data to the cell, the bit line corresponding to the '0' storing node (BLB in Fig. 1a) has to be charged to V_{DD} while the bit line corresponding to the '1' storing node (BL in Fig. 1a) has to be discharged. Since the cell was designed to reject high disturbances at the '0' node before flipping state, boosting the V_{BLB} voltage will have no significant effect on the write time. On the other hand, decreasing the bit line voltage V_{BL} leads to an increase in the gate to source voltage of the access transistor rendering it stronger and hence allowing for a faster flip of the cell.

Different bias conditions for the nodal voltages of the SRAM cell have different effects on the functionality metrics in read and write operation modes. Figure 2 and Table 1 summarize the described assist methods and their effects in read and write operation.

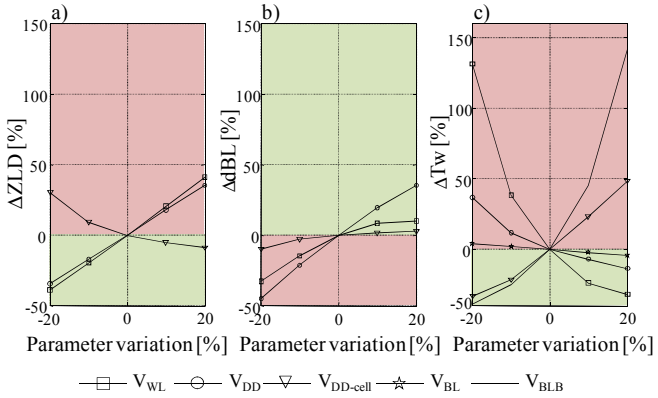

Figure 2 – Functionality Metrics vs. Assist Techniques: a) Sensitivity of Zero Level Degradation to control voltage variation, b) Sensitivity of differential bit line voltage to control voltage variation, c) Sensitivity of write time to control voltage variation. The green regions mark the cell's functionality improvement, while the red regions mark the functionality degradation.

TABLE 1. ASSIST METHODS AND THEIR IMPACT ON CELL'S FUNCTIONALITY

Control Voltage	Read	Access	Write
V_{WL}	↓ 1	↑ 2	↑ 2
V_{DD}	↓ 2	↑ 1	↑ 4
$V_{DD\text{-}cell}$	↑ 3	↑ 3	↓ 1
V_{BL}	-	-	↑ 5
V_{BLB}	-	-	↓ 3

The arrows in Table 1 indicate the direction in which the corresponding control voltage has to be modified in order to improve the functionality of the cell (i.e. the arrow pointing upwards means increasing the corresponding voltage leads to increased functionality of the cell). The numbers in each box are used to sort the assist methods by their impact on each of the functionality metrics, *1* representing the larger impact, *5* the lower.

For a robust read operation, the zero level degradation has to be as small as possible, so that under process variability the probability of ZLD voltage being larger than the trip point of the controller inverter could be reduced. This effect is obtained by lowering the word line voltage, the global supply voltage or increasing the cell's supply voltage. In order to ensure a correct read of the data stored by the SRAM cell, the differential bit line voltage has to be large enough for the sense amplifier to detect it. In other words, a larger differential bit line voltage decreases the chances of an erroneous read. This increase of dBL can be obtained by increasing the word line voltage, the global supply voltage or the cell's supply voltage ($V_{DD\text{-}cell}$). The write operation can be improved by increasing the cell's supply voltage, the word line voltage and the global supply voltage.

A method to compare different SRAM cells by means of parametric failure analysis is described in the next section.

III. Parametric Analysis of the SRAM Cell

In this section, a method of comparing the functionality of different SRAM cells under random threshold voltage variation by means of parametric analysis using the Acceptance Region (AR) concept is described.

The analysis of the SRAM cell functionality is performed in the parameter variation space. All transistors in the SRAM cell are assumed to be affected by random process variability hence the parameter variation space is a 6D space given by the threshold voltage variation for each of the cell's transistors ($\Delta V_{TH1\div6}$).

The Acceptance Region is defined as the region in the parameter variation space, where the SRAM cell functions according to a set of specifications. The remainder of the parameter variation space forms the Failure Region (FR). The boundary between Acceptance and Failure Regions is defined as the Satisfiability Boundary (SB) [9].

Without loss of generality, for illustration simplicity, the parametric analysis method is described using a 2D representation. Assuming that only two of the cell's transistors are subjected to threshold voltage variability, while the others maintain their nominal threshold voltage values, the parameter variation space is given by the ($\Delta V_{TH2}0\Delta V_{TH1}$) plane (Fig. 3). The combination of threshold voltage variations for which the SRAM cell complies with the specifications gives the Acceptance Region (green region in Fig. 3), all other ΔV_{TH} combinations will cause specification violation (Failure region – marked in red in Fig. 3). Precisely identifying the acceptance and failure regions assumes a large number of electrical simulations, which are time consuming.

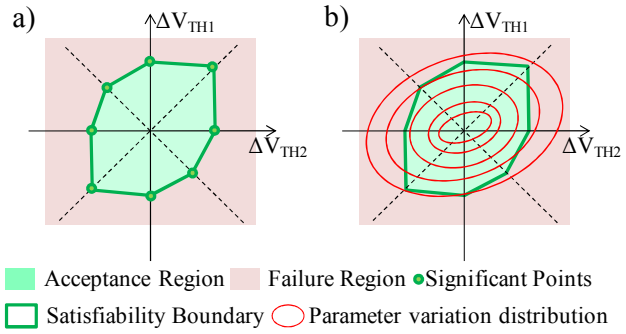

Figure 3 – Two dimensional representations of Acceptance and Failure Regions: a) the Satisfiability Boundary in the parameter space obtained by linear interpolation using the Significant Points; b) Failure probability estimation by over imposing the statistical parameter distribution [9]

In this analysis, the satisfiability boundary is approximated by a polygon whose vertices (Significant Points) are obtained by simulation. The AR in this case is approximated by the region inside this polygon (Fig. 3a).

Once the two regions have been identified, the failure probability of the SRAM cell can be obtained taking into consideration the probability density function and integrating over the Failure Region (Fig. 3b).

Different cells can be compared by comparing their failure probabilities. A quantitative comparison between SRAM cells assuming different assist techniques can be thus performed and the efficiencies of the said assist techniques on mitigating parametric failures can be estimated.

Since the interest of this paper is to obtain a fast estimation of the assist technique efficiency, the integration step is not necessary. Analyzing the acceptance regions assuming different control voltage levels, a qualitative comparison between different assist methods is performed.

The aim of a parametric failure mitigation technique is to decrease as much as possible the cell's failure probability under process variability. In this analysis, a zero failure probability is achieved when the maximum variability range in parameter space is inscribed in the Acceptance Region; i.e. there is no combination of process variation in the maximum variability range that will cause the cell to fail. This situation is illustrated in 2D in Fig. 4a. Therefore the purpose of an assist technique used to mitigate the parametric failures of an SRAM cell is to enlarge the acceptance region, preferably until it circumscribes the maximum variability range. In this note, a qualitative comparison between different designs can be performed by evaluating the position of the acceptance region and the maximum variability range. The less reliable design is the one for which the acceptance region is inscribed in the maximum variability range (Fig. 4c), while the more reliable is the one for which the AR circumscribes the maximum variability range (Fig. 4a).

A new metric to evaluate the SRAM cell's compliance with the functional specifications by parametric analysis is proposed: the *Spec Violation Metric* (*SVM*).

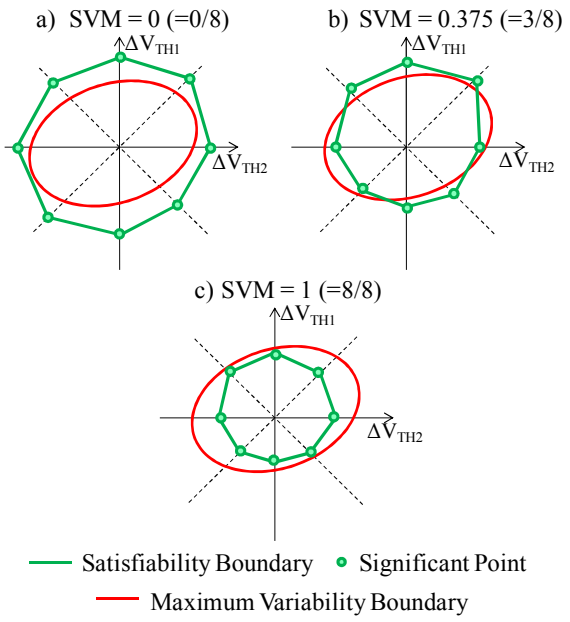

Figure 4 – 2D Spec. Violation Metric (SVM) examples: a) best case scenario SVM = 0, b) SVM = 0.375, c) worst case scenario SVM = 1 (the total number of SPs in this illustration is 8)

This metric evaluates the localization of the acceptance region with respect to the maximum variability range in parameter variation space, more precisely, how much of the AR is inside the maximum variability range. The Spec Violation Metric is maximum (=1) in the worst case scenario (AR inscribed in the maximum variability range) and zero in the best case scenario (AR circumscribes the maximum variability range).

Since the acceptance region is determined as the area of the parameter variation space delimited by the satisfiability boundary, the analysis can be performed by studying the position of this boundary with respect to the maximum variability range in the parameter variation space. Seeing as the satisfiability boundary is approximated by a polygon whose vertices are the significant points, the position of the AR with respect to the maximum variability range, is given by the localization of the significant points. The Spec Violation Metric is defined as the ration between the number of significant points inside the maximum variability range and the total number of significant points. In the example in Fig. 4b 3 of the 8 significant points are inside the maximum variability range, hence *SVM=3/8*. Assuming the maximum variability to be 3σ, the Spec Violation Metric is defined as:

$$SVM = \frac{\#SP^{3\sigma}}{\#SP} \qquad (1)$$

where *SVM* is the Spec Violation Metric, $\#SP^{3\sigma}$ is the number of significant points in the 3σ variability range, and *#SP* is the total number of significant points.

For the SRAM cell to be considered reliable under process variation, it has to be reliable in all operation modes. The acceptance region for each operation mode has been determined by evaluating the functionality metrics described in the first section of the paper (i.e. the static noise margin, zero order degradation, differential bit line and write time) in the parameter domain and imposing cell operation performances in terms of robustness and speed. The region in the parameter space where all specifications are complied with is given by the intersection of these acceptance regions (as illustrated in Fig. 5a in a 2D representation). The resulting acceptance region is defined as the *Overall Acceptance Region*. This acceptance region is delimited by the overall satisfiability boundary.

The significant points on the overall satisfiability boundary ($SP_{overall}$) are determined by identifying among the significant points (*SP*) the closest point to the origin of the parameter space for each searching direction. The searching direction is indicated by $j=1 \div J$, with *J* denoting the total number of directions (in the 2D representations in Fig. 4 and Fig. 5, *J* is 8). The module of the vector from the parameter space origin to the significant point $SP_k(j)$ (where *k* is either *a* - access mode, *w* - write mode, *r* - read mode or *h* - data retention mode and denotes the operation mode satisfiability boundary to which the significant point belongs), obtained for the j^{th} searching direction is given by $|\boldsymbol{SP}_k(j)|$.

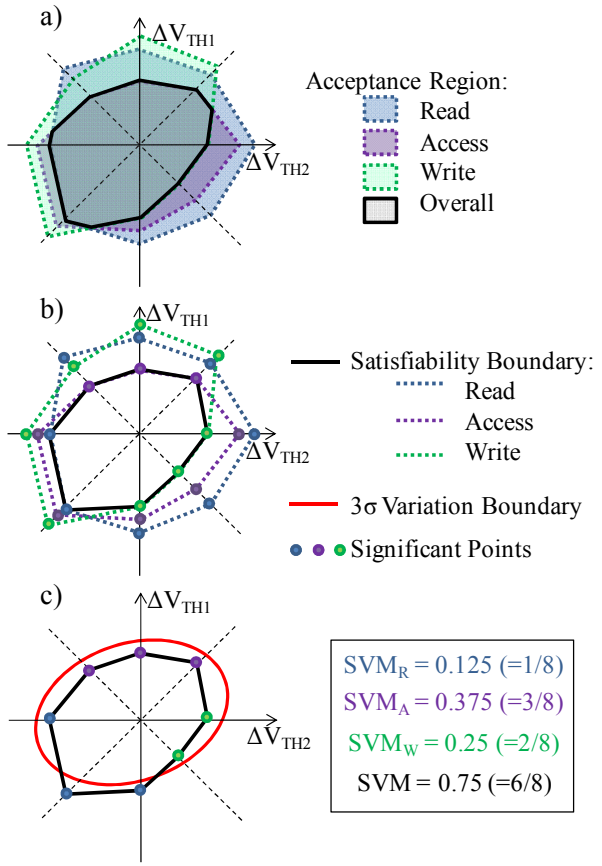

Figure 5 – Global and Operation Mode Contribution SVM in 2D analysis: a) Definition of the *Overall Acceptance Region*, b) Estimation of the *Overall Satisfiability Boundary*, c) Estimation of the *Operation Mode Contribution Metrics* and *Global SVM*

The vector from the origin of the parameter space to the significant point $SP_{overall}$ is given by $\boldsymbol{SP_{overall}}$ vector and its module is determined by:

$$|SP_{overall}(j)| = \min(|SP_r(j)|, |SP_a(j)|, |SP_w(j)|, |SP_h(j)|) \quad (2)$$

Equation (2) is illustrated in Fig. 5b in a two dimensional representation.

Moreover, for the proposed analysis methodology the points inside the 3σ variability range are of interest. The set of overall significant points inside the maximum variability range (in each searching direction *j*) is given by the set of significant points defined as:

$$\left\{SP^{3\sigma}_{overall}(j)\right\} = \left\{SP_{overall}(j) \,|\, |SP_{overall}(j)| < 3\sigma\right\} \quad (3)$$

Each of these points belongs to one of the individual satisfiability boundaries as it can be observed from Fig. 5b. In this way, one can identify which of the operation modes is more sensitive to random threshold voltage variation, by finding out which of the individual satisfiability boundaries has more significant points inside the maximum variability range (spec. violation points).

The spec violation metric is defined for each operation mode: *Operation Mode Contribution Metrics*. The operation mode contribution Spec Violation Metric is defined as the number of points among the overall satisfiability points given by each of the operation modes divided by the total number of significant points.

- Read mode

$$SVM_r = \frac{\#\left\{SP^{3\sigma}_{overall} \cap SP_r\right\}}{\#SP_{overall}} \quad (4)$$

- Access Mode

$$SVM_a = \frac{\#\left\{SP^{3\sigma}_{overall} \cap SP_a\right\}}{\#SP_{overall}} \quad (5)$$

- Write Mode

$$SVM_w = \frac{\#\left\{SP^{3\sigma}_{overall} \cap SP_w\right\}}{\#SP_{overall}} \quad (6)$$

In the 2D representation in Fig. 5c, the overall significant points are illustrated, and their provenience marked by different colors (green dots for SP_w, violet dots for SP_a and blue dots for SP_r). The values obtained for the operation mode contribution metrics and the global spec violation metric are also included in Fig. 5c. The operation mode contribution metric which takes the larger value indicates the more sensitive operation to process variation. In this example the larger contribution SVM is SVM_a (access mode) which means that the cell is most likely to fail during read operation due to insufficient differential bit line voltage. Therefore one can conclude that an assist technique capable of increasing the differential bit line voltage will decrease the cells failure probability.

From these considerations and using Table 1 a decision can be made on which of the assist techniques should be used to mitigate the effect of process variability on the SRAM for correct operation.

In the next subsection, the effect of different assist techniques on the SRAM cell functionality under random threshold voltage variation is analyzed by means of spec violation metrics.

IV. Efficiency Evaluation of Parametric Failure Mitigation Techniques

First, HSPICE simulations have been performed to localize the Acceptance Region in the parameter variation space in each operation mode for a 6T SRAM cell designed using high performance 32nm Predictive Technology Model (PTM) transistors [10]. The analysis is performed in 6D parameter variation space, since all transistors are assumed to be subjected to random threshold voltage variation. Once the acceptance regions for read robustness, read access and write have been determined, the overall acceptance region is estimated as the region in the parameter space where all operation modes are successful, i.e. as the intersection between the acceptance regions of individual modes.

The Spec Violation Metrics, both operation mode contribution and global, are determined for assist technique efficiency estimation. When analyzing the nominal SRAM cell (i.e. no assist technique applied), the write mode contribution spec violation metric is zero, which means that the overall satisfiability boundary is given only by read and access mode, implying that for the given specifications, assist techniques have to be applied to improve the robustness in read mode (decrease the zero level degradation) and the read reliability (increase the differential bit line voltage). It derives, using Table 1, that the control voltages that need to be modified for increase reliability under process variations are the supply voltage, at cell level and overall and the word line voltage.

The SVM metrics have been determined for 5 different setups for assist technique efficiency evaluation: 1) no assist technique (nominal); 2) 10% increase in the cell's supply voltage ($V_{DD\text{-}cell}$); 3) 10% increase in the overall supply voltage (V_{DD}); 4) 10% increase in the word line voltage (V_{WL}) and 5) 10% decrease in the word line voltage (V_{WL}).

The most efficient method to mitigate the random threshold voltage variability when the robustness of the SRAM cell to read access is analyzed is to increase the supply voltage at $V_{DD\text{-}cell}$ node, the same method is the most efficient for improving the differential bit line voltage for a reliable read operation.

In Fig. 6 the normalized operation mode contribution metrics are illustrated for read robustness and read access mode and also the global spec violation metric, assuming 3σ variability for each of the five assist techniques previously mentioned. The metrics are normalized with respect to their value in the nominal case, i.e. when no assist technique is used.

It can be observed that all five techniques help decrease the number of Significant Points in the maximum variability range

($SP^{3\sigma}_{overall}$) and hence increase the Acceptance Region. Boosting the word line voltage by 10% an 11% decrease of the overall SVM is observed, while boosting the supply voltage at cell node ($V_{DD\text{-}cell}$) by 10% an 84% decrease of the overall SVM is observed proving that this is the most efficient mitigation technique among the ones evaluated in this paper. Also, by comparing the normalized operation mode contribution metrics for each mode (SVM_a and SVM_r), the efficiencies of the used mitigation techniques can be compared.

In order to validate the proposed Spec Violation Metric, the failure probabilities have been determined by means of Monte Carlo simulations. The cell's failure probabilities are obtained for each of the previously described setups (nominal, boosted V_{DD}, $V_{DD\text{-}cell}$ and V_{WL} and decreased V_{WL}). The correlation between the normalized Spec Violation Metric and the normalized cell failure probability metric is determined using Pearson's Correlation Coefficient and illustrated in Fig. 7. The Pearson correlation coefficient in this analysis is r = 0.916.

This high correlation proves that the proposed metric (Spec Violation Metric) is suitable to estimate the benefits provided by an assist technique, without the need of actually computing the cell's failure probability. In this way, a combination of assist techniques can be analyzed, and the most efficient one chosen for mitigating the effects of process variability on the cell's functionality.

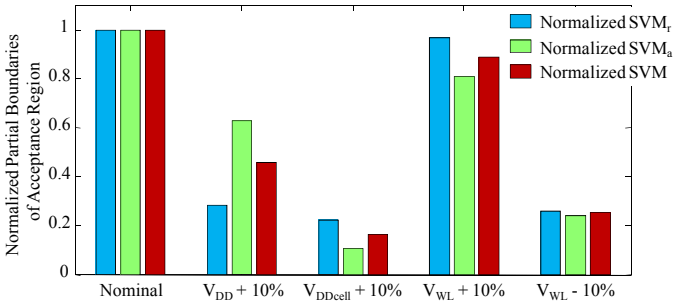

Figure 6 – Normalized Operation mode Contributions to Spec Violation Metric and the Global Spec Violation Metric in moderate variability scenario

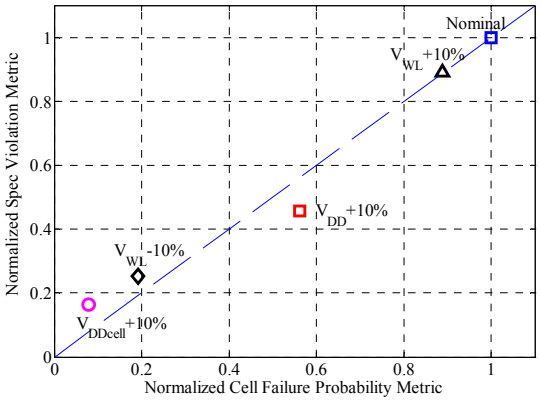

Figure 7 – Correlation between the two metrics: the cell's failure probability and the Spec Violation Metric in moderate variability, correlation coefficient: r = 0.916

V. Conclusions

This paper proposes a new method to evaluate the efficiencies of different assist techniques used to mitigate the parametric failures of an SRAM cell. The method is based on analyzing the cell's performance in the parameter variation space by identifying the acceptance region and localizing it with respect to the maximum variability range. This is done by means of the proposed *Spec. Violation Metric (SVM)*. This metric can be evaluated for each operation mode (contribution metric) in order to determine the most likely failure scenario without the need of statistical analysis.

By using the proposed methodology the effects of the assist techniques can be evaluated qualitatively and quantitatively (by determining the Spec Violation Metric) for each individual operation mode and for the overall cell functionality. The results obtained using the SVM approach have been proven to have high correlation (0.916) with the ones obtained by means of Monte Carlo simulations. The method is two orders of magnitude faster when compared with standard Monte Carlo simulations (in this case 100000) and assuming the maximum variability range to be 3σ. The speed up is even higher if the maximum variability range is assumed to be 6σ (which is the case for the high capacity memories), since for the SVM method the same number of simulations is needed, while the number of MC simulations increases considerably.

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