

# Sliding-Mode Control to Compensate PVT Variations in Dual Core Systems

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**Abstract**—In this paper, we present a novel robust sliding-mode controller for stabilizing supply voltage and clock frequency of dual core processors determined by dynamic voltage and frequency scaling (DVFS) methods in the presence of systematic and random variations. We show that maximum rejection for process, voltage and temperature (PVT) variations can be achieved by using the proposed sliding-mode controller. The stabilization of the presented controller is confirmed by the Lyapunov method. Experimental results demonstrate maximum 20% robustness against 20% parameter variations for a hardware of two core processors executing a JPEG decoding application.

**Keywords**- Sliding-Mode Feedback Control; PVT Variations; Systematic and Random Variations; Dual Core System;

## I. INTRODUCTION

The use of multiprocessor architecture instead of single-processor architecture typically results in more power savings with constant throughput [1]. So far different extensive works have been done to cope with the synchronization and control of multiple concurrent tasks on multiple processors cores [2]. In addition, different dynamic voltage and frequency scaling (DVFS) methods have been proposed to scale back processor voltage and frequency to match processing requirements for the purpose of saving energy consumption [3].

The operating supply voltage and clock frequency determined through DVFS are not always reliable, since they are prone to process, voltage and temperature (PVT) variations. In [4, 5], it has been showed that parameter variations pose a major challenge for design and reliability of high performance microprocessors in nanometer technologies. Also, because of the larger impact of memory latency and bandwidth on the overall throughput, multi-core processors are essentially less variation tolerant than single core processors [6, 7]. Therefore, a technique to control the nominal behavior of system parameters -supply voltage and clock frequency- is needed to attain the optimum performance in low power multi-core systems. Two control methods have been proposed to deal with the stabilization of voltage and frequency in multiprocessors: the proportional integral derivative (PID) controller presented in [8] and the state-feedback controller presented in [9]. However, a PID controller does not guarantee the correct operation of the processors in the presence of parameter variations [10]. The same argument holds for state-feedback controllers. A state-feedback controller has a limited robustness bound for system parameters against dynamic process

variations. Beside feedback controllers, software based look-up tables have been proposed as well to compensate process variations in multi-core processors [11]. Due to the unpredictability nature of PVT variations, look-up table methods are not reliable for diverse applications, and furthermore, the table needs to be designed for each particular application.

In this paper, we present a robust controller for stabilizing the supply voltage and clock frequency obtained through DVFS. Our approach works for dual core processor architectures in the presence of PVT variations. We consider the model of dual core processors that are communicating with each other across two mixed-voltage, and mixed-frequency buffers. We assume that: 1) DVFS is applied to both processors to determine the minimum voltage and frequency of each processor and the buffers in between them, 2) The occupancy of both buffers is measurable. In this paper, we propose a sliding-mode control rule to compensate PVT variations. The sliding-mode controller measures the buffer occupancy in the presence of PVT variations. With respect to the reference occupancy value, it adjusts clock frequency to compensate the maximum amount of variations. In fact, the sliding-mode controller is a supervisory feedback controller for DVFS that rejects the impact of PVT variations. Unlike other works [10, 12], the proposed sliding-mode controller feedback law guarantees the stability of the system against PVT variations. We prove the stability based on the Lyapunov method and the state-space model of the dual core system.

The paper is organized as follows: In section (II) we present the problem description. In section (III) we design the sliding-mode controller to stabilize system parameters around desired values determined by DVFS in the presence of system uncertainties and PVT variations. The results are presented in section (IV) and finally the paper is concluded in section (V).

## II. PROBLEM DESCRIPTION

Consider the dual core architecture shown in Fig. 1. The

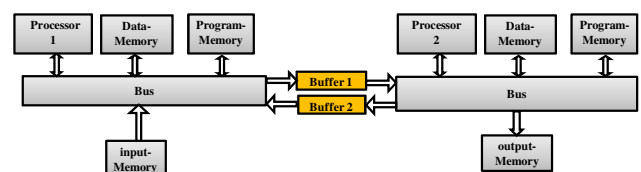


Figure 1. Dual processor architecture used to share and execute applications. Two buffers between processors are used, one for writing the informations and the other one for reading them

state-space model of this architecture is as follows [8, 9]:

$$\begin{cases} q_1(t) = q_1(t - T_c) + T_c \cdot [\lambda_1 f_1(t - T_c) - \mu_1 f_2(t - T_c)] \\ q_2(t) = q_2(t - T_c) + T_c \cdot [\lambda_2 f_2(t - T_c) - \mu_2 f_1(t - T_c)] \end{cases} \quad (1)$$

where  $q_i(t)$   $\{i = 1, 2\}$  is the occupancy of the  $i^{\text{th}}$  FIFO at time  $t$   $\{t = T_c, 2T_c, \dots\}$ ,  $T_c$  is the control interval time during which the system parameters, frequency and supply voltage of processors, are fixed,  $\lambda_i(t)$  is the arrival rate of data into the  $i^{\text{th}}$  buffer at time  $t$ ,  $\mu_i(t)$  is the departure rate of data from the  $i^{\text{th}}$  buffer, and  $f_i(t)$  is the clock frequency of processor  $i$  at time  $t$ . Suppose that the application is already divided between processors and that the values of  $f_1$  and  $f_2$  are determined by DVFS taking into account workload variations to satisfy the worst case execution time (WCET) of the application. If PVT variations do not exist and DVFS determines the frequency values of processor 1 and 2 as  $(f_1, f_2)$ , then the occupancy values of buffer 1 and 2 at time  $t$  are as  $(q_1, q_2)$ . But due to PVT variations the frequency values of processor 1 and 2 are as  $(f_1 \pm \Delta f_1, f_2 \pm \Delta f_2)$  and consequently the occupancy values of buffers are as  $(q_1 \pm \Delta q_1, q_2 \pm \Delta q_2)$ . Since the correct operation of the system depends on nominal parameter values known at design time, it then follows that  $(q_1 \pm \Delta q_1, q_2 \pm \Delta q_2)$  should approach  $(q_1, q_2)$  as much as possible. Our goal is to design two sliding-mode controllers to stabilize system parameters around the desired values (reference points) considering PVT variations and possible state-space model uncertainties. The sliding-mode controller modifies the operating frequency (and supply voltage) of processors 1 and 2 to regulate the occupancy values of both buffers to the desired values without being affected by PVT variations and also inaccuracy of the state-space model (1). On the other hand the sliding-mode controller modifies the frequency of processors in the neighborhood of their nominal values to compensate PVT variations. Fig. 2 shows that the frequency values of processors 1 and 2 are determined by the DVFS method (the nominal values) and that the sliding-mode controllers adjust them to minimize PVT variations.

### III. SLIDING-MODE FEEDBACK CONTROLLER

Sliding-mode control is a high-speed switching feedback control that switches between two values based upon a control rule [12]. In this section, we describe how to design the sliding-mode feedback controllers to regulate buffer occupancies of (1)

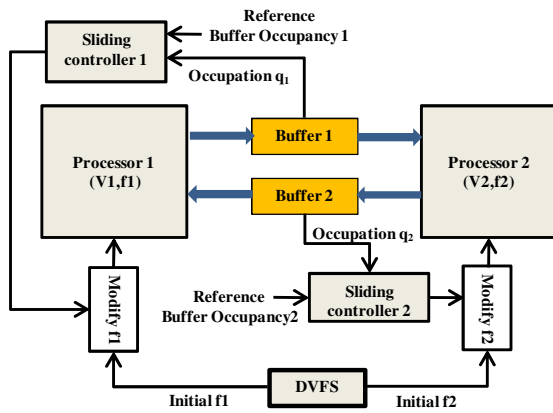


Figure 2. General block diagram of the proposed sliding feedbacks to adjust clock frequencies (and supply voltages) of the dual core system

by modifying frequency values determined by DVFS. Also, we mathematically prove that the feedback controllers guarantee the stability of the architecture against PVT variations and system uncertainties. The model (1) has two control states: occupancy of buffer 1 ( $q_1$ ) and occupancy of buffer 2 ( $q_2$ ), and two input states: frequency of processor 1 ( $f_1$ ) and frequency of processor 2 ( $f_2$ ). To regulate buffer occupancy  $q_1$ , we assume that the sliding-mode controller adjusts only frequency  $f_1$  and hence  $f_2$  is fixed. Also for regulating the buffer occupancy  $q_2$  the frequency  $f_2$  needs to be adjusted by the second sliding feedback and  $f_1$  is fixed. In the following steps, we describe how to design two sliding-mode controllers for regulating  $q_1$  and  $q_2$  around their nominal values. We describe the controller design for buffer 1 and the same procedure can be followed for the second feedback rule.

#### A. Individual State-Space Model for Buffer 1

In the dual core architecture, the frequency of each processor and the corresponding supply voltages are not changing instantaneously and there is a time interval in which the frequencies and voltages are fixed. We denote this time interval as the control interval time  $T_c$  in (1). Using  $T_c$  as the length of the control interval, suppose that the minimum time requirement for one possible change in frequency is  $t_f \ll T_c$ . Assume that the sampling period needed to measure the buffer occupancy is  $t_s \ll T_c$ . We denote  $N$  as the total number of samples of the buffer occupancy and changing the frequency in  $T_c$ . Therefore, if  $\Delta t = t_f + t_s$ , then  $T_c = N\Delta t$ . Also let's assume that the demand  $\lambda$  and service rate  $\mu$  that hold for  $T_c$  are modeled as two independent and stationary random processes along the time axis [13]. Since the goal is to keep the buffer occupancy  $q_1$  fixed around the nominal value in presence of PVT variations, here we assume that frequency  $f_1$  is adjustable and  $f_2$  is fixed. The same assumption holds for buffer 2 and for stabilizing  $q_2$ , the frequency  $f_2$  is adjustable and  $f_1$  is fixed. For simplicity and without loss of generality, we divided the model (1) into two separate state-space models: one state-space for buffer 1 and one for buffer 2. The state-space model for regulating buffer 1 is defined in (2) where we use the notations

TABLE I. NOTATION USED FOR THE STATE-SPACE MODEL OF BUFFER 1

Symbol	Explanation
$x_1(t)$	$x_1(t) = q_1$ : Occupancy of buffer 1 at time $t$ where $t = \{0, \Delta t, 2\Delta t, \dots, (N-1)\Delta t, T_c\}$ .
$x_2(t)$	$x_2(t) = \dot{q}_1$ : Occupancy variation rate of buffer 1. This state has been defined to control the buffer size with more accuracy. Note that $\dot{q}_1 = \frac{q_1(k\Delta t) - q_1((k-1)\Delta t)}{\Delta t}$ where $k = \{1, 2, \dots, N\}$ .
$\bar{\lambda}_1$	Average demand (writing) rate in the whole control interval time. We assume that $\bar{\lambda}_1 = (\bar{\lambda}_1 \pm \Delta \bar{\lambda}_1)$ .
$\bar{\mu}_1$	Average service (reading) rate in the whole control interval time. We assume that $\bar{\mu}_1 = (\bar{\mu}_1 \pm \Delta \bar{\mu}_1)$ .
$(A, B)$	Matrices of the state-space model; $A$ : system matrix and $B$ : input matrix. Matrix $A$ is always fixed for all dual core systems. The system (2) is always controllable if $(\bar{\lambda}_1 \neq 0)$
$q_{ref1}$	Reference occupancy of buffer 1. The goal in buffer 1 is to adjust $f_1$ around the nominal value to compensate PVT variations and $q_1$ approaches to $q_{ref1}$ as much as possible.

defined in Table I.

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}}_A \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ \bar{\lambda}_1 \end{bmatrix}}_B [f_1(t)] - \underbrace{\begin{bmatrix} 0 \\ \bar{\mu}_1 f_2(t) \end{bmatrix}}_{C:Constant} \quad (2)$$

Now consider the model of (2) for designing the sliding feedback rule for  $f_1$ . For simplicity of formulations, let's define:

$$X = [x_1(t), x_2(t)]^T = [q_1(t), \dot{q}_1(t)]^T \quad (3)$$

and (2) can be rewritten as (4).

$$\dot{X} = AX + Bf_1 - C \quad (4)$$

### B. Modeling of PVT Variations and Uncertainties

We model all existing PVT variations, uncertainties, systematic and random variations with two extra terms in the state-space model as follows

$$\dot{X} = AX + Bf_1 - C + \underbrace{\Delta B f_1 + D_{2 \times 2} G_{2 \times 1}}_{Be} \quad (5)$$

where  $A$  and  $B$  are system matrices defined in (2) and (4),  $\Delta B$  represents systematic and random parameter variations ( $\Delta B = [0 \ \Delta \bar{\lambda}_1]^T$ ),  $G$  models other external uncertainties and PVT variations, and  $D$  is the unknown coefficient matrix related to PVT variations. Obviously, because of the random nature of PVT variations, it is not possible to model it with apparent matrices. To design a proper controller, we assume a maximum bound for unknown values and matrices. Observe that other traditional feedback controllers [14] are not able to regulate system parameters around the reference points in the presence of variations, noises, uncertainties and other unpredictable disturbances. If we assume that  $Be = \Delta B f_1 + DG$ , then we can merge all kinds of unknown PVT variations and disturbances into one term and suppose a maximum bound for all unknown terms.

### C. Designing the Sliding-Mode Feedback Controller

The procedure to design a sliding-mode controller is, first, to define a line with two control states ( $x_1(t)$  and  $x_2(t)$ ), and then, based on the desired reference point ( $q_{ref1}$  with zero derivative) find out a feedback law for  $f_1$  to move the buffer occupancy value into the line. The sliding line can be defined in a way that it ends with the reference point. As way of example and without loss of generality, suppose that the desired occupancy buffer values at control interval time  $T_c$  are  $x_1 = 5$  and  $x_2 = 0$ , then because of variations, they have different values e.g.  $x_1 = 6$  and  $x_2 = 0.5$ . In this case, the sliding line should pass the reference desired point ( $x_1, x_2$ ) = (5,0) such that the control law forces states  $x_1$  and  $x_2$  to first come into the line and then keep them staying in line while the desired reference point(5,0) is reached. Fig. 3 explains the sliding-mode feedback controller from a conceptual standpoint. The states of the system (5) ( $x_1(t)$  and  $x_2(t)$ ) start moving from the initial point (1,1) to approach the sliding line by a feedback rule. After approaching the line, the switching sliding feedback enforces both states to move through the line to reach the final desired reference point. In this experiment, the slope of the sliding line is -1 and states start moving from an arbitrary

initial point (1,1) to go to the origin (0,0). Note that these initial and final values are only example points to show the sliding-mode feedback concept. Depending on the system model, PVT variations and frequency values these points can take different values.

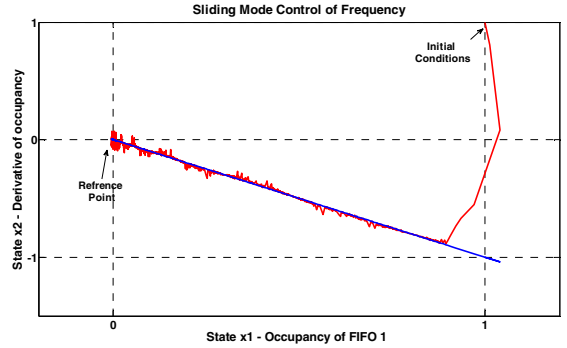


Figure 3. Moving system states through the defined sliding line

Suppose now that the maximum amount of parameter variations and state-space model uncertainties is  $\rho$ :

$$|e| \leq \rho \quad (6)$$

The value  $\rho$  represents the maximum of PVT variations and state-space model uncertainties that affects the buffer occupancy 1. To derive a proper feedback controller to stabilize the state-space (5), we use the Lyapunov theory presented in [12]. The following theorem describes how to design the sliding feedback law for  $f_1$  to compensate unknown PVT variations and to model uncertainties besides stabilizing the buffer size.

**Theorem-** Consider the state-space model of buffer occupancy 1 controlled by frequency  $f_1$  (and/or supply voltage) as (5) and suppose that the maximum amount of PVT variations and model uncertainties is as (6). If the frequency value of processor 2 is fixed, the feedback rule (7) for  $f_1$  stabilizes the occupancy of buffer 1 in the dual core architecture.

$$f_1 = -(SB)^{-1}(SAX - C) - \rho \cdot \text{sgn}(\sigma SB) \quad (7)$$

where  $\sigma = SX$  is the equation of the sliding line, matrix  $S = [m \ 1]$  and  $m$  is an arbitrary value determined by the designer. Also  $\text{sgn}(\sigma SB)$  in (7) is a sign function with the following definition:

$$\text{sgn}(\sigma SB) = \begin{cases} 1 & \text{if } \sigma SB > 0 \\ -1 & \text{if } \sigma SB < 0 \end{cases} \quad (8)$$

Rule (7) can regulate the buffer occupancy 1 to the desired reference points even if it has initial values far from the desired ones. The value of  $m$  can be changed by the designer. Consider Fig. 2, which shows the proposed closed loop controller configuration to compensate PVT variations. DVFS determines the voltage and frequency values of each processor. Based on a determined  $(V_1, f_1)$  and  $(V_2, f_2)$ , the occupancy of buffer 1, for example, is  $q_{ref1}$ . The sliding controller measures the occupancy of buffer 1 as  $(q_{ref1} \pm \Delta x_1)$ . The term  $\Delta x_1$  is because of PVT variations. Then, the sliding controller changes the clock frequency as (7) to make the term  $\Delta x_1$  smaller as

much as possible and to compensate PVT variations. In (7), there exists only one free parameter  $m$  that should be modified by designer for each application. The parameter  $m$  can be changed to find the best control rule in sense of PVT rejection.

**Proof-** Select the Lyapanov function as  $V = 0.5\sigma^2$ . The first derivative of  $V$  with respect to time is

$$\dot{V} = \sigma\dot{\sigma} \quad (9)$$

and based on Lyapanov theory, if  $\dot{V} < 0$ , then the system (5) is stable. The Lyapanov function is a positive function corresponding to systems states  $X = (x_1, x_2)$ . It is not a unique function and designers can define other Lyapanov functions for the system and get different control rules. For calculating  $\dot{\sigma}$ , we use the definition of the sliding line and use (5), and then we have:

$$\dot{\sigma} = S\dot{X} = S(A\dot{X} + Bf_1 - C + Be) \quad (10)$$

We divide the feedback control law into two parts:

$$f_1 = f_{1k} + f_{1u} \quad (11)$$

where  $f_{1k}$  is the feedback control frequency for known part of the model without considering PVT variations and model uncertainties, and  $f_{1u}$  is the feedback control frequency for unknown part of the model. Hence we can rewrite (10) as

$$\dot{\sigma} = \underbrace{SAX + SBf_{1k} - C}_{\text{known}} + \underbrace{SBf_{1u} + SBe}_{\text{unknown}} \quad (12)$$

From (12) it is possible to find  $f_{1k}$  as

$$SAX + SBf_{1k} - C = 0 \Rightarrow f_{1k} = -(SB)^{-1}(SAX - C) \quad (13)$$

Therefore, the derivative of the Lyapanov function changes as

$$\dot{V} = \sigma\dot{\sigma} = \sigma SBf_{1u} + \sigma SBe \quad (14)$$

Then we always have:

$$\sigma\dot{\sigma} = \sigma SBf_{1u} + \sigma SBe \leq \sigma SBf_{1u} + |\sigma SBe| \leq \sigma SBf_{1u} + |\sigma SB||e| \quad (15)$$

Since we defined maximum amount of PVT variations in (6),  $|e| \leq \rho$ , then in the worst case we have:

$$\sigma\dot{\sigma} \leq \sigma SBf_{1u} + |\sigma SB||e| \leq \sigma SBf_{1u} + |\sigma SB|\rho \quad (16)$$

by choosing  $f_{1u}$  as

$$\sigma SBf_{1u} = -|\sigma SB|\rho \Rightarrow f_{1u} = -\rho \frac{|\sigma SB|}{\sigma SB} = -\rho \cdot \text{sgn}(\sigma SB) \quad (17)$$

The Lyapanov function will always be zero (in case of  $|e| = \rho$ ) or negative (in case of  $|e| < \rho$ ) and the theorem is proved. Therefore, using (7) with choosing a proper  $m$  and  $\rho$  values results in stabilizing buffer occupancy 1 around the desired reference value.

#### IV. RESULTS

In this section, we evaluate the performance of the proposed sliding-mode feedback rule (7) in the presence of PVT variations by executing different experiments. We first simulate a state-space model for a dual core system and two FIFOs in between with numerical parameters presented in

TABLE II. NUMERICAL VALUES OF THE FIRST EXPERIMENT: DESIGN SLIDING FEEDBACK TO REGULATE BUFFER 1 AND 2

PARAMETER	Explanations
$A = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}$ , $B_1 = B_2 = \begin{bmatrix} 0 \\ 0.9 \end{bmatrix}$	System matrices ( $A, B$ ) are defined as (2). Note that matrix $A$ is fixed for all buffer models.
$S_1 = [m_1 \ 1]$ , $S_2 = [m_2 \ 1]$	Sliding lines defined by the designer. For each buffer off-line profiling should be done to find the best $m$ values. We select $m_1 = m_2 = 1$ .
$C_1 = \begin{bmatrix} 0 \\ 0.1 \end{bmatrix} f_2$ $C_2 = \begin{bmatrix} 0 \\ 0.1 \end{bmatrix} f_1$	Matrix $C$ mentioned in (5)–This is important to mention that we assumed that the speeds of two-processors are same ( $f_1 = f_2$ ) in this experiment.
$e_1 = e_2 = 30 \sin(t)$	Disturbance signal: this models PVT variations that affect the system parameters.
$\rho_1 = \rho_2 = 30$	Maximum amount of PVT variations – the value 30 means that PVT variations change the system parameters with $\pm 30\%$ of the nominal values.
$\bar{\lambda}_1 = \bar{\mu}_2 = 0.9$ , $\bar{\mu}_1 = \bar{\lambda}_2 = 0.1$	Assumption for the average of writing and reading in each buffer.
$T_c = 100\Delta t$	This assumption allows to sample the occupancy of buffers 100 times per each control interval

Table II. In this experiment, we show how the sliding controller regulates the occupancy of buffers around the nominal reference values. The controller is designed based on (7) and the buffer occupancy results of this experiment are shown in Fig. 4 and Fig. 5. The occupancy of FIFO 1 in one control interval time is shown in Fig. 4 and the occupancy of FIFO 2 is shown in Fig. 5. The sliding-mode feedback rules move the occupancies from unstable conditions to the stable ones and stabilize them around desired reference values. Different desired values depend on the frequency values of two processors and writing-reading coefficients. In this experiment, we assume that PVT variations affect nominal system parameters as shown in Fig. 6. Note that since the initial conditions are far from the reference points, it takes around  $40\Delta t$  for the sliding feedbacks to regulate the buffer

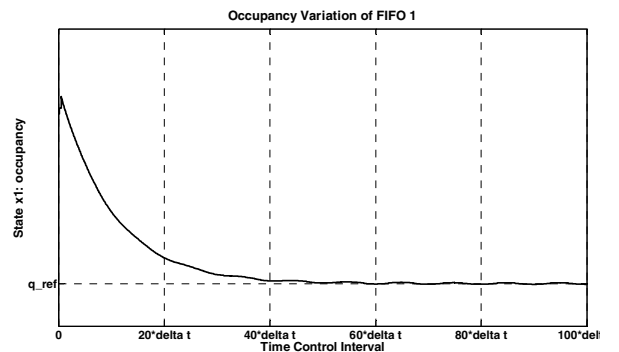


Figure 4. Occupancy of FIFO 1 controlled by the sliding-feedback rule  $f_1$  in one control interval time

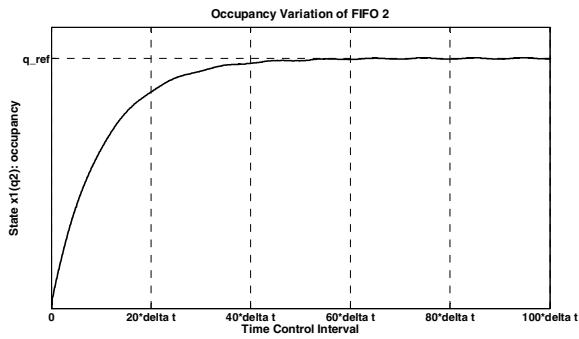


Figure 5. Occupancy of FIFO 2 regulated by the sliding-feedback rule  $f_2$

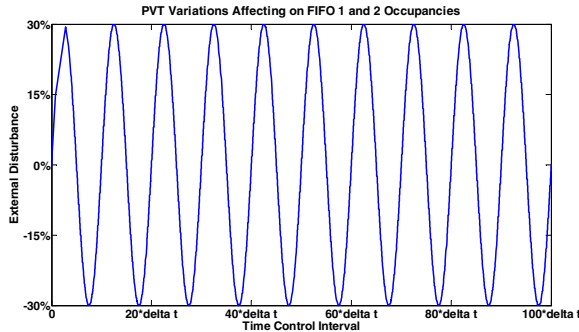


Figure 6. PVT variations used for evaluating the effectiveness of the sliding-mode controller

occupancies. For the purpose of evaluating the controller, in this experiment, we only assume that sinusoidal wave PVT variations affect the buffer occupations in the system. Other experiments (not shown in this paper for the sake of space) confirm that if the shape of the PVT variation changes, the buffer occupancy is tuned accordingly. It is worth mentioning that in case the maximum PVT variations increase to a value more than 30% of the nominal occupancy value, the buffer occupancy starts to oscillate around its reference value. In this case, the sliding-feedback cannot stabilize it, unless the PVT variation decreases to a value less than 30% of the nominal value. Also, the choice of parameter  $m$  as the slope of the sliding line plays an important rule on the operation of the controller. In this experiment if a negative value had been chosen, the controller would break and destabilize the system.

In the proposed sliding rule (7), it is assumed that  $f_2$  is fixed and  $f_1$  is controllable. Likewise, for designing a sliding feedback rule for  $f_2$ , it is assumed that  $f_1$  is fixed. In practice, these two frequencies change instantaneously together and they may disturb each other's behavior. Despite the apparent fact that the sliding rules designed for  $f_1$  and  $f_2$  don't take into account each other's interaction between frequencies, there is no possibility that a positive feedback happens to destabilize buffer occupancy. If for example buffer occupancy 1 increases, in practice, it means that PVT variations are causing the system to increase  $f_1$  or to decrease  $f_2$ . In this case, the first sliding-mode controller starts reducing  $f_1$  (to regulate buffer occupancy 1), while the second sliding controller starts increasing  $f_2$  (to regulate buffer occupancy 2). Similarly, both controllers operate in opposite directions to compensate PVT variations when buffer occupancy 1 decreases. When both

sliding feedbacks work instantaneously, the number of frequency switchings in each time interval increases since each increase or decrease of  $f_1(f_2)$  affects the occupancy of buffer 2 (buffer 1). As an example consider the previous experiment. Frequency  $f_1$  which regulates the occupancy of buffer 1 is shown in Fig. 7 in the presence of PVT variations. In this case, both frequencies are controlled by sliding-feedback rules. When  $f_1$  and  $f_2$  change together, each feedback rule adapts itself with new variations. Therefore, both sliding rules have more changes of the nominal parameters. Now assume that  $f_2$  is not controlled by the second sliding-controller and that it is fixed. In this case frequency  $f_1$  changes only due to PVT variations and it turns into the shape shown in Fig. 8 with much less switching activities.

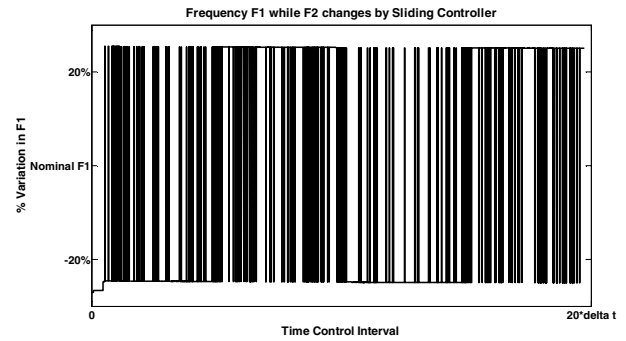


Figure 7. Frequency  $f_1$  when  $f_2$  is also controlling by sliding rule

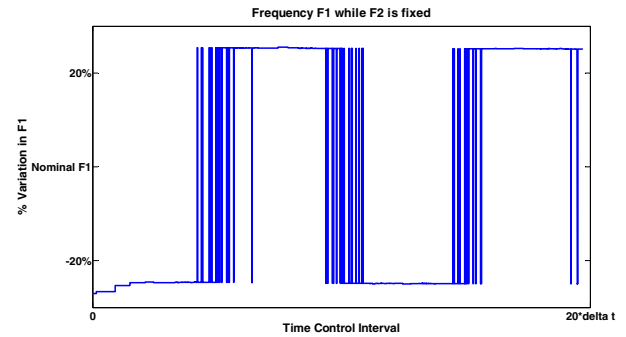


Figure 8. Frequency  $f_1$  when  $f_2$  is fixed

#### A. FPGA Implementation of the Two Processor Controlled System

We also implemented the sliding-controller in an Altera Stratix II FPGA. We mapped the platform of Fig. 1 with two processors and a shared-memory in between as the buffer into the FPGA. We selected a JPEG decoding application as our benchmark set-up to evaluate the controller efficiency. The first processor receives input pictures from a JPEG-coded stream to decode them later and to send them into the second processor. The second processor reads the decoded stream's data from the shared-memory to execute an image processing application (e.g. edge detection, face detection). In this experiment the goal is to apply the sliding-feedback to control the shared-memory size in the presence of PVT variations. The shared-memory size depends on the image size which is in VGA format (640×480 pixels). Each processor works with the nominal voltage of 1.2 V and a nominal frequency of 50 MHz. In this



experiment we measure the memory size and compare it with the reference size, then adjust  $f_1$  based on the feedback rule (7). The worst case execution time (WCET) to execute one JPEG decoding application in this experiment is 1.5msec. We also choose the sampling time as  $\Delta t = 1.5$  msec. We assume that less than 2% variations in the nominal size value of the memory is acceptable. For more than 2% variations, the feedback rule should change the frequency to compensate PVT variations and compels the size of the memory to turn back to its reference value. We produced a random PVT variation signal that can influence the operation of the processors by a maximum of 20% variation of the nominal frequency values. The experimental results of applying the sliding-mode feedback to the two-processor architecture are shown in Fig. 9 and Fig. 10. The PVT variations and the regulated size of the memory are shown in Fig. 9. Also, Fig. 10 shows the sliding-feedback rule for the frequency of processor 1 which changes based on the memory size variations. The feedback rule regulates the memory size based on the maximum amount of parameter variations. In the sliding-feedback rule (7), there is always the possibility of defining different boundaries for  $\rho$  to speed up the buffer size's regulating process. For example in this experiment we define three boundaries for  $\rho$ :  $\rho = 2\%$ ,  $\rho = 10\%$  and  $\rho = 20\%$  of the nominal memory size. If the variations are less than 20% and more than 10%, then the controller changes frequency with the steps of 10%. And if the variations are less than 10% and more than 2% of the nominal values, then the controller changes frequency with the steps of 2%. Consider the memory size at time  $t = 2\Delta t$  in Fig. 9 where the memory size is affected by 18% PVT variations. It means that the frequency  $f_1$  has a value 18% more than its nominal value (59MHz) at time  $2\Delta t$ . The sliding-feedback, at

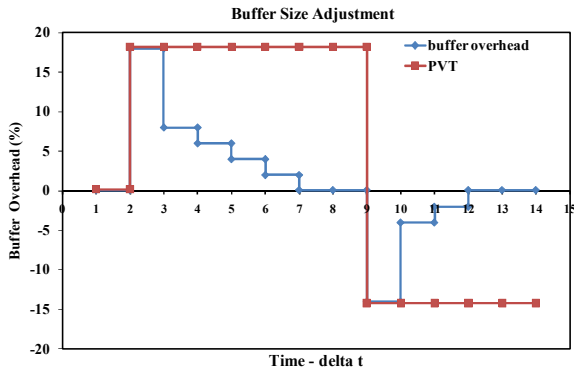


Figure 9. Memory size of the experimental setup affected by PVT variations

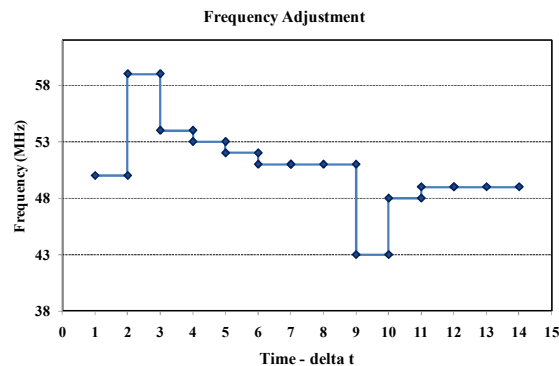


Figure 10. Frequency  $f_1$  adjusted by sliding-feedback controller

this time, reduces the frequency with a factor of -10% and sets  $f_1 = 54$  MHz. Since there is a linear relationship between the frequency and memory size, at time  $3\Delta t$  the memory size will be 8% more than its nominal value. At this time, the controller measures the memory size and since it is less than 10% of the nominal value, it starts then reducing the frequency with steps of 2% with regards to 50 MHz. Therefore at the end, after  $5\Delta t$ , the controller compensates 18% PVT variations.

## V. CONCLUSIONS

We presented a robust feedback controller to protect dual core systems against PVT variations. The controller measures buffer occupancies and adjusts frequency of processors in the neighborhood of their nominal values to compensate PVT variations. The stability of the feedback rules was proved using the Lyapanov theory. The proposed feedback can be extended to use in different similar architectures e.g. network on chips to stabilize them against uncertainties and variations in the design parameters.

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