Accelerators and emulators: Can they become the platform of choice for hardware verification?

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Abstract— **The verification of modern hardware designs requires an enormous amount of simulation resources. A growing trend in the industry is the use of accelerators and emulators to support this effort.**

Because they are very fast compared to software simulators, accelerators and emulators provide the opportunity to significantly shorten the verification cycle. However, for this to happen challenges in all main aspects of the verification process (test-generation, checking, coverage and debugging) will first need to be solved.

In this panel session, experts from both academia and industry (EDA vendors and users) will come together to present their ideas and experiences on how to best utilize accelerators and emulators to enhance the verification process.

PANELISTS

Ronny Morad, Manager, System Verification Technologies, IBM Research – Haifa, Israel

Acceleration (and emulation) platforms are located in the middle between simulation and post-silicon platforms with respect to characteristics such as simulation speed, observability and adaptability to design changes. However, most verification solutions applied to acceleration platforms are taken either from simulation or from the post-silicon domain, hence do not fully exploit acceleration's unique characteristics. I will present research ideas and recent results that demonstrate how to effectively leverage these platforms.

Bodo Hoppe, Senior Technical Staff Member Hardware Verification, IBM Research & Development, Germany

An effective verification methodology that utilizes acceleration platforms needs to address test-generation as well as debug and analysis. Open operating systems like Linux are a good platform for overcoming these challenges. Efficient test-case generation can be done on top of the components' drivers, while reference models are crucial for result prediction. This approach also allows post-silicon validation, and enables remote debugging using tools like GDB.

Jai Kumar, System Validation Architect, Intel Corporation, USA

There are numerous practical challenges/roadblocks in enabling a "shift-left" of HW/SW validation. Having used these hardware-based validation platforms for couple of decades now, I have not seen much advancement. Platform vendors have to scale to new heights to improve the ease-of-use while reducing total cost of deployment. In addition a big change in mindset is required to enable the methodology leap required to facilitate a full-scale leverage of these expensive hardware platforms.

Frank Schirrmeister, Group Director, Marketing, System Development Suite, Cadence Design Systems - CA, USA

Our design and verification vision utilizes a continuum of platforms - from simulation at the transaction and signal-level to emulation and acceleration. The integrated flow will need to deliver scalability across platforms, connecting design and verification flows using a high performance and flexible modeling environment. It will need to keep track of coverage and functional metrics and be able to measure and verify low-power requirements for both hardware and software teams.

Professor Subhasish Mitra, Stanford University, USA

I will focus on the need for transforming "hardware-based" validation (emulator-based validation and post-silicon validation) from an "art" to a "structured" methodology with a solid foundation. I will discuss how accelerators can enable "quicker adoption" of certain classes of systematic solutions to achieve this objective. At the same time, accelerators bring their own set of challenges that will create exciting research opportunities involving "Design for Acceleration" to significantly advance the state-of-the-art. Finally, I will stress the need for "bug benchmarks."

Luc Burgun, CEO and President, EVE, France

Hardware emulation is enjoying a renaissance. After several years of being confined to verifying only ultra-large designs in the processor and graphics space of the electronic industry, at the end of the last decade it has captured the center stage in the design verification process of virtually any type of design. Quarter after quarter, all the major players have been reporting record sales. I will focus on a market analysis of hardware-assisted verification, highlighting the reasons for the recent success of this unique verification technology. I will also explain why the success will continue throughout this decade.

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