

Challenges in Verifying an Integrated 3D Design

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Abstract — the integrated 3D configuration considered in this study includes a silicon die on one side of an organic interposer and a different die on the other side. The three parts are from three different design environments, each has its own database and description language not compatible with the other two. The incompatibility triggered a search for a new methodology for the physical verification of the 3D configuration. Application scripts were developed and successfully used to verify the physical connections within the complex design of the interposer, which accommodates 1600 signals and 12,000 traces for connecting the signals between the two chips. The layout of 56,000 vias for power and signal was also verified to meet the requirements for the manufacturing of the organic interposer.

Keywords - 3D design; verification; integration; system design

I. INTRODUCTION

The silicon design environment for analog and digital circuits is traditionally operated independent of the system design environment for PCB and package. Tools in a silicon design environment can perform highly automated ASIC place-and-route, handle complex digital design flow and integrate analog and digital designs on the same silicon die. Tools in a system design environment are used to handle a larger physical boundary that encloses one or more active components such as a SoC and/or DRAM dies. System designers have to consider the details in the substrate that provides high quality I/O and power connections to a silicon die, and the PCB that supports signal transmission between the packages.

While both design environments are very effective in generating 2D designs independently, many new challenges arise when the designs are integrated to form a 3D system. The observations presented in this paper are a reflection of the challenges that designers face prior to or during their transition to a 3D design environment. The transition needs time for the development, investment and learning of new design tools [1] [2].

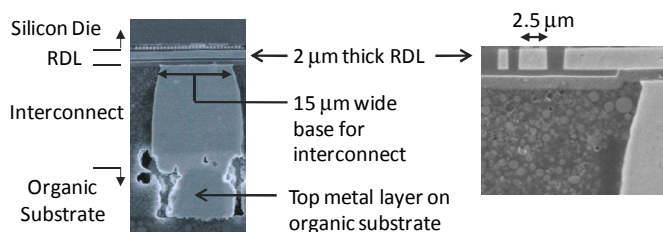


Figure 1. Dimensions of the feature geometries in RDL, substrate and their interconnection are converging.

Small interconnections in high density between a die and its substrate are common in the latest mobile SoC package because of

CMOS process shrink. Figure 1 shows a cross section of a SoC in which the feature sizes of the geometries in the re-distribution layer (RDL), and the solder bumps range from 1 μm to 15 μm. Such dimensions suggest that the smallest feature size on a substrate created in the system design environment is approaching the largest feature size in a RDL created in the silicon design environment. Hence, a RDL can be designed by either a substrate or silicon designer using tools in their respective environments [1].

II. COMPLEXITY OF 3D DESIGN

The generic 3D design considered in this study is made up of three different designs as shown in Figure 2. Design #1 is a SoC with groups of I/O cells. Design #2 is an organic interposer from a system/package design environment. Design #3 is a memory/peripheral device generated in a different silicon design environment in another company.

The design of the interposer in the 3D configuration is at least 100 times more complex than a typical substrate for a single-die mobile SoC package. It has a RDL on its top surface and another on the bottom, and it provides continuous signal paths connecting the I/O of the top die and bottom die. In addition, power supplies are distributed through the interposer to the circuits on both sides. The number of metal layers and the complexity within a layer scale nonlinearly with the number of connections for I/O, power supplies and ground.



Figure 2. An integrated 3D system comprises 2D designs from three different sources.

The difficulties in the integration and verification of the system are at the two physical interfaces A and B as shown in Figure 2. The databases of the three designs are not communicable among the three design environments due to differences in their description languages, including format and naming convention. Communicating the changes in one design to the other two designs requires additional tools that are not readily available, and therefore needed to be developed.

III. VERIFYING PHYSICAL CONNECTIONS

A. Misalignment of Connection Points

In the traditional 2D design flow, the package design environment and silicon design environment are isolated. Prior to any design activities for a package containing one die and one substrate, designers from both sides would agree upon a particular

floor plan and escape routing for feasibility and planning purposes. In general there is no iterative design activity between the two environments during the design process. Minimum communication is needed to update any changes in the coordinates of the interconnections between the die and substrate.

In recent mobile SoC packages, over 1500 interconnections in high density and fine pitch are common [3]. Figure 3 illustrates misalignment due to cumulative errors in the coordinates of 110 consecutive interconnections.

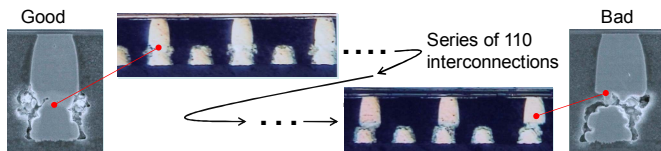


Figure 3. Misalignment of soldered connections resulted from the cumulative errors in the coordinates of 110 interconnections (from left to right side of figure).

B. Application Scripts for Physical Verification

Silicon design tools are for designing highly integrated circuits for a foundry to manufacture chips, while system design tools are for designing substrates for packaging the chips. The process of integrating the 3D system in Figure 2 has turned many of the independently handled areas, such as signal quality and power delivery networks, into co-design topics [4] that call for iterations between the package and silicon design environments. The lack of a common description language severely hampered the important task of physical and functional verification. In response, application scripts were developed to speed up the verification of physical connectivity of the interposer to the SoC and memory silicon.

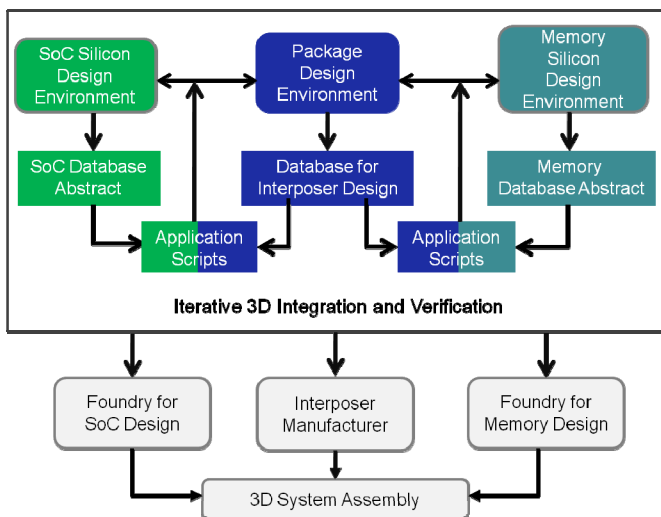


Figure 4. Application scripts for physical verification are used to enable the iterative design flow of a 3D integrated system.

Figure 4 illustrates the iterative process enabled by the application scripts. At the beginning of the design process, the design teams for the interposer, SoC and memory agreed upon the logical connections, which then become the reference for physical verification. The first step in verifying a revision of the SoC or memory design is to extract an ASCII representation from the

database of the design. A script for the verification of physical connections arranges the ASCII data in a format that can be used to compare with data from the interposer design, and verifies all the logical connections. Mismatches in the coordinates of the physical connections are returned to the respective design environment for update. If there is no mismatch, the latest data set becomes the reference for the next design iteration.

The script has successfully verified an interposer design that consists of an organic substrate and two RDLs. The interposer has over 12000 traces and 26000 vias connecting 1600 signals between to the RDLs. It also has 30,000 vias for power supplies. The overall size of the design is 35 mm x 35 mm. Another script was developed to verify the layout of the vias meeting the requirements imposed by the substrate manufacturer.

Although the application scripts can bridge the gap between the silicon and package design environments, it is technically desirable to have a new design environment, as illustrated in Figure 5, that can host the design of package, substrate, interposer and silicon simultaneously or separately. System and silicon designers can work on the same complex 3D configuration using tools for partitioning, automation, integration and verification. The environment can generate the data files in the formats that are suitable for fabricating the different parts by their respective manufacturers.

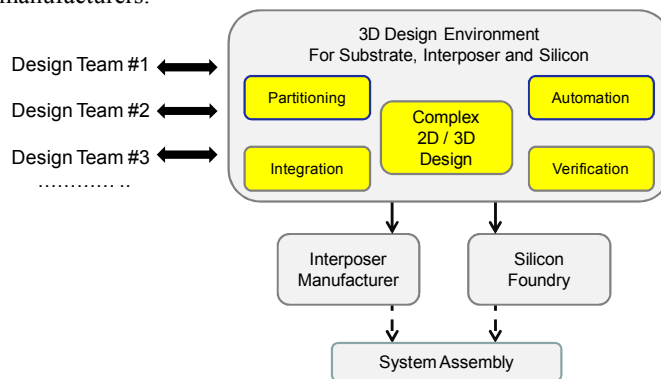


Figure 5. An ideal 3D design environment hosts substrate, silicon and interposer design simultaneously.

IV. CONCLUSION

Until the ideal 3D design environment becomes available, integrating parts from multiple sources to form 3D systems will continue to be hindered by the incompatible description languages of different design environments. Application scripts or other cost effective means for physical verification are needed to enable the iterative design process.

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