

Investigating the Effects of Inverted Temperature Dependence (ITD) on Clock Distribution Networks

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Abstract—The aggressive scaling of CMOS technology toward nanometer lengths contributed to the surfacing of many effects that were not appreciable at the micrometer regime. Among them, Inverted Temperature Dependence (ITD) is certainly the most unusual. It manifests itself as a speed up of CMOS gates when the temperature increases, resulting in a reversal of the worst-case condition, i.e., CMOS gates show the largest delay at low temperatures. On the other hand, for metal interconnects an high temperature still holds as worst case condition. The two contrasting behaviors may invalidate the results obtained through standard design flow which do not consider temperature as an explicit variable in their optimizations.

In this paper we focus on the impact of ITD on clock distribution networks (CDN), whose function is vital to guarantee the synchronization among physically spaced sequential components of digital circuits. Using our simulation framework, we characterized the thermal behavior of a clock tree mapped onto an industrial 65nm CMOS technology and obtained using a standard synthesis tool. Results demonstrate the presence of ITD at low operating voltages and open new potential research scenarios into the EDA field.

I. INTRODUCTION

At the nanometer regime, the dramatic growth of the power consumption, and in particular of the power density (i.e., the power consumed per unit area), induced sensible increase of both on-chip peak temperatures and thermal gradients. Such adverse thermal profiles are well known to have deleterious effects on the electrical characteristics of digital components. On the interconnect side, it has been observed that propagation delay across the wires increases as temperature rises [1]; considering CMOS gates, instead, the delay-temperature relationship gets more complex, and, as proven in recent works (e.g., [2]), CMOS gates may experience an inversion of the temperature dependence, i.e., cells get faster as temperature increases.

Under these conditions, the assumption that worst-case delay occurs at high temperature may no longer holds, and *slow* corners (typically assumed at high temperature) may coincide with low temperatures. Needless to say this complicates many timing-driven design stages and optimization phases. The authors of [3], for instance, have shown that, since ITD essentially invalidates the standard approach of defining corners, it results more difficult to find shortest and longest paths during Static Timing Analysis and sign-off.

Moving on the same direction, in this work we examined the effects induced by ITD during the synthesis of the clock distribution network (CDN), well known to be critical component for the functionality of digital circuits. CDNs consist

of buffered global interconnects routed in the top metal layers with a tree-like shape that traverse the whole chip area. Since CDNs are essential for the correct operation of synchronous circuits, it is important to avoid race conditions between paths, i.e., avoid that clock edges reach various circuit registers at different times. ITD may induce unexpected clock skew variations that standard corner-based design tools are not able to track. On the contrary, our clock skew modeling method, which is applied at post clock tree synthesis, takes into account temperature-induced path delay variations. Our framework has been applied on a benchmark circuit implemented in a 65nm technology to analyze the impact of ITD on clock skew, considering temperature effect on both the active devices and the interconnect system under different supply voltages.

II. INVERTED TEMPERATURE DEPENDENCE

The *alpha-power* law [4] is commonly used to model the propagation delay T_p of CMOS transistor, expressed as:

$$T_p \propto \frac{C_{out}V_{dd}}{I_d} = \frac{C_{out}V_{dd}}{\mu(T)(V_{dd} - V_{th}(T))^\alpha} \quad (1)$$

where C_{out} is the output load capacitance and I_d is the ON state drain current. Two important parameters are strongly dependent on temperature: Threshold voltage $V_{th}(T)$ and carrier mobility $\mu(T)$. Both threshold voltage and carrier mobility decrease with increasing temperature, however (1) shows that they have opposite consequences on the drain current. Depending on the supply voltage and temperature values, the final drain current is determined by the prevailing parameter of the two. At high voltages, $V_{dd} - V_{th}$ becomes less sensitive to thermally-induced variation of V_{th} , and then mobility determines the drain current. At low voltages, $V_{dd} - V_{th}$ decreases making it more sensitive to changes in V_{th} . Hence higher temperature increases the delay at high voltages, but decreases the delay at low voltages. In other words, depending on the magnitude of V_{dd} , the delay increases or decreases as temperature grows. This phenomenon is referred to as *Inverted Temperature Dependence* (ITD) and the voltage, where temperature dependence inverts, is called zero-temperature coefficient (ZTC) voltage V_{ZTC} .

III. THERMAL-AWARE CLOCK-SKEW SIMULATOR

The framework developed for clock skew simulation is based on a SPICE-level simulator and works after CTS. This means that the design is already synthesized and placed, as well as the CDN is completely all over the circuit. The tool takes as input the physical design information, the detailed parasitic

data available in the SPEF format, the circuit thermal map, and the SPICE models provided by the silicon vendor of our technology library. Customized TCL scripts use these data to generate a SPICE-level netlist of the clock tree. Active devices (buffer cells) and interconnects (RC networks) make up the clock tree netlist. The sinks (flip-flops) are modeled as load capacitances, using the datasheet provided by the silicon vendor. An ideal supply voltage feeds the clock input with an ideal clock signal. The thermal map is analyzed in order to set correct temperature values for buffers, while temperature of RC elements is computed with the wire thermal profile proposed in [5], that considers also the self-heating effect. Then a temperature-driven delay simulation is performed using Synopsys HSPICE. When the simulation ends, the tool produces a final report showing values of the clock skew, the longest and shortest timing paths, and also the maximum and the minimum arrival time of all the buffers at each level of the clock tree.

IV. A CASE STUDY

The proposed tool has been applied on a configurable synthetic benchmark circuit *SYNTH* mapped onto an industrial 65nm technology library provided by STMicroelectronics. The circuit is a two dimensional grid of “micro-heater” blocks, each one made up of a variable number of different sized parallel inverter chains. The clock tree consists of 184 buffers and 4800 sinks.

Fig. 1 shows the propagation delay of the clock-edge across the longest path of the clock tree as a function of supply voltage. The delay is plotted for different operating temperatures: $-40^{\circ}C$ up to $125^{\circ}C$.

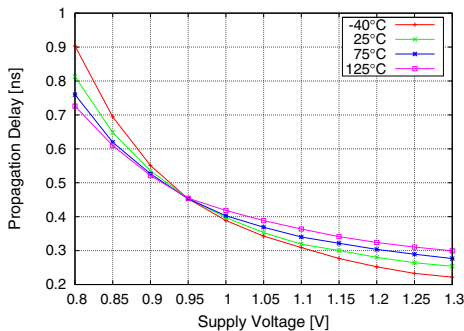


Fig. 1. Propagation delay of longest path vs. supply voltage for increasing temperatures.

The obtained results confirm the presence of the ITD. The simulated value for V_{ZTC} is around $0.95V$. When powered with $V_{dd} \geq V_{ZTC}$, transistors show a direct temperature dependence (i.e., get slower as temperature increases) and the slow corner is at high temperature (line at $125^{\circ}C$). When $V_{dd} \leq V_{ZTC}$, ITD appears and the slowest corner manifests itself at low temperature (line at $-40^{\circ}C$). To notice that the results plotted in Fig. 1 also include the thermally induced delay degradation across the metal wires.

Fig. 2 shows the clock skew as a function of temperature for a subset of typical supply voltages. Under the assumption of direct temperature dependence (i.e., $V_{dd} \geq V_{ZTC}$), the

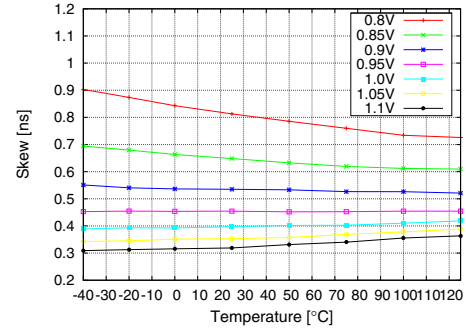


Fig. 2. Clock skew vs. temperature for increasing voltages.

slope of all the lines is positive, i.e., clock-skew increases as temperature increases. For V_{dd} in the range $[0.9 - 1.0]$, the clock-skew is almost insensitive to temperature fluctuations (i.e., flat line). Finally, if ITD appears (i.e., $V_{dd} \leq V_{ZTC}$) the clock-skew shows a negative monotonicity and the worst case appears at low-temperature. It is worth mentioning that the plotted results include the thermal effects on the metal interconnects.

These results, which highlight once again that the worst case temperature may shift from low to high temperatures depending on the actual supply voltage, leave a huge number of open issues that might request further investigation. First and foremost it is important to understand after what point the inverted temperature dependence imposed by the buffers dominates that of the interconnects. Second, if it possible to identify a-priori the V_{ZTC} point below which the clock-tree shows ITD; this is essential to check the timing compliance during the optimization loop of the CTS. Third, if it is possible to exploit the ITD to generate temperature insensitive clock-tree.

V. CONCLUSIONS

In this paper we examined an emerging phenomenon as the inverted temperature dependence and its effects on clock distribution networks. We developed a temperature-aware methodology to analyze thermally-induced clock skew. Testing our methodology on a benchmark circuit, we showed the presence of ITD and the necessity of a deeper timing analysis to ensure timing constraints over the supply voltage/temperature range. As future work, we are exploring how thermal gradients on the die may vary the impact of ITD on clock tree.

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