BEYOND CMOS – BENCHMARKING FOR FUTURE TECHNOLOGIES

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Abstract— **The interaction between the design and the technology research communities working in nanoelectronics, and especially in the Beyond CMOS area, is characterised by a diversity of terminologies, modi operandi and the absence of a consensus on main priorities. We present the findings of the EU project NANO-TEC to date, in the quest to bring together these communities for the benefit of a stronger European Research Area. Through this, we present a summary of technology trends and a preliminary benchmarking analysis for a subset of these as an example of the project work. We summarise relevant design issues concerning these technologies and conclude with recommendations to bridge this design-technology gap.**

Keywords-componen: nanoelectronics, Beyond CMOS, design-technology gap

I. INTRODUCTION

Most experts agree that scaling CMOS technology is coming to an end in the next decades. The questions asked are then: what will come after CMOS? What kind of technology could be used instead? Will Europe play an important role in beyond CMOS technologies and thus have a significant market share with jobs using emerging technologies? And if not, what will happen to European industries in sectors such as the automotive and energy ones, which heavily depend on electronic system competences?

For the imminent generation of devices and systems, design and technology go hand in hand in industrial R&D. However, for future generations in nanoelectronics, design and technology are not sufficiently integrated to ensure a fast exploitation in the form of products. The capability of Europe to transfer and exploit research results in nanoelectronics depends on the availability of integrated solutions provided by a joint design and technology community.

Under the ICT theme of FP7 a Coordination Action, "Ecosystems Technology and Design for Nanoelectronics" (NANO-TEC, project number 257964, www.fp7-nanotec.eu), is funded by the European Commission. It intends to respond to this need having two main objectives:

- Identify the next generation of (emerging) device concepts and technologies for ICT.
- Build a joint technology-design community to coordinate research efforts in nanoelectronics in Europe.

II. CONCEPT

The relationship between technology and design in nanoelectronics is seen in the project NANO-TEC as a mutually dependent two-block partnership. Consider a function of relevance to Beyond CMOS, which comes out of the myriad of possibilities arising from the fast progress in material sciences, coupled to developments in the control of morphology and or the nanostructuring of these materials. A crucial next step is to find a way to link this function to an established, or a new, logic. For this logic to work, ideas on design and architecture are needed. In this basic frame of analysis, design plays a key enabling role in the latter two steps, as well as in the consideration of the way the information-related function, based on of these new materials and (nano) structures, is linked to a logic system.

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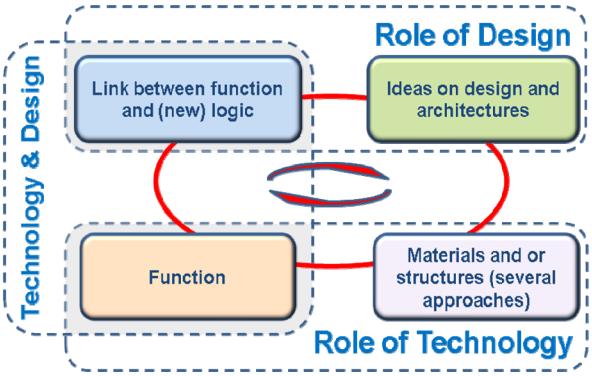

Figure 1. The NANO-TEC project concept.

III. METHODOLOGY

The main channel to reach the objectives of NANO-TEC are a series of workshops with invited international experts, mainly from Europe and some from the Americas and Asia, covering topics such as beyond CMOS device concepts and design, benchmarking and a SWOT analysis of new devices. The 3rd workshop in this series, on the SWOT analysis, will take place in May 2012. The first workshop sought to identify emerging nanoelectronic technologies and the Designs for new devices to work. These are discussed in section IV below. The 2nd Workshop focused on benchmarking of these and a few more emerging technologies and the preliminary outcome is discussed in section V below with two examples. The sessions had an invited speaker, a discussant and a rapporteur as well as a working group per topic which discussed in more detail the benchmarking aspects. Each workshop had a Panel discussion focusing on Design issues and the bridge to technology. Each workshop had about 70 researchers attending. Participation has been open to all EU ICT project coordinators and partners as well as to the nanoelectronic community in Europe, e.g. ENIAC Scientific Community Council, SINANO Institute, ENI2 consortium partners, and the Design European Networks. The presentations of speakersm discussants and rapporteurs can be found in the above-mentioned project web site.

IV. TECHNOLOGY TRENDS IN BEYOND CMOS

The discussion on trends benefitted from an excellent overview on Nanoelectronics given by Jeffrey Welser (Semiconductor Research Council and IBM) coming from a series of global workshops held in 2010 organised by the National Science Foundation and the National Nanotechnology Initiative [1]. In particular, the USA Semiconductor Research Council and the Nanoelectronics Research Initiative have identified five research vectors:

- New devices: Devices with alternative state vector.
- New ways to connect devices: Non-charge data transfer.
- New methods for computation: non-equilibrium systems.
- New methods to manage heat: Nanoscale phonon engineering
- New methods of fabrication: Directed self-assembly.

The approach followed by NANO-TEC concentrates on specific emerging technologies, namely

A. *Carbon-based electronics*

The unique and versatile physical properties of graphene, make it the preferred material in this group for future electronics and electronics-related applications. Devices already demonstrated include MOSFET with record mobility and transconductance as well as THz devices. Large area flexible electronic applications have also been demonstrated [2]. It is generally agreed that graphene will find several applications in the More than Moore area. The main issues with graphene were identified as (i) the need to engineer a stable and uniform non-zero gap graphene, i.e., bilayer graphene, (ii) its manufacturability and (iii) integration with existing Si CMOS.

B. *Silicon-based electronics*

This is the current dominant technology which upon further scaling faces lithography limits, short channel effects and thermal constraints, among others [3]. Here there is a strong need for new transistor architectures and for novel designs for interconnections since, it is argued, optical interconnects are unlikely to offer a viable solution in the short term. Physical limits are not yet reached. A key challenge is the economic one which is leading to an increasing outsourcing, with the associated negative impact in jobs in Europe and raising questions on the need for R&D, and perhaps training, in technology in Europe. It is here where the interaction technology-design is most urgently needed.

C. *Compound semiconductor-based Micro and Nanoelectronics*

The trends in III-V semiconductor compounds were identified as [4]: (i) Scaling of dimensions to 10's of nm, along with development of new materials for contacts, dielectrics, etc. along with new processes for III-V HBTs and HFETs. There are a variety of III-V heterostructure material choices and variations in device physics employed. (ii) Compound SC integration in silicon technologies. Two examples: Incorporation of III-V materials synergistically with Si for higher speed n-channel and p-channel MOSFETs, i.e. getting the III-V on the Si and, InGaAs MOSFET with 3.5 nm channel on a semi-insulating substrate wafer bonded to Si. (iii) Interest on III-V nanotechnologies (nanowires) such as vertical wrap-gated nanowire transistors. However, the question of single transistor fabrication from each nanowire and interconnection of nanodevices into ICs is still open. The main advantage of integrating III-V semiconductors with Si technology is band gap engineering.

D. *Spintronics and Magneto Electronics*

Fundamental phenomena associated with Giant Magnetoresistance, Tunnel Magnetoresistance) and devices for MRAM (Magneto-resistive Random Access Memory) are

understood and are based on the dependence of transmission spin currents depending on the orientation relation of adjacent ferromagnetic layers. In contrast to systems that are based on charge transport, spin dynamics opens the possibility for non-volatile low dissipation memory devices, since charges do not need to be in motion for information transport. Magnetoresistive devices for magnetic sensing and for data storage have already been commercialized. Currently, pure spin currents without charge transfer in integrated circuits are controlled by magnetic fields or spin-polarized charge currents. In the future they might be controlled by electric fields. Intriguing new physical discoveries from which practical possibilities could emerge are for instance RF-applications, spin logics, the spin-Hall effect, the spin-Seebeck effect and quantum computing. The recent advent of topological insulators, which carry non-dissipative spin currents, could lead to a paradigm change [5]. At present, real possible applications utilizing these new discoveries are sometime still unclear. Mayor challenges include: reliability and stability issues, electrical contacts (interfaces) and interconnects. The latter could be minimized by multifunctional devices and, although some basic concepts are already developed, support for device structure design and for developing disruptive new architectures is needed.

E. Molecular Electronics

Molecular electronic devices can be divided in three categories based on size of the device: i) single molecule electronics, ii) self-assembled molecular electronics and iii) thin-film molecular electronics. The single molecule devices represent a very long term approach and much work is needed to gain insight into the behaviour of the molecules, not to mention optimising the properties for data handling and integration [6]. Some of the thin-film molecular electronic devices are already in commercial production, including OFETs, OLEDs and displays. For the next generation Beyond CMOS devices self-assembled molecular electronics is a potential candidate. Reasonable gain and low power consumption have been demonstrated with devices in which self-assembling monolayers replace gate dielectrics, making integration possible [7, 8]. Also, the recent progress in neuron inspired devices is promising [9]. Fabrication can be solution based and on flexible substrates. Drawbacks are slow speed and, when using the molecules as active part of the device, the still poor understanding of the behaviour of the molecules.

F. Solid state quantum computing

The potential of quantum computing has been recognised for a long time but the real implementation is still missing due to issues related to de-coherence limited computing time and difficulties in integration [10-12]. Quantum computing relies on the coupling of switching quantum bits, or qubits, and one of the advantages of quantum computing is that it consumes no energy at the qubit level. Currently, Josephson junction qubits seem to provide the most promising way to integration and realisation of computers with high number of qubits [13]. This technology is also compatible with Si CMOS processing. Although it is still long way in the future, with 100 integrated qubits a quantum computer would surpass in the efficiency any foreseen classical supercomputer with much smaller power consumption. The drawback is that a quantum computer can solve a limited number of problems and only a few algorithms are available. Also, with increasing number of qubits error correction may consume a major part of the computational resources.

G. MEMS

In MEMS/NEMS almost all the domains of physics are present. They are new technologies that can have a strong impact on normal life and nowadays they have yet to bet completely accepted by the users [14]. MEMS/NEMS are rather complex while simultaneously they must be reliable and low power. In fact they must incorporate autonomous management of power.

The current technology trends are: the merging of top down and bottom up approaches, MEMS/NEMS with functional multi-layers suitable for heterogeneous integration, and increasing system approach, increasing number of applications in harsh environments requiring SiC-, Diamond- and Graphene- based MEMS/NEMS, biocompatibility and flexibility.

Among the most important challenges for MEMS technologies, the following can be included: (i) Miniaturization related to size matters requiring that the design tools and simulation programs must be upgraded to the new solutions. (ii) For integration the most important point is to manage complexity. Monolithic vs. heterogeneous solutions must be considered as performances vs. both, costs and volume. Integration is a key point, because the “user” wants a system. (iii) MEMS/NEMS must be autonomous, with a long life.

H. Nanowires

The interest in nanowires comes from attempts to overcome the scaling limitations of the MOSFETS [15], going from planar FETS to FinFETs and on to nanowire FETs. It is argued that nanowire FETS offer improved scaling and better inverse sub-threshold slope. Vertical Si nanowires offer potentially better electrostatics and more efficient dopant segregation, lower voltage and lower power consumption. However, the ON current may be smaller than a MOSFET. There is a density penalty element in architectures and integration which needs to be addressed as well as strong efforts in materials optimisation and the integrating III-V semiconductor heterostructure nanowires. So far, the gate-all-around Si nanowire is being heralded as the ultimate scaled-down FET. The All-Si nanowire tunnel FET seems to be limited by the band gap, while III-V heterostructure nanowires tunnel FET, if integratable with Si may offer a better option. The main challenges are in making contacts, addressing the nanowire devices and the nanowire diameter variability.

I. Memristors

Memristors are considered as digital memories as well as analogue memories [16]. As a 2-state resistance applications of memristors have been suggested as non-volatile memories, as a “transistorless” logic device and as elements for reconfigurable architectures in the form of field programmable gate arrays. An attractive application of memristors as artificial synapses holds

the promise of a cognitive chip (CMOS "neuron") if a hybrid circuit is realised and proven to work consisting of a memristor crossbar on a CMOS. Dedicated architectures and programming schemes are still in their infancy.

V. Design Issues beyond CMOS

Due to the design-technology gap, today we face two communities hardly being able to understand each others main issues. While the "Beyond CMOS inventor" is curious how his findings of new devices with promising opportunities work in a design, the CMOS designer is overstrained by their uncertainties and packed with enough CMOS design problems. Nevertheless, an interaction between both communities is strongly needed.

Such an interaction should lead to a path between great new devices which show magnificent opportunities and the possibility to be composed to a useful system. This path includes the ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology. [17]

The gap to be bridged here is one from physical effects to engineering practices [18]. There is consensus that while emerging devices have very attractive properties the design needed to enable their use in large scale and in mass production, to compete with classic circuit design, is a "completely different story". For example, there exists ability to simulate molecular structures and charging effects for a small number of atoms but it is far away from simulating realistic systems. At present:

(i) A variety of nanodevices can be reliably fabricated from various materials.

(ii) Novel circuits and architectures are going to be needed for a full exploitation of nanodevices.

(iii) Several open questions still exist concerning the mode of operation of such devices.

(iv) Modelling and simulation can provide important answers for better understanding of these devices.

(v) A multi-scale approach is needed in order to describe realistic systems.

(vi) Education is far away from teaching a new generation of designers who know about devices and technology.

(vii) A normal design process of a high performance microprocessor incorporates hundreds of tools and too many experts to work on it.

Looking at the current CMOS design process, we notice, that design on different abstraction levels is crucial for emerging technologies: While design runs at different abstraction levels, certain constraints and conditions are assumed, set and neglected respectively. Due to scaling or other technological progress in CMOS, the neglected constraints could become essential some years later, but then they hardly can be considered. A good example for this was the issue of reliability: It took about five years to incorporate reliability issues into the CMOS design process. Hence, the necessary abstraction on different levels of design leads to immobility with respect to efficiency in scaling and to emerging technologies. There solution has to be found.

Of course the objective of design now and in the future is efficiency: Non-specialists, with sufficient training, should be able to design reliable and robust systems first time right without knowing details of technology. Especially in analogue design for example, we are far off such a situation. Additionally, design approaches should also balance efficiencies and effectiveness and be open to new science breakthroughs. Therefore a simple and open infrastructure for design is needed [19].

Concurrently, a 'Beyond CMOS' device has to meet several challenges with respect to the function of a system that is build from it. Such can be computation, storage interconnect and I/O including analogue. [17] For every 'Beyond CMOS' contender several things have to be valid:

(i) It must add value to one or more of the 4 system functions mentioned above and should be compatible with the others.

(ii) All-in throughput/Watt and/or transactions/Joule must beat CMOS at time of manufacturing at equivalent or lower cost.

(iii) System level manufacturability, reliability, testability must beat ultimate CMOS solutions.

(iv) Room temperature operation is mandatory.

(v) Device variability must be mitigated and modelled and cost efficient error resilient design solutions must be available.

(vi) Design methods and tools must be in place supporting design from device to system. Design tool development time is 3x technology development time.

All this indicates, that in design and in technology, there is a lot to be done hand in hand in order to solve the problems arising 'Beyond CMOS'.

VI. Examples of Benchmarking

Benchmarking in nanoelectronics typically uses criteria from the current CMOS technology point of view [21]. While this approach applies well to devices that behave like "traditional" switches which are the building blocks for Boolean circuits , designed according to a "traditional" architecture, some of the emerging device concepts do not fit into this category and the criteria set should be applied in a relatively loose and flexible manner. In NANO-TEC the term "Beyond CMOS" is understood in a slightly more general sense than in the ITRS roadmap, i.e., instead of direct comparison as in "proper" benchmarking, the NANO-TEC exercise is to identify among the emerging device concepts those that have interesting, and useful, properties and, at least some potential in the long term. Therefore, it is very difficult to define metrics that can be applied to all emerging technologies. Thus, for the recent, and not yet completed, benchmarking exercise, a set of criteria has been defined which can be adapted but must include gain, signal/noise ratio, non-linearity, speed, power consumption, architecture and integratability,

efficiency, tolerances and manufacturability as well as the timeline of each potential technology. In fact, the question to be answered is which of the 'beyond CMOS' devices can complement or outperform CMOS devices in the long term.

Two preliminary examples of the on-going NANO-TEC benchmarking exercise are given below.

A. Example 1: Molecular Electronics

The gain is found to be acceptable for self-assembled molecular FET, still undergoing optimised. In a 2-terminal junction the current is still low. The signal-to-noise ratio is unclear as noise properties have hardly been studied. Most molecular junctions behave non-linear but are not yet quantified. The molecular FET is in general slow but consumes relatively low power with a switching energy of approximately 50zJ/mol. With respect to architectures and integrability, 2- and 3-dimensional arrays of molecules or nanoparticles could implement certain functions, e.g. reconfigurable logic and neuron-inspired functions. Among some of the main advantages of molecular electronics is the almost infinite combination of molecules, adjustable by chemistry leading to specific designs targeting one molecule for one function. With respect to manufacturability, molecular electronics can use solution processing, which is compatible with flexible substrates. The weak defect control and ensuing variability may not be a problem if operations are based on artificial network concepts. Finally, the time to exploitation is expected to be over the 5 to 10 years time scale.

B. Example 2: Graphene electronics

Gain in graphene devices is low due to the ambipolarity and will benefit from the presence of a gap. So far, the best way to open such gap remains unclear. Candidate approaches include chemical modifications, use of graphene nanoribbons, bilayer graphene or develop technology based on zero-gap graphene. Speed is up to THz. The power consumption is problematic when in OFF state while it is good in the ON state (I_{on}/I_{off} = 2 …, 10. Analogue RF properties are "quite" good. Concerning architectures, planar integration has been demonstrated and appears relatively easy. Issues involve mobility dependence on substrate and gate oxide. Graphene offers several advantages, for example, as a replacement of ITO in solar cells, as laser material, printable electronics and as a BISMFET material. Manufacturability issues have been identified concerning deposition, the choice of gate oxide, layer transfer and the fabrication of suspended gates. It is in general compatible with CMOS.

The timeline to production show that graphene ink for printed electronics is expected to be commercially available in 2012, while printed electronic transistors should appear in 2013 and optoelectronic devices in 2013-14. Electronic devices are expected in 2020 (analogue) and 2025 (digital).

VII. CONCLUSIONS AND RECOMMENDATIONS

Currently, it can hardly be predicted how a future basic switching device will look like. For quite some more years to come the deployed dominating technology will still be CMOS but scaling will bring stringent problems with a direct negative impact on power and dependability. When CMOS will have finally reached its scaling limits, new nanoelectronic switching devices will be deployed. In a transition time in between, integrated circuits may be composed in a hybrid manner, i.e., some circuit components may be CMOS-based, others may be emerging nanoelectronics-based. This may refer to the fact that, for example, storage components and logic components have different constraints in terms of delay, footprint, etc. As such, hybrid technologies may have benefits during a transitional time window.

New design techniques and architectures have to be developed to bridge the gap between reliable and power effective applications and the future hybrid and beyond CMOS technologies. These future design techniques must deal with yield and process variation as well as aging effects, thermal effects and soft errors in order to guarantee dependability and power efficiency which are the most critical challenges with respect to new technologies. Manufacturing of nanoelectronic and Beyond CMOS basic switching devices becomes more difficult with shrinking feature size in upcoming technology nodes. Obviously, this trend requires a rethinking of yield, i.e. the faulty components may need to be masked. This lowers the number of available, correctly functioning components but that does not pose a problem with respect to integration ratios of 100 billion (10^{11}) basic switching components that are predicted to be integrated on a single die. Masking may be applied at various abstraction levels of hardware starting from gate level all the way up to a whole processor core and system-on-a-chip. Since within a decade from today hundreds of processors cores can be integrated on a die, masking a whole processor core may still be an economical solution.

Multi-core parallelism is also a well known solution to optimize power consumption at system level. Complete cores or parts of them might be switched off in order to not only save active but also leakage power. Furthermore, multi-supply voltages and different frequencies adapt the power consumption to the required workload. By clock gating, pre-computation or operand isolation power is only needed when new data needs to be computed. New architectural concepts will also be necessary to improve dependability. Let us assume a long processor pipeline, as an example. The probability that a bit flip (e.g. caused by a transient error) occurs somewhere within the pipeline may increase with the size of the pipeline. Upon detection, the pipeline might need to be flushed resulting in performance loss. Parallelism, i.e., more but short pipelines might be a better choice in that case. Parallelism in general might be an advantageous concept with respect to dependability as well as power efficiency.

The technology and design challenges facing the emerging Beyond CMOS approaches may be tackled is specific joint design-technology research programs, for example:

(i) Graphene: Establish a non-zero gap graphene-nanoelectronic program with specify quantitative targets for graphene-based technologies to assess the possibility and test the suitability of fabrication and integration constraints for a combined Si-graphene new ICT technology, beyond sensors and single components.

(ii) Spintronics: Establish a joint program for device structure design and for developing disruptive new architectures.

(iii) MEMS/NEMS: Establish a technology and design program to exploit the third dimension all the way up to system integration for a subset of representative and high-impact applications.

Likewise similar programs for other merging Beyond CMOS concepts could be established. The sooner the complexity is assessed and the magnitude of the challenges estimated, the earlier the opportunity will be there to focus on a subset of most promising new technologies for both Beyond CMOS and More than Moore in Europe. The ambition of the 3rd NANO-TEC workshop is to perform a SWOT analysis based on the trends and benchmarking exercises. This will make it possible to generate specific recommendations.

In summary, new architectural concepts and design methods are needed to master the new challenges of Beyond CMOS technologies, which might result in a new computation paradigm of probabilistic computing algorithms giving results and probabilities for correct functional and timing results under efficient operating conditions.

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