DATE 15

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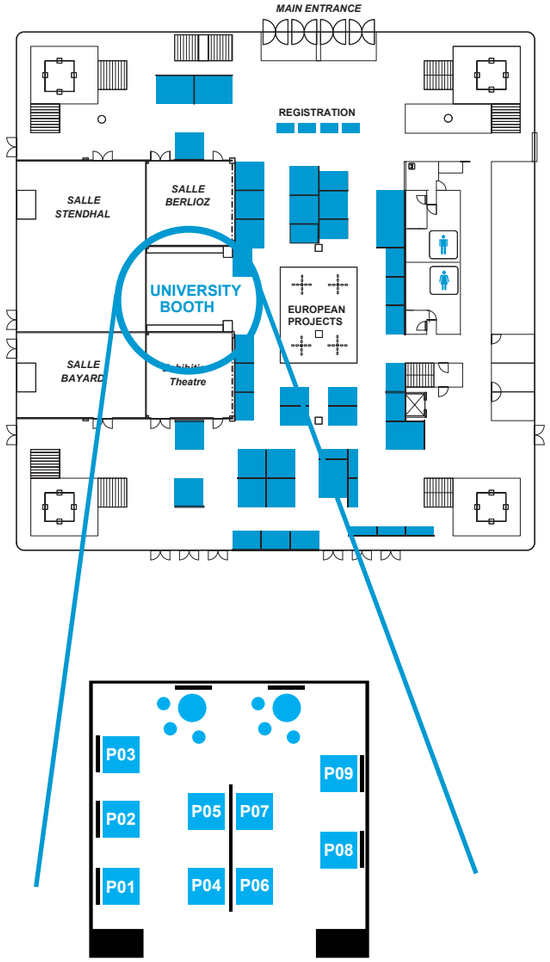
CNRS - Grenoble INP - UJF

CIME nanotech pôle CNFM de Grenoble



Thursday March 12, 2015

EDA Prototypes

10:00 12:00 UB09 | 12:00 14:30 UB10 | 14:30 16:30 UB11

P: Presenter | A: Author

The Ψ-chart Design Approach in TTool/DIPLODOCUS: a Framework for Hw/Sw Co-Design of Data-Dominated Systems-on-Chip
P: Andrea Enrici | A: Ludovic Apvrille, Daniel Camara and Renaud Pacalet, Télécom ParisTech, FR — P07

ISP RAS Verification Tools: Integrated Approach to Hardware Verification at Unit and System Levels Based on Static and Dynamic Methods
P: Andrei Tatarnikov | A: Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak and Sergey Smolov, Institute for System Programming of the Russian Academy of Sciences (ISP RAS), RU — P04

Workcraft: Framework for interpreted graphs
P: Danil Sokolov, Newcastle University, GB — P08

Designing and evaluating resource management policies for heterogeneous system architectures
P: Gianluca Durelli | A: Cristiana Bolchini, Antonio Miele, Gabriele Pallotta, Marcello Pogliani and Marco Santambrogio, Politecnico di Milano, IT — P04

Where is it? Find the code you are interested in!
P: Jan Malburg, University of Bremen, DE
A: Görschwin Fey, U of Bremen / German Aerospace Center, DE — P06

Interactive Visualization of ESL Designs
P: Jannis Stoppe, University of Bremen, DE
A: Robert Wille and Rolf Drechsler, U of Bremen/DFKI GmbH, DE — P08

Real-time Multiprocessor compiler demo: Compiler for Real-Time Multiprocessor Systems with Shared Accelerators
P: Marco Bekooij | A: Guus Kuiper, Stefan Geuns, Philip Wilmanns, Joost Hausmans and Marco Bekooij, U of Twente, NL — P06

3D-COSTAR: Using 3D-COSTAR for 2.5D-/3D-SIC Cost Analysis
P: Mottaqiallah Taouil[1] | A: Mottaqiallah Taouil[1], Said Hamdioui[1] and Erik Jan Marinissen[2]
[1]TU Delft, NL; [2]IMEC, BE — P07 P08

VDA-ADMF: An Agile Migration Framework for Analog Layout Design
P: Po-Cheng Pan[1] | A: Ching-Yu Chin[1], Hung-Ming Chen[1], Tung-Chieh Chen[2], Jou-Chun Lin[2] and Yi-Peng Weng[3]
[1]National Chiao Tung University, TW; [2]Synopsys Co., Ltd., TW; [3]Taiwan Semiconductor Manufacturing Company, TW — P01

FLaRE: A Reconfiguration Aware Floorplanner
P: Riccardo Cattaneo | A: Marco Rabozzi and Marco Santambrogio, Politecnico di Milano, IT — P03

Functional ECO: An efficient rewiring enhanced functional ECO
P: Tak Kei Lam[2] | A: Xing Wei1, Yi Diao[1], Tak Kei Lam[2] and Yu-Liang Wu[1]
[1]Easy-Logic Technology Limited, HK; [2]The Chinese U of Hong Kong, HK — P06

The Bond Calculator
P: Carl Christoph Jung[2]
A: Christian Silber[1] and Juergen Scheible[2]
[1]Robert Bosch GmbH, DE; [2]Reutlingen U, DE — P09

Hardware Design & Test Prototypes

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Linux on TSAR: Porting the Linux kernel to the TSAR manycore architecture
P: César Fuguet Tortolero | A: Joël Porquet and Alain Greiner, UPMC-LIP6, FR — P03 P03

NetFPGA SUME: Making 100GBps a Commodity
P: Noa Zilberman | A:Yury Audzevich, Georgina Kalogeridou and Andrew W. Moore, U of Cambridge, GB — P02 P02

An FPGA lab-on-chip: An Analysis Tool and Framework for Advanced Measurements and Reliability Assessments on Modern Nanoscale FPGAs
P: Petr Pfeifer, Technical U of Liberec, CZ — P02

Reconfigurable FPGA-based non-intrusive BERT for production test
P: Sergei Odintsov | A: Artjom Jasnetski, Tallinn U of Technology, EE — P04

Combination of WSN and 1st Order Kinetic Model for Real-Time Shelf-Life Prediction of Perishable Goods
P: Valerio Francesco Annese | A: Daniela De Venuto, Politecnico di Bari, IT — P01 P01

CryptoChip: Demonstration of Cryptographic ASIC Prototype
P: Xuan Thuy Ngo | A:Xuan Thuy Ngo, Jean-Luc Danger, Sylvain Guilley, Tarik Graba, Yves Mathieu and Zakaria Najm, Télécom ParisTech, FR — P09 P07

Designing Electronics for Medical Applications

10:00 12:00 UB09 | 12:00 14:30 UB10 | 14:30 16:30 UB11

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MAMMA: Speech Enhancement Demo exploiting MEMS Microphone Array for people with disabilities
P: Luca Fanucci[1] | A: Alessandro Palla[1], Luca Fanucci[1] and Roberto Sannino[2]
[1]U of Pisa, IT; [2]STMicroelectronics, IT — P09

Real-Time Pattern Detection of Movement Related Potentials by Synchronized EEG and EMG
P: Valerio Francesco Annese | A: Daniela De Venuto, Politecnico di Bari, IT — P05 P05 P05

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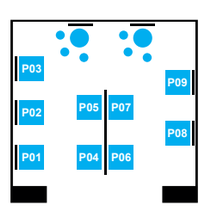

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University Booth at DATE 2015

DATE, the Design, Automation and Test Conference and Exhibition is the unique European event bringing together researchers, user and vendors as well as specialists in the design, test and manufacturing of electronic circuits and systems.

The University Booth is organized during DATE and will be located in the exhibition area. All demonstrations will take place from Tuesday, March 10 to Thursday, March 12, 2015 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrations.

The University Booth program is composed by 39 demonstrations from 14 different countries, presenting software and hardware solutions. The program is organized in 11 sessions of 2 or 2.5 h duration and will cover four major topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Designing Electronics for the Internet of Things
- Designing Electronics for Medical Applications

DATE university booth welcomes you to booth 4 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to booth 4 and find out about the latest innovations.

We are sure that the demonstrations will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this program.

More information can be found on the DATE web site, http://www.date-conference.com/group/exhibition/u-booth.

See you at the University Booth (Booth 4)!

Laurent Fesquet and Andreas Vörg (U Booth Chairs)

Tuesday March 10, 2015

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EDA Prototypes

10:30 12:30 15:00 17:30
12:30 15:00 17:30 19:30
UB01 UB02 UB03 UB04

P: Presenter | A: Author

Implementations of the Semi-Global Matching 3D vision algorithm for automotive applications
P: *Affaq Qamar*
A: *Luciano Lavagno, Politecnico di Torino, IT*

ODEN: Assertion mining for behavioral descriptions
P: *Alessandro Danese |* ***A:*** *Alessandro Danese, Tara Ghasempouri and Graziano Pravadelli, U of Verona, IT*

The Ψ-chart Design Approach in TTool/DIPLODOCUS: a Framework for Hw/Sw Co-Design of Data-Dominated Systems-on-Chip
P: *Andrea Enrici |* ***A:*** *Ludovic Apvrille, Daniel Camara and Renaud Pacalet, Télécom ParisTech, FR*

ISP RAS Verification Tools: Integrated Approach to Hardware Verification at Unit and System Levels Based on Static and Dynamic Methods
P: *Andrei Tatarnikov[1] |* ***A:*** *Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak and Sergey Smolov[1]*
[1]Institute for System Programming of the Russian Academy of Sciences (ISP RAS), RU

HiPER-NIRGAM: A Tool Chain Based Framework for Modelling Thermal - Aware Reliability Estimation in 2D Mesh NoCs
P: *Ashish Sharma[1] |* ***A:*** *Manoj Singh Gaur[1], Lava Bhargava[1], Vijay Laxmi[1] and Mark Zwolinski[2]*
[1]Malaviya National Institute of Technology, Jaipur, IN; [2]U of Southampton, GB

The Bond Calculator
P: *Carl Christoph Jung[2]*
A: *Christian Silber[1] and Juergen Scheible[2]*
[1]Robert Bosch GmbH, DE; [2]Reutlingen U, DE

Workcraft: Framework for interpreted graphs
P: *Danil Sokolov, Newcastle U, GB*

Numerical Methods for Efficient Simulations of Circuits with Separated Time Scales
P: *Genie Hsieh, Sandia National Laboratories, US*

Designing and evaluating resource management policies for heterogeneous system architectures
P: *Gianluca Durelli |* ***A:*** *Cristiana Bolchini, Antonio Miele, Gabriele Pallotta, Marcello Pogliani and Marco Santambrogio, Politecnico di Milano, IT*

OSTC: Combining HIFSuite and SCNSL for smart device integration and simulation
P: *Graziano Pravadelli |* ***A:*** *Alessandro Danese, Franco Fummi, Valerio Guarnieri, Michele Lora, Graziano Pravadelli and Francesco Stefanni, U of Verona, IT*

Where is it? Find the code you are interested in!
P: *Jan Malburg, U of Bremen, DE |* ***A:*** *Görschwin Fey, U of Bremen / German Aerospace Center, DE*

XtSi: The 3-D electro-thermal simulator
P: *Jürgen Scheible |* ***A:*** *Carl C. Jung, Reutlingen U, DE*

ISIS: Customizable Runtime Verification of Hardware/Software Virtual Platforms
P: *Laurence Pierre |* ***A:*** *Martial Chabot, TIMA, FR*

Real-time Multiprocessor compiler demo: Compiler for Real-Time Multiprocessor Systems with Shared Accelerators
P: *Marco Bekooij, U of Twente, NL |* ***A:*** *Guus Kuiper, Stefan Geuns, Philip Wilmanns, Joost Hausmans and Marco Bekooij, U of Twente, NL*

AIDASoft: Analog IC Design Automation
P: *Nuno Horta[1] |* ***A:*** *Nuno Lourenço[1], Ricardo Martins[1], Ricardo Póvoa[1], António Canelas[1], Ricardo Lourenço[2] and Pedro Ventura2*
[1]Instituto de Telecomunicações/Instituto Superior Técnico, PT; [2]Instituto de Telecomunicações, PT

ID.Fix: An EDA Tool for Fixed-Point Refinement of Embedded Systems
P: *Olivier Sentieys[2] |* ***A:*** *Daniel Menard[1] and Nicolas Simon[2]*
[1]INSA Rennes, FR; [2]INRIA, FR

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EDA Prototypes

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FLaRE: A Reconfiguration Aware Floorplanner
P: *Riccardo Cattaneo |* ***A:*** *Marco Rabozzi and Marco Santambrogio, Politecnico di Milano, IT*

Gesture Recognition based Robotic Embedded System
P: *Seetal Potluri[1] |* ***A:*** *Ravindran Balaraman[1], Pradyot K. V. N.[1], Manimaran S. S.[1], Praharasan Raja[1], Anshul Bansal[2] and Abhishek Mehta[2]*
[1]IIT Madras, IN; [2]Punjab Engineering College, IN

VHDL to SystemC Translation and Abstraction: SystemC Manipulation Framework: from RTL VHDL to Optimized TLM SystemC
P: *Syed Saif Abrar |* ***A:*** *Syed Saif Abrar, Valentin Tihomirov, Maksim Jenihhin and Jaan Raik, Tallinn U of Technology, EE*

P08 P08 P03 P06

Hardware Design & Test Prototypes

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UB01 UB02 UB03 UB04

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STRNG: A Self-timed Ring based True Random Number Generator with Monitoring and Entropy Assessment
P: *Abdelkarim Cherkaoui[1] |* ***A:*** *Laurent Fesquet[1], Viktor Fischer[2] and Alain Aubert[2]*
[1]TIMA, FR; [2]LaHC, FR

4-LOOP: 4-core Leon 3 with linux Operating system, OpenMP library and hardware Profiling system
P: *Giacomo Valente |* ***A:*** *Vittoriano Muttillo a. Fabio Federici, U of L'Aquila, IT*

Reconfigurable FPGA-based non-intrusive BERT for production test
P: *Sergei Odintsov |* ***A:*** *Artjom Jasnetski, Tallinn U of Technology, EE*

P01 P01 P01 P01 P07

Designing Electronics for Medical Applications

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MAMMA: Speech Enhancement Demo exploiting MEMS Microphone Array for people with disabilities
P: *Luca Fanucci[1] |* ***A:*** *Alessandro Palla[1], Luca Fanucci[1] and Roberto Sannino[2]*
[1]U of Pisa, IT; [2]STMicroelectronics, IT

PARLOMA: A Remote Communication System for Deafblind People
P: *Ludovico Orlando Russo[1] |* ***A:*** *Giuseppe Airò Farulla[1], Marco Indaco[1], Calogero Maria Oddo[2], Daniele Pianu[3], Paolo Prinetto[1], Stefano Rosa[1] and Ludovico Orlando Russo[1]*
[1]Politecnico di Torino, IT; [2]Scuola Superiore Sant'Anna, The Biorobotics Institute, IT; [3]CNR, IEIIT, IT

P06 P02 P02

Designing Electronics for the Internet of Things

10:30 12:30 15:00 17:30
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UB01 UB02 UB03 UB04

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Orientoma: A wearable orientation system for blind and visually impaired people
P: *Giuseppe AiroFarulla |* ***A:*** *Marco Indaco and Ludovico Russo, Politecnico di Torino, IT*

Smart Cell Development Platform for Embedded Battery Management
P: *Swaminathan Narayanaswamy, TUM CREATE, SG*
A: *Matthias Kauer[1], Sebastian Steinhorst[1], Martin Lukasiewycz[1] and Samarjit Chakraborty[2]*
[1]TUM CREATE, SG; [2]TU Munich, DE

P02 P04

Wednesday, March 11, 2015

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EDA Prototypes

10:00 12:00 14:00 16:00
12:00 14:00 16:00 18:00
UB05 UB06 UB07 UB08

P: Presenter | A: Author

System-level FPGA prototyping of analog/mixed-signal systems
P: *Georg Gläser[1] |* ***A:*** *Eckhard Hennig[1], Vojtech Dvorak[2]*
[1]Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE; [2]Brno U of Technology, CZ

ODEN: Assertion mining for behavioral descriptions
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XtSi: The 3-D electro-thermal simulator
P: *Jürgen Scheible, Reutlingen U, DE*
A: *Carl Christoph Jung, Reutlingen U, DE*

RSoC Framework: Framework for rapid prototyping of applications on reconfigurable SoCs
P: *Korcek Pavol |* ***A:*** *Jan Viktorin, Vlastimil Kosar and Jan Korenek, Brno U of Technology, CZ*

ISIS: Customizable Runtime Verification of Hardware/Software Virtual Platforms
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A Framework for the Emulation and Prototyping of Nano-Photonic Optical Accelerators
P: *Alberto Garcia-Ortiz[2] |* ***A:*** *Wolfgang Büter[1], A. Ali[2], S Mahmood[2], S. Arefin[2], V. V. Parsi Sreenivas[2], M. Mike Bülters[3] and R.-B. Bergmann[3]*
[1]Institute for Electrodynamics and Microelectronics Systems (ITEM), DE; [2]U of Bremen, Physics/Electrical Engineering, DE; [3]Bremer Institut für angewandte Strahltechnik GmbH, DE

An FPGA lab-on-chip: An Analysis Tool and Framework for Advanced Measurements and Reliability Assessments on Modern Nanoscale FPGAs
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