ADVANCE PROGRAMME

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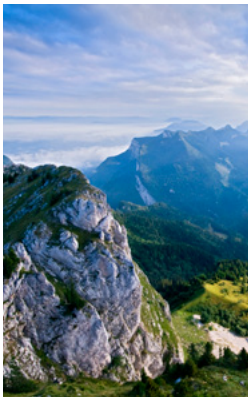

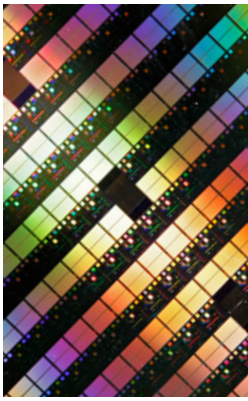

DATE 15

Design, Automation and Test in Europe

March 9—13, 2015, Grenoble, France

DATE 2015 SPONSORS

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European Electronic Chips & Systems design Initiative

ACM Special Interest Group on Design Automation

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MEDIA PARTNERS

The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in the editorial pages. Listed below are the media houses and publications who generously agree to media partnership with DATE, and whose publications can be found on-site.

3D InCites

3D InCites is the only online community resource devoted exclusively to the development of interposer and 3D integration technologies including 3D TSVs, 3D ICs and 3D system architectures. Through original contributed content from industry experts, 3D InCites brings to life, the people, the personalities, the ideas, and the minds behind 3D integration.

http://www.3DinCites.com

Chip Design Magazine

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won't want to miss. And, be sure to visit www.eecatalog.com for valuable information about all of Extension Media's outstanding technology resources.

http://chipdesignmag.com

EDA Confidential

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes "Recipes", Freddy Santamaria's "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

http://www.aycinena.com

EDACafé

Thousands of IC, FPGA and System designers visit EDACafé.com to learn the latest news and research design tools and services. The sites attract more than 75,000 unique visitors each month and leverages TechJobsCafé.com to bring you job opportunities targeted to engineering and design. And daily e-newsletters reach more than 30,000 engineering professionals. EDACafe.com will be doing Executive Video interviews of exhibitors and show organizers at its stand in the Rhodes Hall. For more details visit www.EDACafe.com and www.TechJobsCafe.com.

http://www.edacafe.com

EE Times Europe

EE Times Europe provides marketing professionals in the electronics industry with integrated online and print marketing services. EE Times Europe's print edition is a monthly magazine that brings news, analysis and product and design information to 70,000 highly qualified subscribers in over 40 European countries. EE Times Europe's web site eetimes.eu welcomes over 110,000 monthly unique visitors. EE Times Europe's electronic newsletters reach over 30,000 daily readers.

http://www.electronics-eetimes.com

MEDIA PARTNERS

DATE15
March 9 – 13, 2015, Grenoble, France

ElectroniqueS

ElectroniqueS the reference monthly for decision makers and engineers in the electronics sector Circulation of 10,000 copies www.electroniques.biz, the electronic professional's web site Daily Newsletter, the day's essential news about our industry's major sectors Sent to more than 26,000 free subscribers Weekly newsletter, the newsletter that summarizes the previous 5 daily newsletters main topic Sent to more than 23,000 free subscribers Vertical newsletter, 3 subjects: Automotive / Mil-Aero / Medical 5 mailings a year (each 2 in 3 months)

http://www.electroniques.biz

Elektronik i Norden

Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed copies proves we are the major electronics paper in this area. We publish news, comments and in-depth technical articles.

http://www.elinor.se

Engineering & Technology Magazine – Published by The IET

Engineering & Technology is packed with articles on the latest technology covering the areas of communications, control, consumer technology, electronics, IT, manufacturing & power engineering. It is Europe's largest circulation engineering magazine, published monthly & offers a global circulation of over 140,000 copies to more than 100 countries & a high pass-on readership. Each member of the Institution of Engineering & Technology (IET) receives a copy as part of their membership package. Readers include design & development engineers, system designers & integrators, solutions providers & installers, engineering distributors, consultants, planners, facilities managers & end-users.
With its HQ in London & regional offices in Europe, North America & Asia-Pacific, the Institution of Engineering & Technology provides a global knowledge network to facilitate the exchange of ideas & promote the positive role of technology around the World. The Institution of Electrical Engineers, dating from 1889, became the Institution of Engineering & Technology in 2006. It now organises more than 120 conferences & other events each year whilst providing professional advice & briefings to industry, education & governments.

http://eandt.theiet.org

JB Systems Media

JB Systems Media is a high tech engineering and media company. JB Systems main areas of interest are among others IoT Embedded Systems, IP Systems, On-Line Education, Systems Engineering & Science.

http://www.jbsystech.com

L'Embarqué

L'Embarqué is a 100% digital media focused on the embedded software and embedded systems market. The media combines a French language web site, several newsletters and a French digital magazine in rich PDF format. The web site www.lembarque.com features a daily updated news feed, various « guest » blogs run by embedded experts and/or VIPs, online job postings and regularly refreshed information on new products. With more than 50 pages displayed in rich PDF format and readable on PCs and tablets, the quarterly digital magazine features interviews, analysis articles written by L'Embarqué journalists, and in-depth contributed articles on new embedded hardware or software technologies. Various market fields are addressed by L'Embarqué (mil/aero, medical, industrial, automotive, consumer electronics, telecoms/datacoms…) and the media has a very strong focus on topics related to IoT technologies, software, tools, IP, EDA tools, services and markets.

http://www.lembarque.com

WELCOME TO DATE 2015

Dear Colleague,

We proudly present to you the Advance Programme of **DATE 2015.** DATE combines the world's favorite electronic systems design and test conference with an international exhibition for electronic design, automation and test, ranging from advances on system-level hardware and software implementation to integrated circuit design and nano-technology manufacturing technologies.

DATE 2015 received eligible 915 paper submissions – an all-time high for DATE and a 3% increase over DATE 2014. Besides the large share (45%) of submissions coming from Europe, 24% of submissions are from North-America, 28% from Asia, and 3% from the rest of the world. This proves DATE's international character, its global reach and world-wide impact.
For the 18th successive year, DATE has prepared an exciting technical programme. With the help of the 309 members from its Technical Programme Committee who carried out 3675 reviews (more than four per submission), finally 206 papers (22%) were selected for regular presentation and 86 additional ones (9%) for interactive presentation this year.
The DATE 2015 conference will be held at the Alpexpo Congress Center in Grenoble, France, offering once again a truly interesting programme lasting the whole week of March 9 to 13, 2015. On Monday, the conference starts with ten in-depth tutorials. From Tuesday to Thursday, the main technical programme composed of 78 technical sessions comes about. This programme is divided in parallel tracks from four main areas: **D** – Design Methods and Tools, **A** – Application Design, **T** – Test and Robustness; and **E** – Embedded Systems Software. Finally, on Friday, ten parallel workshops will highlight latest research on hot topics in electronic systems design, such as, 3D design automation, neurocomputing and optical interconnect systems.

This year two of the **plenary keynote speakers on Tuesday** are EU Commissioner Günther H. Oettinger to talk about European Microelectronics Strategy and Jean Marc Chery, Chief Operating Officer of STMicroelectronics. On the same day, the **Executive Track** offers a series of business panels discussing hot topics. Executive speakers from companies leading the design and automation industry will address some of the complexity issues in electronics design and discuss about the advanced technology challenges and opportunities.

In addition, the distinctive highlights of DATE 2015 are the two special days: **"Designing Electronics for the Internet of Things (IoT)"** on Wednesday, and **"Designing Electronics for Medical Applications"** on Thursday. A comprehensive overview regarding both themes will be given, ranging from innovations and applications of latest technologies to analysis of upcoming electronic design automation (EDA) research challenges.

On one hand, the IoT, also known as the "Internet of Anything" promises to realize the omnipresent network of tens of billions of communicating devices. These devices will enable new business models and revolutionize industrial production, logistics and social life, but they will also require dedicated hardware, ultra-low power robust devices and new design methodologies. These topics will be covered by the **three keynotes on Wednesday.** First, Wolfgang Wahlster (German Research Center for Artificial Intelligence, DE) will address "Industrie 4.0: From the Internet of Things to Cyber-Physical Production Systems". Then, Antun Domic (Synopsys, US) will analyze "The Rise of IoT, and the Role of EDA". Finally,

WELCOME TO DATE 2015

Wolfgang Nebel

David Atienza

Hannes Schwaderer (Intel, DE) will highlight the market driven challenges of IoT devices.

On the other hand, providing universal and costly-effective healthcare to the complete human kind has become a major challenge in our modern society. Thus, Thursday will feature an outstanding set of four special sessions on the topic of "Game-changing innovation in health care". This day includes ten trend-setting invited papers, eight of which come from key industrial players in the health care field. Furthermore, **one keynote** in the frame of the Special Day on Medical Electronics will be given by Kristoffer Famm from GlaxoSmithKline (GSK) to talk about "Bioelectronic Medicines - Heralding in a New Therapeutic Approach".

In addition, numerous **Interactive Presentations** are organized into five IP sessions during the conference. The accompanying **exhibition** offers a comprehensive overview of commercial design and verification tools including vendor seminars and industrial presentations in the Exhibition Theatre. Moreover, abundant networking possibilities exist with fringe meetings and demonstrations of university research in European projects.

We wish you a successful and exciting DATE 2015 and an entertaining DATE networking event on Wednesday evening, which will take place in the memorable "Musée de Grenoble".

DATE 2015 General Chair
Wolfgang Nebel
OFFIS & University of Oldenburg, DE

DATE 2015 Programme Chair
David Atienza
EPFL, CH

OPENING PLENARY

Tuesday, March 10, 2015,
0830 — 1030 Auditorium Dauphine

Opening Session: Plenary, Awards Ceremony & Keynote Addresses

KEYNOTE ADDRESSES

Geneviève Fioraso

1.1.3 Keynote Address

Geneviève Fioraso,
secrétaire d'Etat chargée de l'Enseignement supérieur et de la Recherche (to be confirmed), FR

Günther H. Oettinger

1.1.4 Keynote Address

Günther H. Oettinger,
European Commissioner for Digital Economy and Society, DE

Jean Marc Chery

1.1.5 ST technologies fully addressing Internet of Things applications from LP Digital to RF-CMOS, eNVM and sensors

Jean Marc Chery,
STMicroelectronics, FR

WEDNESDAY KEYNOTE ADDRESS

Wolfgang Wahlster

1250 — 1320
Salle Oisans

7.0.1 Industrie 4.0: From the Internet of Things to Cyber-Physical Production Systems

Wolfgang Wahlster,
German Research Center for Artificial Intelligence, DE

The Internet of Things is finding its way into production. Semantic machine-to-machine communication revolutionizes factories by decentralized control. Embedded digital product memories guide the flexible work piece flow through smart factories, so that low-volume, high-mix production is realized in a cost-efficient way. A new generation of industrial assistant systems using augmented reality and multimodal interaction will help factory workers to deal with the complexity of cyber-physical production. INDUSTRIE 4.0 is the German strategic initiative to take up a pioneering role in industrial IT that is currently revolutionizing the manufacturing engineering sector. Semantic product memories will play a key role in the upcoming fourth industrial revolution based on cyber-physical production systems. Low-cost and compact digital storage, sensors and radio modules make it possible to embed a digital memory into a product for recording all relevant events throughout the entire lifecycle of the artifact. By capturing and interpreting ambient conditions and user actions, such computationally enhanced products have a data shadow and are able to perceive and control their environment, to analyze their observations and to communicate with other smart objects and human users about their lifelog data. Cyber-physical systems and the Internet of Things lead to a disruptive change in the production architecture: the workpiece navigates through a highly instrumented smart factory and tries to find the production services that it needs in order to meet its individual product specifications stored on the product memory. We illustrate this revolutionary production architecture with examples from DFKI' Smart Factory.

WEDNESDAY KEYNOTE ADDRESS

1320 — 1350
Salle Oisans

7.0.2 The rise of IOT, and the role of EDA

Antun Domic,
Synopsys, US

Antun Domic

On April 19th, 2015, we will celebrate the 50th anniversary of Moore's law. Process technology went from several microns to a few nanometers, transistors integration capabilities increased millions of times, and volume production grew from the few thousands of units in the early digital computer era to the several billions in the smartphone one. IoT is expected to bring volume production up by one, and perhaps even two orders of magnitude in the next decade. Today, IC volume growth has been anchored on smart phones. Smart everything (cars, homes, cities) may be the next killer application, which would fuel the volume growth. IoT devices and systems will certainly span the entire spectrum, from extremely advanced and complex to "disposable". They will make metrics such as reliability and resilience, be as important as performance, power, and area. But in order for IoT to happen, our industry should dramatically improve its efficiency – all "resources" are scarce, and therefore precious. Flexibility – systems are heterogeneous by nature – and productivity – to deliver the best possible quality-of-results within the allotted turn-around-time – will be critical. As both process technology and system complexity increase, advanced EDA will be a key enabler. Advanced design implementation infrastructure, tools, flows, and methodologies will deliver a competitive advantage, and advanced IP sub-systems, consisting of hardware and software solutions will deliver complete, complex functions, ready for integration, greatly simplifying the IoT "siliconization". These two components show the only viable path towards the trillion units many industry leaders are envisioning.

THURSDAY KEYNOTE ADDRESS

1320 — 1350
Salle Oisans

11.0.1 Bioelectronic Medicines – Heralding in a New Therapeutic Approach

Kristoffer Famm,
GlaxoSmithKline, GB

Kristoffer Famm

Imagine a day when electrical impulses are a mainstay of medical treatment, a day when your doctor will routinely administer microscopic devices that modulate signals in specific nerves for treatment effect. Every organ in our bodies is wired and controlled by nerves, so bioelectronic medicines may be applicable across a broad range of diseases just like molecular medicines are today. Through bioelectronic medicines, GSK, a leading pharmaceutical company, and its extensive network of research collaborators aim to bring the precision and intelligence of electronics right to the core of future treatments.

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This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 2015. Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website **www.date-conference.com**

Dates and Venue

The conference will take place from 9 to 13 March, 2015, in the Alpexpo Congress Centre

ALPEXPO-ALPES Congres
Parc Événementiel de Grenoble
Avenue d'Innsbruck – CS 52408
38034 Grenoble cedex 2
France
www.alpexpo.com

The accompanying exhibition is scheduled from 10 to 12 March, 2015 and will take place in the foyer of the Alpexpo congress centre, directly next to the session rooms. The spacious area also hosts the poster presentation area as well as coffee break area.

Interactive Programme Online

A fully interactive DATE 2015 programme is available on the web **www.date-conference.com** where you will be able to view the entire details of the programme and plan your attendance in advance.

Internet Access

There will be free wireless internet access throughout the whole congress center. The WLAN login code will be available on-site at the registration desk (entrance foyer).

WHOVA APP

The DATE organizers are happy to announce that there will be an app available for the first time at the DATE conference. The WHOVA App can be downloaded via the following link or in the Apple/Google stores for free: **https://whova.com/download**

Please install the app and search for the conference "DATE 2015" → Password: "DATE"

Online Conference Evaluation via the App ("survey" button): every fully registered delegate who fills in the online conference evaluation via the WHOVA App, will receive a DATE mug at the registration desk (when showing the confirmation page).

Proceedings

The conference proceedings are available for download on-site through the DATE-WLAN for every fully registered conference delegate at the following link: **www.date-conference.com/proceedings**

GENERAL INFORMATION

Coffee Break in Exhibition Area

On all conference days (Tuesday to Thursday), coffee and tea will be served during the coffee breaks at the below-mentioned times in the exhibition area.

Lunch Break

On Tuesday and Wednesday, lunch boxes will be served in front of the session room Salle Oisans and in the exhibition area for fully registered delegates (a voucher will be given upon registration on-site). On Thursday, lunch will be served in Room Les Ecrins (for fully registered conference delegates only).

Tuesday, March 10, 2015

Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Keynote session sponsored by Mentor Graphics in room Oisans	1320 – 1420
Coffee Break	1600 – 1700

Wednesday, March 11, 2015

Coffee Break	1000 – 1100
Lunch Break	1230 – 1430
Keynote lectures in room Oisans	1250 – 1420
Coffee Break	1600 – 1700

Thursday, March 12, 2015

Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
Keynote lecture in room Oisans	1320 – 1350
Coffee Break	1530 – 1600

Welcome Reception — Mon, March 9, 2015

The organizers kindly invited all registered conference delegates to the DATE 2015 Welcome Reception which will take place on Monday, March 9, 2015, from 1800 – 1900 in the area "Salle de Reception" of the congress center. Subsequently, the PhD Forum will take place from 1900 – 2100 in the same location, where every interested delegate can attend as well.

Exhibition Reception — Tue, March 10, 2015

The Exhibition Reception will take place on Tuesday, March 10, 2015, from 1830 – 1930 in the exhibition area of the congress center, where free drinks for all conference delegates and exhibition visitors will be offered. All exhibitors are welcome to also provide drinks and snacks for the attendees.

DATE 15
March 9 – 13, 2015, Grenoble, France

GENERAL INFORMATION

DATE Networking Event

Wed, March 11, 2015

As one of the main networking opportunities during the DATE week, the DATE Party states a perfect occasion to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities. **It will take place on March 11, 2015, from 1930 to 2300 in the renowned "Musée de Grenoble" (Grenoble Museum).**

This painting museum features a unique collection of ancient, modern and contemporary art including major masterpieces of classical Flemish, Dutch, Italian and Spanish painting and all the great pot-1945 contemporary art-trends, right up to the most recent artwork of the 2000s. During this evening, you can enjoy the famous French Cuisine and outstanding wines. Discover the region of the French Alps through its cheese and wine specialties. The dinner will be accompanied by jazz songs and instrumental music from Annah Cruz and her vocal band. Another highlight will be the show waders "THE INSEPARABLES", sweet and ephemeral characters walking through the premises, releasing dreams and laughter. Furthermore, at the very beginning of the evening, from 2000 to 2130, you will have the opportunity to visit parts of the permanent collection of the museum (ninetieth and twenties century). Please kindly note that it is not a seated dinner. All delegates, exhibitors and their guests are invited to attend the party. Please be aware that entrance is only possible with a valid party ticket. Each full conference registration includes a ticket for the DATE Party (which needs to be booked during the online registration process though). Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets). Price for extra ticket: 60 € per person.

How to get there: Tram B has a stop called "Notre Dame Musée" which is next to the Museum. Attendees would take Tram A from Alpexpo and change for Tram B in one of the stations between "Gares" and "Maison du Tourisme" to get to the museum. The trip takes about 30 minutes.

Interactive Presentations, sponsored by Cadence Academic Network

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide shown on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held in the Poster Area (as part of the exhibition area) in 30-minute time slots on the following days:

IP Session 1	Tuesday, March 10, 2015	Exhibition Area	1600 – 1630
IP Session 2	Wednesday, March 11, 2015	Exhibition Area	1000 – 1030
IP Session 3	Wednesday, March 11, 2015	Exhibition Area	1600 – 1630
IP Session 4 Presentation of Best IP Award	Thursday, March 12, 2015	Exhibition Area Salle Oisans	1000 – 1030 1315
IP Session 5	Thursday, March 12, 2015	Exhibition Area	1530 – 1600

EXECUTIVE SESSIONS — TUESDAY

Organiser: **Yervant Zorian,** Synopsys, US

DATE 2015 will again feature an Executive Track of presentations by leading company executives representing a range of semiconductor manufacturers, EDA vendors, fables houses and IP providers. This one-day programme will be held on Tuesday 10 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks.

All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view.

2.1 **EXECUTIVE SESSION:**

New Opportunities in the Internet of Things

See Page 41

3.1 **EXECUTIVE SESSION:**

Extending Morre's Law & Heterogeneous Integration

See Page 46

4.1 **EXECUTIVE SESSION:**

Trends and Challenges in Today's Automotive Semiconductors

See Page 52

SPECIAL DAY — WEDNESDAY

Organiser and Chair: **Rolf Drechsler,** University of Bremen/DFKI, DE

Designing Electronics for the Internet of Things

The IoT, also known as the "Internet of Anything" promises to realize the omnipresent network of tens of billions of communicating devices. These devices will enable new business models and revolutionize industrial production, logistics and social life, but they will also require dedicated hardware, ultra-low power robust devices and new design methodologies. The sessions and keynotes of the Special Day on Wednesday will cover these topics.

5.1 **SPECIAL DAY Hot Topic: Applications of IoT**
See Page 56

6.1 **SPECIAL DAY Hot Topic: Platforms for the IoT**
See Page 61

7.0 **SPECIAL DAY Keynotes**

7.0.1 **Industrie 4.0: From the Internet of Things to Cyber-Physical Production Systems**

7.0.2 **The rise of IOT, and the role of EDA**

7.0.3 **Market driven challenges of IoT devices**
See Page 65

7.1 **SPECIAL DAY Hot Topic: Design Tools for the IoT**
See Page 65

8.1 **SPECIAL DAY Panel: Security and Verification for the IoT**
See Page 71

SPECIAL DAY — THURSDAY

Organiser and Chair: **Jo De Boeck,** IMEC, BE

Designing Electronics for Medical Applications

Providing universal and costly-effective healthcare to the complete human kind has become a major challenge in our modern society. Thus, Thursday will feature an outstanding set of 4 special sessions on the topic of "Game-changing innovation in health care". This Special Day includes 10 trend-setting invited papers, 8 of which come from key industrial players in the health care field and one keynote during lunch time.

9.1 **SPECIAL DAY Hot Topic: Game-changing Innovative Technology Platforms for Health Care**
See Page 77

10.1 **SPECIAL DAY Hot Topic: Wearable Medical Applications**
See Page 82

11.0 **SPECIAL DAY Keynote Bioelectronic Medicines – Heralding in a New Therapeutic Approach**
See Page 87

11.1 **SPECIAL DAY Hot Topic: Implantable Medical Applications**
See Page 87

12.1 **SPECIAL DAY Hot Topic: Technology and Design Platforms for Diagnostics**
See Page 93

SPECIAL SESSIONS

Special Session Chairs: **Marco Casale-Rossi,** Synopsys, US
Marco Platzner, University of Paderborn, DE

The following ten Special Sessions have been organized, which should prove to be of great general interest. Panel Sessions provide forums in which motivated opinions on unsettled issues are discussed. The 'trend setters' are given a time-slot to present their views, which are then subjected to critical appraisal and rich exchanges from the audience. Hot Topic Sessions give technical information about strongly emerging topics and offer a good overview and technical insight provided by leading experts in the field. Relevant issues and their importance for research and development are exposed as food for thought. Embedded Tutorials give an insight of relevant topics usually starting from an introductory basis.

3.6 Hot Topic - Memristor based Computation-in-Memory Architecture for Data-Intensive Applications

Organisers: **Koen Bertels,** TU Delft, NL
Said Hamdioui, TU Delft, NL

3.8 Hot Topic - Design Methodologies for a Cyber-Physical Systems Approach to Personalized Medicine-on-a-Chip: Challenges and Opportunities

Organiser: **Krishnendu Chakrabarty,** Duke University, US

5.8 Hot Topic - The Next Generation of Virtual Prototyping: Ultra-fast yet Accurate Simulation of HW/SW Systems

Organisers: **Daniel Müller-Gritschneder,** Technische Universitaet München, DE
Oliver Bringmann, University of Tübingen, DE

6.6 Panel - The Future of Electronics, Semiconductor, and Design in Europe

Organiser: **Marco Casale-Rossi,** Synopsys, US

7.2 Hot Topic - Trading Accuracy for Efficient Computing

Organisers: **Anand Raghunathan,** Purdue University, US
Akash Kumar, National University of Singapore, SG

SPECIAL SESSIONS

7.3 Hot Topic - Advances in Hardware Trojans Detection

Organiser: **Julien Francq,** Airbus Defence & Space -- CyberSecurity, FR

8.5 Hot Topic - Spintronics based Computing

Organisers: **Weisheng Zhao,** University Paris-Sud/CNRS, FR
Lionel Torres, LIRMM, CNRS/University of Montpellier, FR

9.2 Hot Topic - Transparent Use of Accelerators in Heterogeneous Computing Systems

Organisers: **Heiner Giefers,** IBM Research Zurich, CH
Christian Plessl, University of Paderborn, DE

9.8 Hot Topic - Monolithic 3D: A Path to Real 3D Integrated Chips

Organisers: **Giovanni De Micheli,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Pierre-Emmanuel Gaillardon, École Polytechnique Fédérale de Lausanne (EPFL), CH

11.3 Hot Topic - Multi/Many-Core Programming: Where Are We Standing?

Organisers: **Jeronimo Castrillon,** Technische Universität Dresden, DE
Rainer Leupers, RWTH Aachen, DE

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EVENT OVERVIEW

MONDAY
- Educational Tutorials
- Fringe Meetings
- Welcome Reception
- ACM SIGDA/EDAA PhD Forum

TUESDAY
- Opening Plenary, DATE Awards Ceremony and Keynote Addresses
- Technical Conference
- Executive Sessions
- Lunchtime Keynote Session sponsored by Mentor Graphics
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings
- Exhibition Reception

WEDNESDAY
- Technical Conference
- Special Day on Designing Electronics for the Internet of Things and Keynotes
- Vendor Exhibition & Exhibition Theatre
- University Booth
- DATE Networking Event (DATE Party)

THURSDAY
- Technical Conference
- Special Day on Designing Electronics for Medical Applications and Keynote
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings

FRIDAY
- Special Interest Workshops

CONTACTS

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Eva Schubert
K.I.T. Group GmbH, DE
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MONDAY 09 MARCH

0730 – 0930	Tutorial Registration and Welcome Refreshments				
Breaks	1100-1130 Morning Coffee Break 1600-1630 Afternoon Coffee Break				
	Belle-Etoile	Meije	Chartreuse	Sept Laux	Les Bans
0930– 1300	M01 New Technologies: Spintronics: From Devices To Systems	M03 Embedded Systems: Embedded Memory Design for Future Technologies: Challenges, Solutions and Applications	M05 Automotive: Let's kick start electric vehicles!	M07 Low Power: Fixed-point refinement, a guaranteed approach towards energy efficient computing	M09 Testing: From Data to Actions: Applications of Data Analytics in Semi-conductor Manufac-turing & Test
1300 – 1430	Lunch Break				
1330	Conference registration begins				
	Belle-Etoile	Meije	Chartreuse	Sept Laux	Les Bans
1430 – 1800	M02 New Technologies: Spin Orbit Torque Magnetic Memories (SOT-MRAM): A Device to Architecture Review	M04 Embedded Systems: Functional Qualification: Applications in the C/C++ domain	M06 Automotive: Automotive Cyber-Physical Systems	M08 Low Power: The power of Power in future wireless smart systems for the Internet of Things	M10 Testing: Memory Test and Reliability in Nano-Era
1800 – 1900	Welcome Reception, Salle de Reception				
1900 – 2100	ACM SIGDA/EDAA PhD Forum, Salle de Reception				

TUESDAY 10 MARCH

0730	Registration and speaker's breakfast, room Les Écrins			
0830–1030	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses			
1030 – 1130	Exhibition and Coffee Break			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Oisans	Belle-Etoile	Stendhal	Chartreuse
1130 – 1300	2.1 New Opportunities in the Internet of Things	2.2 Adaptability for Low Power Computing	2.3 System Level Design Methods	2.4 Automotive Systems and Smart Energy Systems
1300 – 1430	Lunch Break Keynote session sponsored by Mentor Graphics, 1320-1420, room Oisans			
	Oisans	Belle-Etoile	Stendhal	Chartreuse
1430 – 1600	3.1 Extending Morre's Law & Heterogeneous Integration	3.2 Passive Implementation Attacks and Countermeasures	3.3 Loop Acceleration	3.4 Tackling Memory Walls with Emerging Architectures and Technologies
1600 – 1700	Coffee Break IP1 Interactive Presentations			
	Oisans	Belle-Etoile	Stendhal	Chartreuse
1700 – 1830	4.1 Trends and Challenges in Today's Automotive Semiconductors	4.2 Implementation and Verification of Security Components	4.3 Multi-/Manycore Scheduling	4.4 Exploring Reliability and Efficiency Tradeoffs at the Architectural Level
1830 – 1930	EXHIBITION RECEPTION			

TUESDAY 10 MARCH

Registration and speaker's breakfast, room Les Écrins				0730
1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses				0830–1030
Exhibition and Coffee Break				1030 – 1130
TRACK 5	TRACK 6	TRACK 7	TRACK 8	
Meije	Bayard	Les Bans	Lesdiguières	
2.5 Power of Assertions	2.6 Design and Analysis of Dependable Systems	2.7 Compilation and Code Transformations for Reconfigurable Computing	2.8 Facilities for Design and Fabrication for FDSOI IC	1130 – 1300
Lunch Break Keynote session sponsored by Mentor Graphics, 1320-1420, room Oisans				1300 – 1430
Meije	Bayard	Les Bans	Lesdiguières	
3.5 Breaking Simulation Boundaries	3.6 Hot Topic - Memristor based Computation-in-Memory Architecture for Data-Intensive Applications	3.7 Model-based Analysis and Verification	3.8 Hot Topic - Design Methodologies for a Cyber-Physical Systems Approach to Personalized Medicine-on-a-Chip: Challenges and Opportunities	1430 – 1600
Coffee Break IP1 Interactive Presentations				1600 – 1700
Meije	Bayard	Les Bans	Lesdiguières	
4.5 Industrial Test and Validation Experiments	4.6 Online Testing and Reliable Memories	4.7 How Resilient Are Emerging Technologies?	4.8 Strength by Interdisciplinary Research: The Cadence Academic Network	1700 – 1830
EXHIBITION RECEPTION				1830 – 1930

PLENARY SESSION
EXECUTIVE SESSION
SPECIAL SESSION
IP SESSION
EXHIBITION THEATRE
D-TRACK
A-TRACK
T-TRACK
E-TRACK

WEDNESDAY 11 MARCH

0730	Registration and speaker's breakfast, room Les Écrins			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
0830–1000	5.1 SPECIAL DAY Hot Topic: Applications of IoT	5.2 Hardware Trojan and Active Implementation Attacks	5.3 Variability Challenges in Nanoscale Circuits	5.4 Emerging Technologies for NoCs
1000 – 1100	Coffee Break IP2 Interactive Presentations			
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
1100 – 1230	6.1 SPECIAL DAY Hot Topic: Platforms for the IoT	6.2 Physical Unclonable Functions	6.3 Emerging Low Power Techniques	6.4 Bridging the Moore's Law Gap with Application-Specific Architectures
1230 – 1430	Lunch Break 7.0 SPECIAL DAY Keynotes, 1250 – 1420, room Oisans			
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
1430 – 1600	7.1 SPECIAL DAY Hot Topic: Design Tools for the IoT	7.2 Hot Topic - Trading Accuracy for Efficient Computing	7.3 Hot Topic - Advances in Hardware Trojans Detection	7.4 Routing Advances for Fault-tolerant and Multicast NoCs
1600 – 1700	Coffee Break IP3 Interactive Presentations			
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
1700 – 1830	8.1 SPECIAL DAY Panel: Security and Verification for the IoT	8.2 Flash Memories & Numerical Approximation	8.3 Dynamic Thermal Management for Multi-cores	8.4 Industrial System Design Opportunities
1930 – 2300	DATE Networking Event (DATE PARTY)			

WEDNESDAY 11 MARCH

	Registration and speaker's breakfast, room Les Écrins			0730
TRACK 5	TRACK 6	TRACK 7	TRACK 8	
Meije	Bayard	Les Bans	Lesdiguières	
5.5 Critical Embedded Systems	5.6 Analyzing and Improving Memories	5.7 Architectures and Design for Cyber-Physical Systems	5.8 Hot Topic - The Next Generation of Virtual Prototyping: Ultra-fast yet Accurate Simulation of HW/SW Systems	0830–1000
	Coffee Break IP2 Interactive Presentations			1000 – 1100
Meije	Bayard	Les Bans	Lesdiguières	
6.5 Multimedia and Consumer Electronics	6.6 Panel – The Future of Electronics, Semiconductor, and Design in Europe	6.7 Application-Mapping Strategies for Many-Cores	6.8 → 6.6 in room Bayard	1100 – 1230
	Lunch Break 7.0 SPECIAL DAY Keynotes, 1250 – 1420, room Oisans			1230 – 1430
Meije	Bayard	Les Bans	Lesdiguières	
7.5 System Reliability: from Runtime to Design Languages	7.6 Test Power and 3-D Fault Tolerance	7.7 Energy-efficient Computing	7.8 Critical Research Areas Driven by Industry Transformations	1430 – 1600
	Coffee Break IP3 Interactive Presentations			1600 – 1700
Meije	Bayard	Les Bans	Lesdiguières	
8.5 Hot Topic - Spintronics based Computing	8.6 Statistical Answers to Analog/Mixed Signal Design and Test Problems	8.7 Compilers and Tools for Performance	8.8 Share a Fab - Multi Project Wafers Enable Your Innovations	1700 – 1830
	DATE Networking Event (DATE PARTY)			1930 – 2300

THURSDAY 12 MARCH

0730	Registration and speaker's breakfast, room Les Écrins			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
0830–1000	9.1 SPECIAL DAY Hot Topic: Game-changing Innovative Technology Platforms for Health Care	9.2 Hot Topic - Transparent Use of Accelerators in Heterogeneous Computing Systems	9.3 NoC Optimization	9.4 Advanced Trends in Alternative Technologies
1000 – 1100	Coffee Break IP4 Interactive Presentations			
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
1100 – 1230	10.1 SPECIAL DAY Hot Topic: Wearable Medical Applications	10.2 Emerging Memory Architectures	10.3 Modern Architectures for Real-Time Systems	10.4 Energy Aware Data Center: Design and Management
1230 – 1400	Lunch Break Best IP Award Presentation, 1315-1320, room Oisans 11.0 SPECIAL DAY Keynote, 1320-1350, room Oisans			
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
1400 – 1530	11.1 SPECIAL DAY Hot Topic: Implantable Medical Applications	11.2 Variability and Robustness for Emerging Technologies	11.3 Hot Topic - Multi/ Many-Core Programming: Where Are We Standing?	11.4 Logic Synthesis: the Faithful, the Approximate and the Stochastic
1530 – 1600	Coffee Break IP5 Interactive Presentations			
	Salle Oisans	Belle-Etoile	Stendhal	Chartreuse
1600 – 1730	12.1 SPECIAL DAY Hot Topic: Technology and Design Platforms for Diagnostics	12.2 Solver Advances and Emerging Applications	12.3 Patterning, Pairing, Placement and Packing	12.4 High-Level Specifications and Models

THURSDAY 12 MARCH

	Registration and speaker's breakfast, room Les Écrins				0730
	TRACK 5	TRACK 6	TRACK 7	TRACK 8	
	Meije	Bayard	Les Bans	Lesdiguières	
0830–1000	9.5 Modeling and Simulation of Extra-Functional Properties	9.6 Design, Synthesis and Validation of Analog Circuits	9.7 Test Generation, Fault Simulation and Diagnosis	9.8 Hot Topic - Monolithic 3D: A Path to Real 3D Integrated Chips	0830–1000
1000 – 1100	Coffee Break IP4 Interactive Presentations				1000 – 1100
	Meije	Bayard	Les Bans	Lesdiguières	
1100 – 1230	10.5 Reconfigurable Architectures and Applications	10.6 Circuit Design and Test: From Characterization to Measurement	10.7 Expanding the Applicability of Formal Methods	10.8 From IP to EDA Tools Enterprise Management: What is so special?	1100 – 1230
1230 – 1400	Lunch Break Best IP Award Presentation, 1315-1320, room Oisans 11.0 SPECIAL DAY Keynote, 1320-1350, room Oisans				1230 – 1400
	Meije	Bayard	Les Bans	Lesdiguières	
1400 – 1530	11.5 Ultra-low Power Devices for Health and Rehabilitation	11.6 Video Architectures for Multimedia and Communications	11.7 Exploiting Dark Silicon	11.8 (1400-1500) Exhibition Keynote: Designing Systems for the Connected Autonomous Future	1400 – 1530
1530 – 1600	Coffee Break IP5 Interactive Presentations				1530 – 1600
	Meije	Bayard	Les Bans	Lesdiguières	
1600 – 1730	12.5 New Perspectives in Next-Generation Medical Systems	12.6 Medical Design Automation: Is All That Simulation and Model Reduction Getting Into Your "Head"?	12.7 Brain Health and Mental Disorders: new challenges for electronic engineers	12.8 (1500-1730) Tutorial: An Industry Approach to FPGA/ARM System Development and Verification	1600 – 1730

SPECIAL SESSION
IP SESSION
SPECIAL DAY SESSION
EXHIBITION THEATRE
D-TRACK
A-TRACK
T-TRACK
E-TRACK

FRIDAY 13 MARCH

0730 – 0830	Workshop Registration and Welcome Refreshments			
Breaks	Please see individual workshop programmes for lunch and break times			
0830 – 1600 Meije	0830 – 1630 Bayard	0830 – 1600 Stendhal	0830 – 1630 Berlioz	0815 – 1730 Belle-Etoile
W01 1st Workshop on Model-Implementation Fidelity (MiFi)	W02 Design Automation of Things: EV Battery Packs	W03 2nd International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2015)	W04 DUHDe – 2nd Workshop on Design Automation for Understanding Hardware Designs	W05 3D Integration Technology, Architecture, Design, Package, Automation, and Test
0830 – 1700 Chartreuse	0830 – 1630 Salle Lesdiguières	0830 – 1700 Sept Laux 4	0830 – 1630 Sept Laux 5	0830 – 1700 Les Bans
W06 Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN)	W07 Designing with Uncertainty - Opportunities & Challenges	W08 Heterogeneous Architectures and Design Methods for Embedded Image Systems	W09 International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)	W10 TRUDEVICE 2015: Workshop on Trustworthy Manufacturing and Utilization of Secure Devices

TUTORIALS — MONDAY 09 MARCH

0730-0930	**REGISTRATION AND TUTORIAL WELCOME REFRESHMENTS**
0930-1300	**TUTORIALS** (1100-1130 Coffee Break)
M01 Belle-Etoile	**NEW TECHNOLOGIES: SPINTRONICS: FROM DEVICES TO SYSTEMS**
M03 Meije	**EMBEDDED SYSTEMS: EMBEDDED MEMORY DESIGN FOR FUTURE TECHNOLOGIES: CHALLENGES, SOLUTIONS AND APPLICATIONS**
M05 Chartreuse	**AUTOMOTIVE: LET'S KICK START ELECTRIC VEHICLES!**
M07 Sept Laux	**LOW POWER: FIXED-POINT REFINEMENT, A GUARANTEED APPROACH TOWARDS ENERGY EFFICIENT COMPUTING**
M09 Les Bans	**TESTING: FROM DATA TO ACTIONS: APPLICATIONS OF DATA ANALYTICS IN SEMICONDUCTOR MANUFACTURING & TEST**
1300-1430	**LUNCH BREAK**
1330	**CONFERENCE REGISTRATION BEGINS**
1430-1800	**TUTORIALS** (1600-1630 Coffee Break)
M02 Belle-Etoile	**NEW TECHNOLOGIES: SPIN ORBIT TORQUE MAGNETIC MEMORIES (SOT-MRAM): A DEVICE TO ARCHITECTURE REVIEW**
M04 Meije	**EMBEDDED SYSTEMS: FUNCTIONAL QUALIFICATION: APPLICATIONS IN THE C/C++ DOMAIN**
M06 Chartreuse	**AUTOMOTIVE: AUTOMOTIVE CYBER-PHYSICAL SYSTEMS**
M08 Sept Laux	**LOW POWER: THE POWER OF POWER IN FUTURE WIRELESS SMART SYSTEMS FOR THE INTERNET OF THINGS**
M10 Les Bans	**TESTING: MEMORY TEST AND RELIABILITY IN NANO-ERA**
1800-1900	**WELCOME RECEPTION**
1900-2100	**ACM SIGDA /EDAA PHD FORUM**

TUTORIALS

M01 New Technologies: Spintronics: From Devices To Systems

Belle-Etoile 0930 — 1300

Organiser **Rangharajan Venkatesan,** Purdue, US

Invited Speakers
Kaushik Roy, Purdue University, US
Anand Raghunathan, Purdue University, US
Rangharajan Venkatesan, Purdue, US

With the scaling of CMOS technology approaching its fundamental limits, several new technologies are being actively explored as potential replacements. Among them, spintronics, which uses electron "spin" rather than "charge" as a state variable is considered to be a promising direction for the post-CMOS era. Spintronic devices are well-suited for realizing memories that are highly dense and non-volatile, i.e., have very low leakage power, compared to their CMOS counterparts such as SRAM and DRAM, and therefore have great potential to revolutionize the storage and computing capabilities of future systems. Further, spintronic devices have certain unique characteristics that make them highly efficient for non-Boolean computing. In addition to extensive research efforts over the decade, multiple industrial prototypes and early commercial offerings of spintronic memories underscore the great interest in this field.

This tutorial presents a devices-to-systems overview of the state-of-the-art in the design of spintronic computing systems. The first part of the tutorial focuses on the design of memory hierarchies with different spintronic technologies – Spin Transfer Torque Magnetic RAM (STT-MRAM), Domain Wall Memory (DWM), Spin-Hall Magnetic RAM (SH-MRAM). We show that spintronic memories fundamentally change the design landscape in terms of read-write stability, density, energy, and performance and pose certain unique challenges such as high write latency and energy, asymmetry in write operations, variable access latency, etc. We survey a wide range of device, circuit and architectural techniques to address the challenges associated with spintronic memories.

The second part of this tutorial focuses on the design of spintronic logic. Realizing Boolean logic with spintronic devices is considerably more challenging than memory. We will describe various proposals for spintronic Boolean logic families and compare their merits and demerits with CMOS. Re-configurable fabrics, which make extensive use of memory to store logic functions and interconnect configurations, offer an opportunity to harness the efficiency of spintronic memory for logic design. This tutorial will cover proposals for spintronic reconfigurable fabrics and memory-based computing. Further, spintronic devices are highly promising in certain application domains that match their characteristics. We present one such application – neuromorphic computing, the design of computing systems that mimic the functionality of the human brain. Neuromorphic computing has received great interest in the last decade in several applications involving classification, recognition, search, and inference and is used in real-world systems such as Google+ image search, Apple Siri voice recognition, etc. We describe recent efforts to use spintronic devices for realizing the building blocks of artificial neural networks, viz. neurons and synapses, and to utilize these primitives for large-scale neuromorphic computing.

0930 **SESSION 1**

0930 **INTRODUCTION TO SPINTRONICS**
Speaker: Kaushik Roy, Purdue University, US

1000 **SPINTRONIC MEMORIES: DEVICES AND BIT-CELLS**
Speaker: Kaushik Roy, Purdue University, US

1045 **SPINTRONIC MEMORY HIERARCHIES**
Speaker: Rangharajan Venkatesan, Purdue, US

1200 **SESSION 2**

1200 **SPINTRONIC LOGIC DEVICES**
Speaker: Kaushik Roy, Purdue University, US

1220 **BOOLEAN AND NON-BOOLEAN COMPUTING WITH SPINTRONIC DEVICES**
Speaker: Anand Raghunathan, Purdue University, US

M02 New Technologies: Spin Orbit Torque Magnetic Memories (SOT-MRAM): A Device to Architecture Review

Belle-Etoile 1430 — 1800

Organiser **Mehdi Tahoori,** Karlsruhe Institute of Technology, DE

Invited Speakers
Pietro Gambardella, Department of Materials, ETH Zurich, CH
Gregory Di Pendina and Guillaume Prenat, Spintec / CEA-CNRS, FR
Mehdi Tahoori, Karlsruhe Institute of Technology, DE

The microelectronics industry will face major challenges related to power dissipation and energy consumption in the next years. Both static and dynamic power consumption (already dominated by the leakage power) will soon start to limit microprocessor performance growth. Multicore processors will not be able to afford keeping more than a very small fraction of all cores active at any given moment and their scaling will soon hit a power wall. A promising way to stop this trend is the integration of non-volatility as a new feature of memory caches, which would immediately minimize static power as well as paving the way towards normally-off/instant-on computing. The development of an electrically addressable Non Volatile Memory (NVM) combining high speed and high endurance is essential to achieve these goals. Among the recent emerging memories, Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) has been identified by the ITRS as the most credible candidate. However STT-MRAM still suffers from i) lack of speed for fast cache application, ii) potential endurance issues due to the large current injected through the tunnel barrier that can be damaged during the switching of the magnetization, and, iii) reliability issues due to read disturb caused by the common reading and writing paths.

There is a new spin-based technology, called "Spin Orbit Torque" (SOT), which can be viewed as the ultimate evolution of STT. It offers the same non-volatility and compliance with technological nodes below 22nm, with the addition of potentially lower power consumption, cache-compatible high speed compatibility, and truly infinite endurance. Moreover, since the SOT-MTJ is a 3-terminal device, reading and writing paths are completely separated, giving an intrinsic behavioral robustness.

The objective of this tutorial is to bring the attention of design automation community to this novel emerging magnetic technology for integrated circuit design, including the challenges and opportunities provided by this novel technology, from magnetic layer all the way to architecture and system level issues. The presenters in this tutorial will cover various aspects from physics and device, circuit, and architecture.

1430 **SPIN-ORBIT-TORQUE SPINTRONIC DEVICE AND TECHNOLOGY**
Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE, Contact Mehdi Tahoori

1430 **SPIN-ORBIT-TORQUE SPINTRONIC DEVICE AND TECHNOLOGY**
Speaker: Pietro Gambardella, Department of Materials, ETH Zurich, CH

1450 **HYBRID CMOS/MAGNETIC NON-VOLATILE STANDARD CELL DESIGN FLOW**
Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE, Contact Mehdi Tahoori

1450 **HYBRID CMOS/MAGNETIC NON-VOLATILE STANDARD CELL DESIGN FLOW**
Speakers: Gregory Di Pendina and Guillaume Prenat, Spintec / CEA-CNRS, FR

1500 **MEMORY AND SYSTEM ARCHITECTURE DESIGN USING SOT-MRAM**
Chair: Guillaume Prenat, Spintec / CEA-CNRS, FR, Contact Guillaume Prenat

1500 **MEMORY AND SYSTEM ARCHITECTURE DESIGN USING SOT-MRAM**
Speaker: Mehdi Tahoori, Karlsruhe Institute of Technology, DE

M03 Embedded Systems: Embedded Memory Design for Future Technologies: Challenges, Solutions and Applications

Meije 0930 — 1300

Organiser **Swaroop Ghosh,** University of South Florida, US

Invited Speakers

Swaroop Ghosh, University of South Florida, US
Swarup Bhunia, Case Western Reserve University, US
Jaydeep Kulkarni, Intel Corporation, US

Conventional CMOS memory i.e., Static Random Access Memory (SRAM) has been the popular choice for embedded memory application for last several decades. However, SRAM seems to be approaching a brick wall. On one hand process variability and leakage power is posing severe obstruction towards SRAM scaling to future nodes and on the other hand, emerging energy-constrained and bandwidth hungry electronic gadgets demand for larger as well as energy-efficient on-chip cache which cannot be satisfied with SRAM. To address the changing landscape of consumer market, there is a corresponding need of changing the design paradigm. What is really needed is a memory technology that s at least 50-100X denser, 1000X energy-efficient and as fast as SRAM. Several emerging memory technologies are on the horizon but there is no clear universal choice for embedded application. This tutorial will explore the latest trends in the embedded memory segment and discuss the fundamental limitations of SRAM in meeting the new needs of the electronic systems. The complex (and not very well understood) inter-relationships between memory density, bandwidth, latency, power and speed will be elaborated. The tutorial will discuss most promising emerging memory technologies where storage element is based on charge, spin and resistance. The specific focus will be on the operating principles, design challenges and solutions of non-volatile memories (NVM) such as Spin Transfer Torque RAM (STTRAM), Domain Wall Memory (DWM) and Resistive RAM (RRAM). New applications of the emerging memory technologies for exciting applications such as memory-based computations, hardware security and neuromorphic computing will also be presented.

0930 **INTRODUCTION AND MOTIVATION**

STATIC RANDOM ACCESS MEMORY

SPINTRONIC MEMORY

RESISTIVE RAM

CONCLUSIONS AND DISCUSSIONS

M04 Embedded Systems: Functional Qualification: Applications in the C/C++ domain

Meije 1430 — 1800

Organiser **Florian Letombe,** Synopsys, FR
General Chair **Ali Abbara,** Synopsys, FR

Invited Speakers

Susanne Kandl, Vienna University of Technology, AT
Stéphane Bouvier, ST Microelectronics, FR
Jürgen Hanisch, Robert Bosch GmbH, DE
Jean-Marc Forey, Synopsys, FR
Olivier Sentieys, INRIA - University of Rennes 1, FR

The amount of effort spent creating, debugging and maintaining a typical verification environment often outstrips the effort spent on the design itself. Measuring the effectiveness of verification is critical to ensuring high-quality, bug-free designs. As the use of languages like C/C++ to represent portions of the design continues to increase, the ability to obtain such measurements via traditional techniques becomes difficult.

This tutorial describes the fundamental aspects of functional verification that remain invisible to existing verification tools. It introduces the origins and the main concepts of a technology that allows this gap to be closed: mutation-based testing.

Certitude™'s mutation-based approach assesses verification effectiveness by measuring the environment's ability to activate, propagate and detect potential bugs. This technique, in use with RTL designs for years, can now be applied to components described in C/C++, with similar benefits. This tutorial will cover the following:

- A primer on the use and operation of Certitude;
- An overview of how these techniques can be applied to components described in C/C++;
- A survey of specific applications and benefits in the C/C++ domain.

1430 **MUTATION-BASED TESTING: ORIGINS, CONCEPTS, AND APPLICATIONS**
Chair: Ali Abbara, Synopsys, FR, Contact Ali Abbara
Co-Chair: Florian Letombe, Synopsys, FR, Contact Florian Letombe

1430 **CERTITUDE-C/C++ : A FUNCTIONAL QUALIFICATION TOOL FOR FAULT INJECTION IN C/C++/SYSTEMC MODELS**
Speaker: Jean-Marc Forey and Ali Abbara, Synopsys, FR

1530 **HOW MUTATIONS CAN HELP TO PROVE THAT YOUR SYSTEM DOES NOT CONTAIN (UNWANTED) MUTATIONS**
Speaker: Susanne Kandl, Vienna University of Technology, AT

1630 **APPLYING CERTITUDE ON AUTOMOTIVE AND MULTIMEDIA C/C++/SYSTEMC MODELS**
Chair: Ali Abbara, Synopsys, FR, Contact Ali Abbara
Co-Chair: Florian Letombe, Synopsys, FR, Contact Florian Letombe

1630 **MULTIMEDIA IPS VERIFICATION QUALITY IMPROVEMENT : USAGE OF CERTITUDE ON C/C++ MODELS**
Speaker: Stéphane Bouvier, STMicroelectronics, FR

M05 Automotive: Let's kick start electric vehicles!

Chartreuse 0930 — 1300

Organiser **Davide Quaglia,** EDALab s.r.l., IT

Invited Speakers

Martin Lukasiewycz, TUM CREATE, SG
Riccardo Muradore, University of Verona, IT
Sebastian Steinhorst, TUM CREATE, SG
Massimo Poncino, Politecnico di Torino, IT

Future electric vehicle E/E architectures will bring disruptive changes to many areas of automotive design automation and system design. This tutorial will give both insights into which changes to expect and how these changes can help to design automotive systems more effectively. Topics such as communication-controller co-design, advanced battery management, verification approaches and system-level simulation have been relevant in the research community. The organizers of this tutorial believe, however, that it is now the time to bring a condensed overview of these topics to a wider audience, clearly focusing on applicability and relevance to all researchers and practitioners to stimulate adoption of best practices established over recent years as well as bleeding edge approaches.

The tutorial is targeted towards students, researchers and practitioners belonging to both academia and industry and concerned with:

- Electric Vehicle Architectures
- Automotive Electronics
- Automotive Communication Architecture Design
- Advanced Electrical Energy Storages
- Networked Control Systems

The presentations will report concrete case studies, e.g. , the electric vehicle built by TUM CREATE in Singapore (http://www.eva-taxi.sg), thus showing how the presented concepts support the design and verification of actual electric vehicles.0930 Session 1

0930 **SESSION 1**
Chair: Davide Quaglia, EDALab s.r.l., IT, davide.quaglia@edalab.it

0930 **INTRODUCTION TO ELECTRIC VEHICLES: KEY ASPECTS AND DESIGN CHALLENGES**
Speaker: Martin Lukasiewycz, TUM CREATE, SG

1015 **BATTERY MANAGEMENT IN ELECTRIC VEHICLES**
Speaker: Sebastian Steinhorst, TUM CREATE, SG

1130 **SESSION 2**
Chair: Martin Lukasiewycz, TUM CREATE, SG

1130 **JOINT CONTROLLER-COMMUNICATION DESIGN IN ELECTRIC VEHICLES**
Speaker: Riccardo Muradore, University of Verona, IT

1215 **SYSTEM-LEVEL SIMULATION OF ELECTRIC VEHICLES**
Speaker: Davide Quaglia, EDALab s.r.l., IT

M06 Automotive: Automotive Cyber-Physical Systems

Chartreuse 1430 — 1800

Organiser **Samarjit Chakraborty,** TU Munich, DE

Invited Speakers

Samarjit Chakraborty, TU Munich, DE
Rafik Henia, Thales, FR
Arne Hamann, Robert Bosch GmbH, DE

Tutorial abstract: Modern high-end cars have many electronic control units (ECUs) that are connected by a complex communication architecture and are used to support various control applications ranging over safety-critical, driver assistance and comfort-related functions. Traditionally, such control applications are designed using a model-based approach – e.g., using Matlab/Simulink – where many idealistic assumptions about the implementation platform are made. These include the availability of infinite precision for mathematical computations, control laws being computed in negligible time, and delays from sensor to controller and controller to actuator being negligible. Models based on these assumptions are then used to automatically generate, e.g., C code representing the control applications. Such code is then partitioned into tasks, which are then mapped onto the in-vehicle distributed architecture.

However, in such a setup, the idealistic assumptions made at the model level, for control algorithm design, do not hold true at the implementation level. This is referred to as the semantic gap, and leads to a deviation in the control performance between what is expected at the model level and what is obtained in practice. In order to close this gap, a considerable effort is spent on integration, testing and debugging which significantly increases the development cost and poses an obstacle towards certification. The goal of this tutorial is to highlight these problems and present approaches currently being developed in the area of cyber-physical systems towards co-design of control algorithms and their implementation platforms.

Intended audience and scope:This tutorial will be beneficial to both academic researchers as well as practitioners from the industry. It is primarily intended towards an audience with a background in embedded systems and software (i.e., a typical DATE audience). No background in control theory or formal verification will be assumed. The level of the tutorial will be from intermediate to advanced. While the study of cyber-physical systems is gaining importance, there is still some confusion on – What exactly are cyber-physical systems? How are they different from embedded systems? etc. This tutorial will discuss embedded control systems as one possible domain of cyber-physical systems and position this with respect to other domains like sensor networks, Internet-of-things (IoT) and networked control systems. The tutorial will also introduce the intersection of embedded systems and control theory and will appeal to those who have a background in embedded systems and are starting to work on cyber-physical systems.

M07 Low Power: Fixed-point refinement, a guaranteed approach towards energy efficient computing

Sept Laux 0930 – 1300

Organiser **Olivier Sentieys,** INRIA - University of Rennes 1, FR

Invited Speakers
Daniel Menard, INSA Rennes/IETR, FR
David Novo, EPFL, CH
Karthick Parashar, IMEC, BE

Emerging smart systems market is constantly pushing for miniaturization and reduction in form-factors even while the demand for computation is steadily increasing. Surmounting the so-called "power-wall" and achieving higher number of computations at the expense of unit energy is increasingly becoming a challenge. Software-defined modems or video applications, which are under constant pressure for reaching the market expectations set by modern communication standards, are a classic example of this phenomenon.

In this tutorial, we demonstrate how careful tuning of the fixed-point arithmetic used to implement numerous signal processing algorithms can lead to better system performance parameters irrespective of the chosen implementation platform. The choice of fixed-point word-lengths has a direct impact on area, latency and energy consumption of hardware designs implemented as ASICs or realized on FPGAs. With the growing complexity of hardware designs, paradigms enabling further design automation, such as high level synthesis (HLS), are becoming a must to achieve a competitive product design cycle. Importantly, efficient automatic fixed-point refinement is essential for HLS to approach the quality of hand-tuned hardware designs. Furthermore, several popular embedded computer architectures support Single Instruction Multiple Data (SIMD). In all such architectures, shorter bit-widths can potentially benefit from high order of vectorization at the cost of a controlled loss in accuracy. Changing data-level parallelism by modifying bit widths has an impact on the throughput, latency and eventually the energy profile of the processor. Processor's performance and accuracy of computation is therefore an important design trade-off for achieving efficient implementations.

This tutorial packs nearly a decade worth of research in designing fixed-point systems for signal processing. It broadly consists of two parts. In the first part, we expose the deficiency in the support offered by existing fixed-point evaluation tools and motivate the need for new solutions. Accordingly, we put into perspective several recent techniques that have been developed to facilitate a quick analysis of the impact of a selected fixed-point format on the accuracy of the system. In the second part, we focus on the processor architecture - compiler ecosystem. Here, we explore opportunities to improve energy efficiency by appropriately dimensioning the bit widths of variables used to represent signals. For this, we reflect upon a recent promising idea called soft SIMD that provides insights on the impact of choice of bit widths on SIMD vectorization, and describe novel techniques for jointly achieving optimized sub-word parallelism and fixed-point refinement. We also expose some energy reduction approaches that are uniquely available for processor-based and accelerator-based implementations. Along this tutorial, we use several examples from the signal and video processing domain and a complete wireless application to illustrate the impact of fixed-point refinement on the system performance.

In summary, with this tutorial we challenge the extended dogma of starting the application mapping onto software or hardware from a typed specification (i.e., the variables are already defined with standard data types such as int, short, etc.), which has already obscured the potential for significant optimizations, especially in terms of performance and energy efficiency.

0930 **FIXED-POINT REFINEMENT, A GUARANTEED APPROACH TOWARDS ENERGY EFFICIENT COMPUTING: PART I**
Organiser: Olivier Sentieys, INRIA - University of Rennes [1], FR, Contact Olivier Sentieys

0930 **1. INTRODUCTION**
Speaker: Olivier Sentieys, INRIA - University of Rennes [1], FR

0945 **2. FIXED-POINT ARITHMETIC**
Speaker: Olivier Sentieys, INRIA - University of Rennes [1], FR

1015 **3. FINITE WORD-LENGTH EFFECT ANALYSIS**
Speaker: Daniel Menard, INSA Rennes/IETR, FR

MONDAY 09 MARCH, 2015

DATE15
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MON

1130 **FIXED-POINT REFINEMENT, A GUARANTEED APPROACH TOWARDS ENERGY EFFICIENT COMPUTING: PART II**
Organiser: Olivier Sentieys, INRIA - University of Rennes 1, FR

1130 **4. HIGH-LEVEL SYNTHESIS UNDER ACCURACY CONSTRAINT**
Speaker: Karthick Parashar, IMEC, Leuven, BE

1215 **5. SIMD VECTORIZATION UNDER ACCURACY CONSTRAINT**
Speaker: David Novo, EPFL, CH

1235 **6. OPPORTUNISTIC RUN-TIME PRECISION ADAPTATION**
Speaker: David Novo, EPFL, CH

1250 **7. CONCLUSION AND OPEN RESEARCH DIRECTIONS**
Speaker: David Novo, EPFL, CH

M08 Low Power: The power of Power in future wireless smart systems for the Internet of Things

Sept Laux 1430 — 1800

Organiser **Massimo Poncino,** Politecnico di Torino, IT

Invited Speakers
Davide Quaglia, EDALab s.r.l., IT
Alain Pegatoquet, LEAT/University of Nice Sophia Antipolis, FR
Massimo Poncino, Politecnico di Torino, IT

In the future, objects and people will be almost permanently connected and exchanging information in the so-called Internet of Things (IoT). While the potential influence of IoT in our daily life is enormous, there are major challenges related to its energy sustainability. Also in the healthcare domain, progress in microelectronics has enabled the miniaturization of data processing elements, radio transceivers and sensors for medical applications. However, the inherent resource-constrained nature of these systems, coupled with the specific operating conditions and the stringent autonomy requirements pose important design challenges. The evolution of battery energy density is below the curve of Moore's law thus making power consumption the limiting factor of next-generation smart systems. Furthermore, technology allows integrating various types of energy harvesting devices, which are able to scavenge energy from the environment thus potentially compensating the increased gap between the energy demand and its availability.

This tutorial addresses all these issues involving energy management in autonomous wireless devices from a novel perspective. As a matter of fact, while the analysis and the optimization of how energy is consumed in electronic systems has been the subject of many studies, a lot of misconceptions are still around when it comes to how optimally generate, store, convert and distribute the energy available in a system that incorporates energy generation and storage devices.

The tutorial will cover the following key topics:

1) Architecture of wireless autonomous smart systems and design challenges
2) Energy storage devices: background and non-idealities, models and design guidelines, conversion issues
3) Energy harvesting techniques and architectures for energy neutral systems
4) Power management policies and protocols for autonomous objects
5) Modeling and simulation techniques
6) Trends for future wireless smart systems

The presentations will report results from SMAC and CONTREX European projects and will be accompanied by actual case studies, showing how the presented concepts support the design and verification of wireless autonomous smart systems.

The tutorial is targeted towards students and pratictioners belonging to both academia and industry and concerned with design of advanced wireless embedded systems (e.g., wearables, smart metering, body sensor networks, etc).

1430 SESSION 1
Chair: Davide Quaglia, EDALab s.r.l., IT

1430 INTRODUCTION TO AUTONOMOUS WIRELESS SMART SYSTEMS AND DESIGN CHALLENGES
Speaker: Davide Quaglia, EDALab s.r.l., IT

1500 ENERGY STORAGE DEVICES: CHARACTERISTICS, NON-IDEALITIES AND DESIGN CHALLENGES
Speaker: Massimo Poncino, Politecnico di Torino, IT

1630 SESSION 2
Chair: Alain Pegatoquet, LEAT/University of Nice Sophia Antipolis, FR

1630 MANAGING POWER TO ENABLE AUTONOMOUS COMMUNICATING OBJECTS
Speaker: Alain Pegatoquet, LEAT/University of Nice Sophia Antipolis, FR

1730 HOLISTIC MODELING AND SIMULATION TECHNIQUES
Speaker: Davide Quaglia, EDALab s.r.l., IT

MONDAY 09 MARCH, 2015

DATE15
March 9—13, 2015, Grenoble, France
MON

M09 Testing: From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test

Les Bans 0930 — 1300

Organisers **Haralampos Stratigopoulos,** TIMA Laboratory, FR
Yiorgos Makris, The University of Texas at Dallas, US

Invited Speakers
Haralampos Stratigopoulos, TIMA Laboratory, FR
Yiorgos Makris, The University of Texas at Dallas, US

Throughout the design and production lifetime of an integrated circuit, a wealth of data is collected for ensuring its robust and reliable operation. Ranging from design-time simulations to process characterization monitors on first silicon, and from high-volume specification tests to diagnostic measurements on chips returned from the field, the information inherent in this data is invaluable. At the same time, the need for cost-effective solutions for various test-related tasks is becoming more pressing, especially in complex mixed-signal Systems-on-Chip. As a result, using data analytics methods to mine this information and identify meaningful correlations has seen intense interest and numerous breakthroughs have been made during the last decade. To motivate the need, the challenges, and the benefits of using data analytics, this tutorial will discuss its utility on the following actual industrial problems: (a) extraction of wafer-level spatial and lot-level spatiotemporal correlation and utilization in test cost reduction, process monitoring, and yield learning, (b) test cost reduction through replacement of costly tests by low-cost alternatives and/or elimination of superfluous tests, either statically or adaptively during test application, and (c) pre-deployment evaluation of candidate test methods through probabilistic test metrics. This tutorial is intended for (a) process and test engineers who wish to understand the utility of data analytics in their practice, (b) graduate students/faculty/researchers who wish to familiarize with the state-of-the-art and conduct research in this domain, and (c) data analytics experts who wish to apply their expertise on semiconductor manufacturing data.

0930 INTRODUCTION

0930 DATA ANALYTICS OPPORTUNITIES IN SEMICONDUCTOR MANUFACTURING AND TEST
Speaker: Yiorgos Makris, The University of Texas at Dallas, US

0945 WAFER-LEVEL VARIATION ANALYSIS AND APPLICATIONS

0945 FUNDAMENTALS OF SPATIAL AND SPATIOTEMPORAL VARIATION MODELING
Speaker: Yiorgos Makris, The University of Texas at Dallas, US

1015 TEST COST REDUCTION THROUGH STATISTICAL ESTIMATION USING INTER-DIE CORRELATIONS
Speaker: Yiorgos Makris, The University of Texas at Dallas, US

1045 PROCESS MONITORING, OUTLIER DETECTION, AND YIELD LEARNING
Speaker: Yiorgos Makris, The University of Texas at Dallas, US

1130 STATISTICAL LEARNING IN TEST

1130 FUNDAMENTALS OF MACHINE LEARNING AND ITS APPLICATIONS IN TEST
Speaker: Haralampos-G. Stratigopoulos, TIMA Laboratory, FR

1200 ADAPTIVE TEST
Speaker: Haralampos-G. Stratigopoulos, TIMA Laboratory, FR

1230 PROBABILISTIC TEST METRICS FOR EVALUATING ALTERNATIVE LOW-COST TESTS
Speaker: Haralampos-G. Stratigopoulos, TIMA Laboratory, FR

M10 Testing: Memory Test and Reliability in Nano-Era

Les Bans 1430 — 1800

Organizer **Said Hamdioui,** Delft University of Technology, NL

Invited Speakers
Said Hamdioui, Delft University of Technology, NL
Kanad Kanad Chakraborty, Lattice Semiconductor

The objective is to provide attendees with an overview of memory test, reliability and yield improvement.

In terms of testing, aspects such as fault modeling, test design and BIST will be covered. Traditional fault modeling and advanced ones for current and future technologies are covered. Systematic methods are presented for designing and optimizing tests, supported by industrial results from different companies (e.g. Intel, ST, Infineon) in order to get better insight in the test effectiveness. State-of-the art and novel BIST architectures are covered. Testing of some emerging memories is discussed.

In terms of reliability and yield improvement, effects of process scaling and environment on reliability failures caused by static noise (contributed by crosstalk, IR-drop, threshold voltage variation, negative-bias temperature instability, and random telegraph noise), hot carrier injection (HCI), gate oxide breakdown, latchup, metallization reliability failures and electrostatic discharge/electrical overstress (ESD/EOS) will be discussed. Industry practices for designing for reliability are discussed. Traditional reliability testing approaches such as burn-in, IDDQ/IDD, parametric and at-speed functional testing, and present-day adaptive and data-driven approaches are covered. Self-repair and yield/reliability tradeoffs and yield modeling of repairable memories is discussed. Yield learning based on correlation to defect inspection and physical failure analysis is highlighted. Improved RAM circuit design techniques for noise and SEU mitigation are discussed, together with an overview of ECC approaches.

Finally, future challenges in memory testing and reliability are highlighted.

1430 SESSION 1
Said Hamdioui, Delft University of Technology

INTRODUCTION
Quality versus Reliability
Importance of test
Importance of reliability

FAULT MODELS, TESTS AND INDUSTRIAL RESULTS
Defects v fault models
Classification of memory fault models
Static fault models
Dynamic fault models
Test algorithms
Industrial results
Summary

MEMORY BIST ARCHITECTURE
Motivation
Space of algorithms and stresses
MBIST Classification
Algorithm based MBIST architecture
Generic March Element MBIST architecture
March element MBIST architecture
Memory operation based MBIST
Comparison

TESTING EMERGING MEMORIES
Testing Resistive RAMS
Testing stacked 3D ICs
Testing MRAMS

1630 SESSION 2
Kanad Kanad Chakraborty, Lattice Semiconductor

RELIABILITY IN MEMORIES
Motivation
Impact of scalability on memory reliability
- **Supply voltage and power constraints**
- **Threshold voltage control**
- **Gate-oxide reliability**
- **Hot-carrier degradation**
- **Latchup susceptibility**
- **ESD/EOS and metallization reliability**

TECHNICAL PROGRAMME

1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses

Auditorium Dauphiné 0830 - 1030

Chair: **Wolfgang Nebel,** OFFIS & University of Oldenburg, DE
Co-Chair: **David Atienza,** EPFL, CH

0830 **WELCOME ADDRESSES**
Wolfgang Nebel
DATE 2015 General Chair, OFFIS & University of Oldenburg, DE

David Atienza
DATE 2015 Programme Chair, EPFL, CH

0845 **PRESENTATION OF DISTINGUISHED AWARDS**

DATE 2015 Best Paper Award

2015 EDAA Lifetime Achievement Award
(Lothar Thiele, ETH Zurich, CH)

EDAA Outstanding Dissertation Award

DATE Fellow Award
(Anne Cirkel, Mentor US | Gerhard Fettweis, TU Dresden, DE)

IEEE Fellow Award
(Rolf Drechsler, University of Bremen/DFKI, DE)

IEEE/CEDA Outstanding Service Contribution Award 2014
(Gerhard Fettweis, TU Dresden, DE)

IEEE CS TTTC Outstanding Contribution Award
(Gerhard Fettweis, TU Dresden, DE)

2015 IEEE Frederik Philips Award
(Benedetto Vigna, STMicroelectronics, CH)

0910 **KEYNOTE ADDRESSES**

KEYNOTE ADDRESS
Geneviève Fioraso, secrétaire d'Etat chargée de l'Enseignement supérieur et de la Recherche (to be confirmed), FR

KEYNOTE ADDRESS
Günther H. Oettinger, European Commissioner for Digital Economy and Society, DE

KEYNOTE ADDRESS: ST TECHNOLOGIES FULLY ADDRESSING INTERNET OF THINGS APPLICATIONS FROM LP DIGITAL TO RF-CMOS, ENVM AND SENSORS
Jean Marc Chery, Chief Operating Officer of STMicroelectronics, FR

1030 **COFFEE BREAK IN EXHIBITION AREA**

TECHNICAL SESSIONS

2.1 Executive Panel - New Opportunities in the Internet of Things

Salle Oisans 1130 - 1300

Organiser: **Yervant Zorian,** Synopsys, US

Billions of devices connected to the internet is not too far from today's reality. Such an Internet of Things offers advanced connectivity between built-in sensors, field operation devices, and cloud systems, covering a variety of applications, including medical, home automation, energy, transportation, environmental monitoring, etc. This results in several new approaches and innovative methods that work together to enable the network of smart devices. Executives in this session will discuss the impact of IoT on the semiconductor industry and the new opportunities it may bring in designing today's Internet of Things.

1130 **PANELISTS**
Mojy Chian, CEO, Silicon Cloud International, US
Christoph Heer, Division VP, Head of Design System & IP, Intel, DE
Subramani Kengeri, VP, Global Design, GLOBALFOUNDRIES, US
Philipe Magarshack, EVP, Design Enablement, STMicroelectronics, FR
Remy Pottier, Director, IoT Strategy, ARM, GB
Yankin Tanurhan, VP, Processor & SOC Solutions, Synopsys, US

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

2.2 Adaptability for Low Power Computing

Belle-Etoile 1130 - 1300

Chair: **Patrick Knocke,** OFFIS, DE
Co-Chair: **Ruzica Jevtic,** Universidad Carlos III, ES

Run-time adaptability is increasingly exploited to improve efficiency of energy-scarce systems. This however inevitably brings serious increases in system complexity to optimally control the adaptability knobs and threatens system reliability. This session groups several approaches to achieve effective run-time reconfiguration at various levels of granularity. Adaptive strategies for multi-core task allocation, NV back-up storage, PV energy harvesting and multi-domain clock gating are presented.

1130 **CLOCK DOMAIN CROSSING AWARE SEQUENTIAL CLOCK GATING**
Mohit Kumar[1], Jianfeng Liu[2], Mi-Suk Hong[2], Kyungtae Do[2], JungYun Choi[2], Jaehong Park[2], Abhishek Ranjan[1], Manish Kumar[1] and Nikhil Tripathi[1]
[1]Calypto Design Systems, IN; [2]S.LSI, Samsung Electronics Co. Ltd., KR

1200 **AN ENERGY EFFICIENT BACKUP SCHEME WITH LOW INRUSH CURRENT FOR NONVOLATILE SRAM IN ENERGY HARVESTING SENSOR NODES**
Hehe Li[1], Yongpan Liu[1], Qinghang Zhao[1], Guangyu Sun[2], Chao Zhang[2], Yizi Gu[1], Rong Luo[1], Huazhong Yang[1], Meng-Fan Chang[3] and Xiao Sheng[1]
[1]Department of Electronic Engineering, Tsinghua University, CN; [2]Center for Energy-Efficient Computing and Applications, EECS, Peking University, CN; [3]Department of Electrical Engineering, National Tsing Hua University, TW

1230 **RACE TO IDLE OR NOT: BALANCING THE MEMORY SLEEP TIME WITH DVS FOR ENERGY MINIMIZATION**
Chenchen Fu[1], Minming Li[1] and Jason Xue[2]
[1]Department of Computer Science, City University of Hong Kong, HK; [2]City University of Hong Kong, HK

1245 **EVENT-DRIVEN AND SENSORLESS PHOTOVOLTAIC SYSTEM RECONFIGURATION FOR ELECTRIC VEHICLES**
Xue Lin[1], Yanzhi Wang[1], Massoud Pedram[1], Jaemin Kim[2] and Naehyuck Chang[3]
[1]University of Southern California, US; [2]Seoul National University, KR; [3]Korea Advanced Institute of Science and Technology, KR

IPS **IP1-1, IP1-2**

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

2.3 System Level Design Methods

Stendhal 1130 - 1300

Chair: **Yuichi Nakamura,** NEC, JP
Co-Chair: **Andreas Herkersdorf,** TU München, DE

This session tackles complex system-level design problems in state-of-the-art FPGA-based designs and schedulability-critical systems. The first talk proposes a runtime system assigning multi-clock domains in FPGA-based designs for minimizing the makespan of multiple tasks. The second talk studies novel multi-cycling optimization in high-level synthesis which is driven by software profiling. The third talk presents useful schedulability analysis and formulation on execution time bound for integrated modular avionic systems. Finally two IP talks propose an automated design flow for asynchronous dataflow networks to achieve better performance and area as well as feature localization for SystemC designs.

1130 **ONLINE BINDING OF APPLICATIONS TO MULTIPLE CLOCK DOMAINS IN SHARED FPGA-BASED SYSTEMS**
Farzad Samie[1], Lars Bauer[1], Chih-Ming Hsieh[2] and Joerg Henkel[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]Karlsruhe Institute of Technology, DE

1200 **PROFILING-DRIVEN MULTI-CYCLING IN FPGA HIGH-LEVEL SYNTHESIS**
Stefan Hadjis[1], Andrew Canis[1], Ryoya Sobue[2], Yuko Hara-Azumi[3], Hiroyuki Tomiyama[2] and Jason Anderson[1]
[1]University of Toronto, CA; [2]Ritsumeikan University, JP; [3]Tokyo Institute of Technology, JP

1230 **SCHEDULABILITY BOUND FOR INTEGRATED MODULAR AVIONICS PARTITIONS**
Jung-Eun Kim[1], Tarek Abdelzaher[2] and Lui Sha[1]
[1]Department of Computer Science, University of Illinois at Urbana-Champaign, US; [2]University of Illinois, US

IPS **IP1-3, IP1-4**

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

2.4 Automotive Systems and Smart Energy Systems

Chartreuse 1130 - 1300

Chair: **Bart Vermeulen,** NXP Semiconductors, NL
Co-Chair: **Geoff Merrett,** University of Southampton, GB

This session covers energy optimisation for embedded systems and emerging automotive systems and networks, including Ethernet and IP. To create effective Ethernet-enabled automotive networks, topics including service discovery, bridging and traffic shaping are addressed.

1130 **WORKLOAD UNCERTAINTY CHARACTERIZATION AND ADAPTIVE FREQUENCY SCALING FOR ENERGY MINIMIZATION OF EMBEDDED SYSTEMS**
Anup Das[1], Akash Kumar[2], Bharadwaj Veeravalli[2], Rishad Shafik[1], Geoff Merrett[1] and Bashir Al-Hashimi[3]
[1]University of Southampton, GB; [2]National University of Singapore, SG; [3]University of Southampton,

1200 **FORMAL ANALYSIS OF THE STARTUP DELAY OF SOME/IP SERVICE DISCOVERY**
Jan Reinke Seyler[1], Thilo Streichert[1], Michael Glaß[2], Nicolas Navet[3] and Jürgen Teich[2]
[1]Daimler AG, DE; [2]Friedrich-Alexander-Universität Erlangen-Nürnberg, DE; [3]Université du Luxembourg, LU

1230 **ANALYSIS OF ETHERNET-SWITCH TRAFFIC SHAPERS FOR IN-VEHICLE NETWORKING APPLICATIONS**
Sivakumar Thangamuthu[1], Nicola Concer[2], Pieter Cuijpers[3] and Johan Lukkien[3]
[1]NXP Semiconductors, IN; [2]NXP Semiconductors, NL; [3]Technische Universiteit Eindhoven, NL

1245 **REAL-TIME CAPABLE CAN TO AVB ETHERNET GATEWAY USING FRAME AGGREGATION AND SCHEDULING**
Christian Herber, Andre Richter, Thomas Wild and Andreas Herkersdorf, Technische Universität München, DE

IPS **IP1-5, IP1-6**

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

2.5 Power of Assertions

Meije 1130 - 1300

Chair: **Franco Fummi,** University of Verona, IT
Co-Chair: **Pablo Sanchez,** University of Cantabria, ES

Assertions play a critical role in verification of hardware systems. This session is focusing on new applications of assertions in a wide variety of validation scenarios such as faster bug localization and post-silicon validation as well as reusing properties across abstraction levels.

1130 **AUTOMATIC EXTRACTION OF ASSERTIONS FROM EXECUTION TRACES OF BEHAVIOURAL MODELS**
Alessandro Danese, Tara Ghasempouri and Graziano Pravadelli, University of Verona, IT

1200 **A METHODOLOGY FOR AUTOMATED DESIGN OF EMBEDDED BIT-FLIPS DETECTORS IN POST-SILICON VALIDATION**
Pouya Taatizadeh and Nicola Nicolici, McMaster University, CA

1230 **DATA MINING DIAGNOSTICS AND BUG MRIS FOR HW BUG LOCALIZATION**
Monica Farkash[1], Bryan Hickerson[2] and Balavinayagam Samynathan[1]
[1]University of Texas at Austin, US; [2]IBM, US

1245 **RTL PROPERTY ABSTRACTION FOR TLM ASSERTION-BASED VERIFICATION**
Nicola Bombieri[1], Riccardo Filippozzi[1], Graziano Pravadelli[1] and Francesco Stefanni[2]
[1]University of Verona, IT; [2]EDALab s.r.l., IT

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

2.6 Design and Analysis of Dependable Systems

Bayard 1130 - 1300

Chair: **Arne Hamann,** Robert Bosch GmbH, DE
Co-Chair: **Viacheslav Izosimov,** Semcon/KTH, SE

This section introduces new methods for uncertainty-aware reliability analysis and soft error vulnerability estimation as well as techniques for error recovery in safety-critical systems and security attacks through the JTAG port

1130 **LOW-COST CHECKPOINTING IN AUTOMOTIVE SAFETY-RELEVANT SYSTEMS**
Carles Hernandez and Jaume Abella, Barcelona Supercomputing Center (BSC-CNS), ES

1200 **UNCERTAINTY-AWARE RELIABILITY ANALYSIS AND OPTIMIZATION**
Faramarz Khosravi, Malte Müller, Michael Glaß and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1230 **EFFICIENT SOFT ERROR VULNERABILITY ESTIMATION OF COMPLEX DESIGNS**
Shahrzad Mirkhani[1], Subhasish Mitra[2], Chen-Yong Cher[3] and Jacob Abraham[4]
[1]University of Texas at Austin, US; [2]Stanford University, US; [3]IBM Research, US; [4]University of Texas, US

1245 **DETECTION OF ILLEGITIMATE ACCESS TO JTAG VIA STATISTICAL LEARNING IN CHIP**
Xuanle Ren[1], Vítor Grade Tavares[2] and Shawn Blanton[1]
[1]Carnegie Mellon University, US; [2]Faculdade de Engenharia da Universidade do Porto, PT

IPS **IP1-8, IP1-9**

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

2.7 Compilation and Code Transformations for Reconfigurable Computing

Les Bans 1130 - 1300

Chair: **Dirk Stroobandt,** University of Ghent, BE
Co-Chair: **Marco Platzner,** University of Paderborn, DE

This session presents techniques for efficient compilation to CGRAs and a code transformation approach to enhance embedded system security.

1130 **JOINT AFFINE TRANSFORMATION AND LOOP PIPELINING FOR MAPPING NESTED LOOP ON CGRA**
Shouyi Yin[1], Dajiang Liu[1], Leibo Liu[2], Shaojun Wei[1] and Yike Guo[3]
[1]Tsinghua University, CN; [2]Institute of Microelectronics and The National Lab for Information Science and Technology, Tsinghua University, CN; [3]Imperial College, London, GB

1200 **PATH SELECTION BASED ACCELERATION OF CONDITIONALS IN CGRAS**
Shri Hari Rajendran Radhika, Aviral Shrivastava and Mahdi Hamzeh, Arizona State University, US

1230 **HARDWARE-ASSISTED CODE OBFUSCATION FOR FPGA SOFT MICROPROCESSORS**
Meha Kainth, Lekshmi Krishnan, Chaitra Narayana, Sandesh Virupaksha and Russell Tessier, University of Massachusetts, US

IPS **IP1-10, IP1-11, IP1-12, IP1-13**

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

TUESDAY 10 MARCH, 2015

DATE15 March 9 – 13, 2015, Grenoble, France TUE

2.8 Facilities for Design and Fabrication for FD-SOI IC

Lesdiguières 1130 - 1300

Organiser: **Ahmed Jerraya,** CEA-Leti, FR
Moderator: **Carlo Reita,** CEA-Leti, FR
Panelists: **Gerd Teepe,** GLOBALFOUNDRIES, DE
Patrick Blouet, STMicroelectronics, FR
Olivier Thomas, CEA-Leti, FR

FD-SOI technology enables low cost and energy efficient designs best suited for today consumer, IoT and automotive applications, in continuity with traditional planar technologies simpler to design and manufacture with. The talks will illustrate the availability of a full FD-SOI technology ecosystem, encompassing IC fabrication, IP availability and design experiences.

1130 **FD-SOI TECHNOLOGY ROADMAP**
Carlo Reita, CEA-Leti, FR

1145 **FOUNDRY SERVICES FOR FD-SOI**
Gerd Teepe, GLOBALFOUNDRIES, DE

1200 **FD-SOI DESIGN AND IP ECOSYSTEM**
Patrick Blouet, STMicroelectronics, FR

1215 **INDUSTRIAL FD-SOI MPW AND GRENOBLE IC DESIGN CENTER**
Olivier Thomas, CEA-Leti, FR

1230 **DISCUSSION**

1300 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote session from 1320 – 1420 (Room Oisans) sponsored by Mentor Graphics

3.0 LUNCH TIME KEYNOTE SESSION: "How micro-electronic will change your life style" sponsored by Mentor Graphics

Oisans 1320 - 1420

Organiser: **Mentor Graphics**
Moderator: **Jean-Marie Saint-Paul,** Mentor Graphics, FR

Microelectronics is opening new vistas in our lives by changing the way we interact with our environment. Speech recognition, Drones and Robots are not only advanced research topics, these are surrounding our daily activities, sharing our lives and may induce a much larger transformation of our life style than we could have imagined 10 years ago. This session will bring together high profile products and vision to show the ongoing transformation.

1320 **NEW LIFE STYLES BEYOND YOUR DREAMS**
Thierry Collette, CEA-Leti, FR

1330 **DRONES THAT FLY FOR YOU**
Nicolas Besnard, Parrot, FR

1350 **ROBOTS THAT LIVE WITH YOU**
Rodolphe Gelin, Aldebaran, FR

1410 **QUESTIONS FROM THE AUDIENCE**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.1 Executive Panel - Extending Moore's Law & Heterogeneous Integration

Salle Oisans 1430 - 1600

Organiser: **Yervant Zorian,** Synopsys, US

Systemic scaling in today's new applications is dramatically impacting the semiconductor industry. As a result, certain applications are moving to new advanced semiconductor nodes and others are adopting heterogeneous integration using multi-die modules. In addition to the technical challenges in each case, these solutions significantly affect the dependency between ecosystem players necessitating smooth interdependency between them. The executives in this session will discuss the solutions in the semiconductor industry and their impact on the eco system players.

1430 **PANELISTS**
Ivo Bolsens, Senior VP & CTO, Xilinx, US
Antun Domic, Executive VP, Design Group, Synopsys, US
Rudy Lauwereins, VP, IMEC, BE
Maria Merced, President, TSMC Europe, NL

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.2 Passive Implementation Attacks and Countermeasures

Belle-Etoile 1430 - 1600

Chair: **Francois-Xavier Standaert,** UCL, BE
Co-Chair: **Francesco Regazzoni,** AlaRI, CH

Passive implementation attacks are a major security threat for embedded systems. This session focuses on improving side-channel analysis considering reliable key extraction, information leakage of static power consumption, and processor instructions. It also presents a monitor to defeat write-back attacks on caches.

1430 **RELIABLE INFORMATION EXTRACTION FOR SINGLE TRACE ATTACKS**
Valentina Banciu, Elisabeth Oswald and Carolyn Whitnall, University of Bristol, GB

1500 **SCANDALEE: A SIDE-CHANNEL-BASED DISASSEMBLER USING LOCAL ELECTROMAGNETIC EMANATIONS**
Daehyun Strobel, Florian Bache, David Oswald, Falk Schellenberg and Christof Paar, Horst Görtz Institute for IT-Security, Ruhr-University Bochum, DE

1530 **SIDE-CHANNEL ATTACKS FROM STATIC POWER: WHEN SHOULD WE CARE?**
Santos Merino del Pozo[1], Francois-Xavier Standaert[1], Dina Kamel[1] and Amir Moradi[2]
[1]UCL Crypto Group, BE; [2]Ruhr University Bochum, DE

1545 **EXTRAX: SECURITY EXTENSION TO EXTRACT CACHE RESIDENT INFORMATION FOR SNOOP-BASED EXTERNAL MONITORS**
Jinyong Lee[1], Yongje Lee[2], Hyungon Moon[1], Ingoo Heo[1] and Yunheung Paek[1]
[1]Seoul National University, KR; [2]Seoul National University, Samsung Electronics Co., Ltd., KR

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.3 Loop Acceleration

Stendhal 1430 - 1600

Chair: **Jürgen Teich,** FAU Erlangen, DE
Co-Chair: **Benjamin Schafer,** Hong Kong Polytechnic University, HK

This session reveals novel loop optimization techniques in high-level synthesis for resolving area overhead and communication bottlenecks in nested loops and/or multidimensional arrays. The first talk leverages loop-array dependencies for loop partitioning to reduce the dimension of the design space in order to ease the design complexity. The second talk quantifies a relationship between loop unrolling and partitioning, based on which area reduction methods are proposed by controlling the degree of loop unrolling. The third talk then resolves communication bottlenecks in embedded accelerators through inter-tile data reuse on loop optimizations.

1430 **EXPLOITING LOOP-ARRAY DEPENDENCIES TO ACCELERATE THE DESIGN SPACE EXPLORATION WITH HIGH LEVEL SYNTHESIS**
Nam Khanh Pham[1], Amit Kumar Singh[2], Akash Kumar[3] and Mi Mi Aung Khin[4]
[1]ECE Department, National University of Singapore, SG; [2]University of York, GB; [3]National University of Singapore, SG; [4]Data Storage Institute (DSI), A*STAR, Singapore., SG

1500 **INTERPLAY OF LOOP UNROLLING AND MULTIDIMENSIONAL MEMORY PARTITIONING IN HLS**
Alessandro Cilardo and Luca Gallo, University of Naples Federico II, IT

1530 **INTER-TILE REUSE OPTIMIZATION APPLIED TO BANDWIDTH CONSTRAINED EMBEDDED ACCELERATORS**
Maurice Peemen, Bart Mesman and Henk Corporaal, Eindhoven University of Technology, NL

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.4 Tackling Memory Walls with Emerging Architectures and Technologies

Chartreuse 1430 - 1600

Chair: **Akash Kumar,** NUS, SG
Co-Chair: **Cristina Silvano,** Politecnico di Milano, IT

This session focuses on various aspects of memory system design including non-volatile reconfigurable cache design, cache directory design, shared DRAM access, and writeback policies for stacked-die caches.

1430 **SELECTDIRECTORY: A SELECTIVE DIRECTORY FOR CACHE COHERENCE IN MANY-CORE ARCHITECTURES**
Yuan Yao[1], Guanhua Wang[2], Zhiguo Ge[3], Tulika Mitra[2], Wenzhi Chen[1] and Naxin Zhang[3]
[1]Zhejiang University, CN; [2]National University of Singapore, SG; [3]Huawei, SG

1500 **DYRECTAPE: A DYNAMICALLY RECONFIGURABLE CACHE USING DOMAIN WALL MEMORY TAPES**
Ashish Ranjan[1], Shankar Ganesh Ramasubramanian[1], Rangharajan Venkatesan[2], Vijay Pai[1], Kaushik Roy[1] and Anand Raghunathan[1]
[1]Purdue University, US; [2]NVIDIA Corporation, US

1530 **COOPERATIVELY MANAGING DYNAMIC WRITEBACK AND INSERTION POLICIES IN A LAST-LEVEL DRAM CACHE**
Shouyi Yin[1], Jiakun Li[1], Leibo Liu[2], Shaojun Wei[1] and Yike Guo[3]
[1]Tsinghua University, CN; [2]Institute of Microelectronics and The National Lab for Information Science and Technology, Tsinghua University, CN; [3]Imperial College, London, GB

1545 **A GENERIC, SCALABLE AND GLOBALLY ARBITRATED MEMORY TREE FOR SHARED DRAM ACCESS IN REAL-TIME SYSTEMS**
Manil Dev Gomony[1], Jamie Garside[2], Benny Akesson[3], Neil Audsley[2] and Kees Goossens[1]
[1]Eindhoven University of Technology, NL; [2]University of York, GB; [3]Czech Technical University in Prague, CZ

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.5 Breaking Simulation Boundaries

Meije 1430 - 1600

Chair: **Elena Ioana Vatajelu,** Politecnico di Torino, IT
Co-Chair: **Florian Letombe,** Synopsys, FR

Faster, faster, faster .... that's all you expect when you are simulating your designs. This session takes you through a journey of super fast simulation techniques at different abstraction levels.

1430 VARIATION-AWARE EVALUATION OF MPSOC TASK ALLOCATION AND SCHEDULING STRATEGIES USING STATISTICAL MODEL CHECKING
Mingsong Chen[1], Daian Yue[1], Xiaoke Qin[2], Xin Fu[3] and Prabhat Mishra[2]
[1]East China Normal University, CN; [2]University of Florida, US; [3]University of Houston, US

1500 A FAST PARALLEL SPARSE SOLVER FOR SPICE-BASED CIRCUIT SIMULATORS
Xiaoming Chen, Yu Wang and Huazhong Yang, Tsinghua University, CN

1530 MRP: MIX REAL CORES AND PSEUDO CORES FOR FPGA-BASED CHIP-MULTIPROCESSOR SIMULATION
Xinke Chen[1], Guangfei Zhang[2], Huandong Wang[3], Ruiyang Wu[1], Peng Wu[1] and Longbing Zhang[1]
[1]Institute of Computing Technology, CAS, CN; [2]Shannon Laboratory, Huawei Technologies Co., Ltd, CN; [3]Loongson Technology Corporation Limited, CN

1545 SOURCE LEVEL PERFORMANCE SIMULATION OF GPU CORES
Christoph Gerum[1], Oliver Bringmann[2] and Wolfgang Rosenstiel[1]
[1]University of Tuebingen, DE; [2]University of Tuebingen / FZI, DE

IPS IP1-14, IP1-15, IP1-16

1600 COFFEE BREAK IN EXHIBITION AREA

3.6 Hot Topic - Memristor based Computation-in-Memory Architecture for Data-Intensive Applications

Bayard 1430 - 1600

Organisers: **Said Hamdioui,** TU Delft, NL
Koen Bertels, TU Delft, NL

In today's data-intensive applications (known as Big Data problems), such as healthcare (e.g., use of genetic information to diagnose and treat diseases), social media, engineering (e.g. large scientific experiments), the primary goal is to increase the understanding of processes in order to extract so much potential and highly useful information hidden in the huge volume of data, which in turn can be used to increase the productivity. As the speed of information growth exceeds Moore's Law at the beginning of this century, excessive data is making great troubles to human beings. At the same time, Big Data arises with many challenges, such as data capture, data storage, data analysis and data visualization. Performing data analysis within economically affordable time and energy is the pillar to solve big data problems, and therefore extract extremely valuable information. The increase of the data size has already surpassed the capabilities of today's computation architectures which suffer from communication bottleneck due to limited bandwidth. For instance, the transfer of 1 petabyes data at a rate of 1000MB/second will cost 12.5 days! Communication and memory access does not only kill the performance, but also energy/power (more than between 70% and 90% such applications). Even the CMOS technology used to implement today's architectures contributes to such power due to the higher leakage; not to mention the limited scalability (as it is becoming very costly), reduced reliability (as it degrades faster), etc. In conclusion, today's CMOS based architecture are not able to provide the computation capability needed for data-intensive applications. New architectures based new technologies are therefore needed. This Hot-Topic Session will address the concept of "Computing-in-memory (CIM)" and discuss a new Memristor Based Architecture Paradigm for Data-Intensive applications, as an alternative architecture. The concept is based on performing the storage and computation in the same crossbar topology (non Von- Neumann architecture) where the key device is the non-volatile resistive switching element (memristor). CIM architecture is able significantly push the "memory wall", while the memristor device is able to reduce the static power to practically zero.

1430 DATA-INTENSIVE APPLICATIONS- A MAJOR CHALLENGE AHEAD
Jan van Lunteren, IBM Research, CH

1500 CIM ARCHITECTURE- BEYOND VON NEUMANN
Koen Bertels[1] and Henk Coorporal[2]
[1]Delft University of Technology, NL; [2]Eindhoven University of Technology, NL

1530 MEMRISTIVE DEVICES - THE KEY ENABLER FOR CIM ARCHITECTURE IMPLEMENTATION
Eike Linn, RWTH Aachen University, DE

1600 COFFEE BREAK IN EXHIBITION AREA

3.7 Model-based Analysis and Verification

Les Bans 1430 - 1600

Chair: **Saddek Bensalem,** Université Joseph Fourier, FR
Co-Chair: **Linh Thi Xuan Phan,** University of Pennsylvania, US

This session focuses on the analysis and verification in model-based design of embedded systems. It has four regular papers : The first paper presents a delay analysis method for a general graph based workload model. The second one presents a new formal approach to verifying Interrupt-driven software based on symbolic execution. The third one proposes a method for model-based verification (and arguably implementation) of real-time systems, where the original model is expressed as a network of UPPAAL timed automata (PIM). The fourth one presents a generic method to automatically generate a symbolic executor for a given hardware architecture specified by some Architecture Description Language, which is used to verify program properties regarding the binary code level. In this session we have also an IP paper, which presents a technique for estimating non-functional requirements using a Knowledge Discovery in Databases (KDD) approach.

1430 DELAY ANALYSIS OF STRUCTURAL REAL-TIME WORKLOAD
Nan Guan[1], Yue Tang[2], Yang Wang[2] and Wang Yi[3]
[1]Uppsala University, SE; [2]Northeastern University, CN; [3]Uppsala University, CN

1500 EFFECTIVE VERIFICATION OF LOW-LEVEL SOFTWARE WITH NESTED INTERRUPTS
Daniel Kroening[1], Lihao Liang[1], Tom Melham[1], Peter Schrammel[1] and Michael Tautschnig[2]
[1]University of Oxford, GB; [2]Queen Mary, University of London, GB

1530 PLATFORM-SPECIFIC TIMING VERIFICATION FRAMEWORK IN MODEL-BASED IMPLEMENTATION
Baek Gyu Kim, Lu Feng, Linh T.X. Phan, Oleg Sokolsky and Insup Lee, University of Pennsylvania, US

1545 ARCHITECTURE DESCRIPTION LANGUAGE BASED RETARGETABLE SYMBOLIC EXECUTION
Andreas Ibing, TU München, DE

1600 COFFEE BREAK IN EXHIBITION AREA

3.8 Hot Topic - Design Methodologies for a Cyber-Physical Systems Approach to Personalized Medicine-on-a-Chip: Challenges and Opportunities

Salle Lesdiguières 1430 - 1600

Organiser: **Krishnendu Chakrabarty**, Duke University, US
Chair: **Paul Pop**, Technical University of Denmark, DK
Co-Chair: **Mohammad Abdullah Al Faruque**, University of California Irvine, US

Modern stressful and sedentary lifestyles coupled with inadequate, irregular and inappropriate sleep patterns and diet have contributed not only to increased prevalence of chronic diseases but also to increased healthcare costs. To address these emerging clinical and healthcare challenges, in this special session, we advocate for a cross-disciplinary approach to cyber-physical systems design (CPS) aiming at seamlessly and safely integrate sensing, computation, communication, control and actuation for developing new technology for personalized and precise medicine.

1430 **ERROR RECOVERY IN DIGITAL MICROFLUIDICS FOR PERSONALIZED MEDICINE**
Mohamed Ibrahim and Krishnendu Chakrabarty, Duke University, US

1500 **A CYBER-PHYSICAL SYSTEMS APPROACH TO PERSONALIZED MEDICINE: CHALLENGES AND OPPORTUNITIES FOR NOC-BASED MULTICORE PLATFORMS**
Paul Bogdan, University of Southern California, US

1530 **ON-CHIP NETWORK-ENABLED MANY-CORE ARCHITECTURES FOR COMPUTATIONAL BIOLOGY APPLICATIONS**
Turbo Majumder[1], Partha Pande[2] and Ananth Kalyanaraman[2]
[1]Indian Institute of Technology Delhi, IN; [2]Washington State University, US

1600 **COFFEE BREAK IN EXHIBITION AREA**

IP1 Interactive Presentations, sponsored by Cadence Academic Network

1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP1-1 **HIGH-RESOLUTION ONLINE POWER MONITORING FOR MODERN MICROPROCESSORS**
Fabian Oboril, Jos Ewert and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

IP1-2 **REDUCING ENERGY CONSUMPTION IN MICROCONTROLLER-BASED PLATFORMS WITH LOW DESIGN MARGIN CO-PROCESSORS**
Andres Gomez[1], Christian Pinto[2], Andrea Bartolini[3], Davide Rossi[2], Hamed Fatemi[4], Jose Pineda de Gyvez[4] and Luca Benini[3]
[1]Swiss Federal Institute of Technology in Zurich (ETHZ), CH; [2]Università di Bologna, IT; [3]Università di Bologna / Swiss Federal Institute of Technology in Zurich (ETHZ), IT; [4]NXP Semiconductors, NL

IP1-3 **DE-ELASTISATION: FROM ASYNCHRONOUS DATAFLOWS TO SYNCHRONOUS CIRCUITS**
Mahdi Jelodari Mamaghani, Jim Garside and Doug Edwards, University of Manchester, GB

IP1-4 **AUTOMATED FEATURE LOCALIZATION FOR DYNAMICALLY GENERATED SYSTEMC DESIGNS**
Jannis Stoppe[1], Robert Wille[1] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen/DFKI GmbH, DE

TUESDAY 10 MARCH, 2015

DATE15
March 9 – 13, 2015, Grenoble, France
TUE

IP1-5 **INDUCTOR OPTIMIZATION FOR ACTIVE CELL BALANCING USING GEOMETRIC PROGRAMMING**
Matthias Kauer[1], Swaminathan Narayanaswamy[1], Martin Lukasiewycz[1], Sebastian Steinhorst[1] and Samarjit Chakraborty[2]
[1]TUM CREATE, SG; [2]TU Munich, DE

IP1-6 **LIGHTWEIGHT AUTHENTICATION FOR SECURE AUTOMOTIVE NETWORKS**
Philipp Mundhenk[1], Sebastian Steinhorst[1], Martin Lukasiewycz[1], Suhaib A. Fahmy[2] and Samarjit Chakraborty[3]
[1]TUM CREATE, SG; [2]School of Computer Engineering, Nanyang Technological University, SG; [3]TU Munich, DE

IP1-7 **MINIMIZING THE NUMBER OF PROCESS CORNER SIMULATIONS DURING DESIGN VERIFICATION**
Michael Shoniker, Bruce Cockburn, Jie Han and Witold Pedrycz, University of Alberta, CA

IP1-8 **AN APPROXIMATE VOTING SCHEME FOR RELIABLE COMPUTING**
Ke Chen[1], Jie Han[2] and Fabrizio Lombardi[1]
[1]Northeastern University, US; [2]University of Alberta, CA

IP1-9 **FLINT: LAYOUT-ORIENTED FPGA-BASED METHODOLOGY FOR FAULT TOLERANT ASIC DESIGN**
Rochus Nowosielski, Lukas Gerlach, Stephan Bieband, Guillermo Paya-Vaya and Holger Blume, Leibniz Universität Hannover, Institute of Microelectronic Systems, DE

IP1-10 **A UNIFIED HARDWARE/SOFTWARE MPSOC SYSTEM CONSTRUCTION AND RUN-TIME FRAMEWORK**
Sam Skalicky[1], Andrew Schmidt[2], Matthew French[2] and Sonia Lopez[1]
[1]Rochester Institute of Technology, US; [2]USC/ISI, US

IP1-11 **(AS)^2: ACCELERATOR SYNTHESIS USING ALGORITHMIC SKELETONS FOR RAPID DESIGN SPACE EXPLORATION**
Shakith Fernando[1], Mark Wijtvliet[1], Cedric Nugteren[1], Akash Kumar[2] and Henk Corporaal[3]
[1]Eindhoven University of Technology, NL; [2]National University of Singapore, SG; [3]TU/e (Eindhoven University of Technology), NL

IP1-12 **ASSISTED GENERATION OF FRAME CONDITIONS FOR FORMAL MODELS**
Philipp Niemann, Frank Hilken, Martin Gogolla and Robert Wille, University of Bremen, DE

IP1-13 **TOWARDS A META-LANGUAGE FOR THE CONCURRENCY CONCERN IN DSLS**
Julien Deantoni[1], Papa Issa Diallo[2], Ciprian Teodorov[2], Joel Champeau[2] and Benoit Combemale[3]
[1]I3S, University of Nice Sophia Antipolis, FR; [2]Lab-STICC - ENSTA Bretagne, FR; [3]IRISA, Universty of Rennes[1], FR

IP1-14 **FAST AND ACCURATE BRANCH PREDICTOR SIMULATION**
Antoine Faravelon, Nicolas Fournel and Frédéric Pétrot, TIMA Laboratory, Université de Grenoble-Alpes/CNRS, FR

IP1-15 **COMPARATIVE STUDY OF TEST GENERATION METHODS FOR SIMULATION ACCELERATORS**
Wisam Kadry[1], Dimtry Krestyashyn[1], Arkadiy Morgenshtein[1], Amir Nahir[1], Vitali Sokhin[1], Jae Cheol Son[2], Wookyeong Jeong[2], Sung-Boem Park[2] and Jin Sung Park[2]
[1]IBM Research - Haifa, IL; [2]Samsung, KR

IP1-16 **USING STRUCTURAL RELATIONS FOR CHECKING COMBINATIONALITY OF CYCLIC CIRCUITS**
Wan-Chen Weng[1], Yung-Chih Chen[2], Jui-Hung Chen[1], Ching-Yi Huang[1] and Chun-Yao Wang[1]
[1]National Tsing Hua University, TW; [2]Yuan Ze University, TW

IP1-17 **NFRS EARLY ESTIMATION THROUGH SOFTWARE METRICS**
Andrws Vieira[1], Pedro Faustini[1], Luigi Carro[2] and Erika Cota[1]
[1]Federal University of Rio Grande do Sul (UFRGS), BR; [2]Federal University of Rio Grande do Sul (UFRGS),

4.1 Executive Panel - Trends and Challenges in Today's Automotive Semiconductors

Salle Oisans 1700 - 1830

Organiser: **Yervant Zorian,** Synopsys, US

While the new chips in the automotive industry keep growing both in functionality and numbers, the complexity level and robustness requirements remain crucial, as always, given their safety critical application. The speakers in this executive session will address the current trends and challenges in the automotive semiconductor industry.

1700 **PANELISTS**
Andreas Brüning, Director Technology Office, ZMDI, DE
Maurizio Peri, General Manager, Automotive R&D, STMicroelectronics, IT
Jean-Marie Saint-Paul, Technical Director, Mentor Graphics, FR
Frank Schirrmeister, Group Director, Cadence Design Systems, US

4.2 Implementation and Verification of Security Components

Belle-Etoile 1700 - 1830

Chair: **Assia Tria,** CEA, FR
Co-Chair: **Wieland Fischer,** Infineon Technologies AG, DE

System designers need secure building blocks for robust security devices. This session presents novel implementation and verification strategies for hardware circuits, post-quantum cryptography schemes and true random number generators.

1700 **PRIVACY-PRESERVING FUNCTIONAL IP VERIFICATION UTILIZING FULLY HOMOMORPHIC ENCRYPTION**
Charalambos Konstantinou[1] and Michail Maniatakos[2]
[1]New York University Polytechnic School of Engineering, US; [2]New York University Abu Dhabi, AE

1730 **EFFICIENT SOFTWARE IMPLEMENTATION OF RING-LWE ENCRYPTION**
Ruan de Clercq, Sujoy Sinha Roy, Frederik Vercauteren and Ingrid Verbauwhede, KU Leuven - COSIC, BE

1800 **EMBEDDED HW/SW PLATFORM FOR ON-THE-FLY TESTING OF TRUE RANDOM NUMBER GENERATORS**
Bohan Yang[1], Vladimir Rozic[1], Nele Mentens[1], Wim Dehaene[2] and Ingrid Verbauwhede[3]
[1]ESAT/COSIC and iMinds, KU Leuven, BE; [2]ESAT-MICAS, KU Leuven, BE; [3]KU Leuven - COSIC, BE

4.3 Multi-/Manycore Scheduling

Stendhal 1700 - 1830

Chair: **Luciano Lavagno,** Politechnico di Torino, IT
Co-Chair: **Aviral Shrivastava,** Arrizona State University, US

This session tackles various issues in realistic, complex task scheduling/assignment methods in 2D and 3D multi/many-core systems. The first talk introduces an intra/inter-cores switching method in multi-core scheduling problem for efficient power saving under throughput constraint. The second talk studies thermal-pattern-aware task assignment for 3D multi-core processors, where hotspot is a critical issue, for improving reliability and lifetime. The third talk effectively combines logic solver and background theory solver to synthesize satisfiability modulo theories (SMT)-based systems.

1700 **AN ONLINE THERMAL-CONSTRAINED TASK SCHEDULER FOR 3D MULTI-CORE PROCESSORS**
Chien-Hui Liao[1], Hung-Pin Wen[1] and Krishnendu Chakrabarty[2]
[1]National Chiao Tung University, TW; [2]Duke University, US

1730 **A SYMBOLIC SYSTEM SYNTHESIS APPROACH FOR HARD REAL-TIME SYSTEMS BASED ON COORDINATED SMT-SOLVING**
Alexander Biewer[1], Benjamin Andres[2], Jens Gladigau[1], Torsten Schaub[2] and Christian Haubelt[3]
[1]Robert Bosch GmbH, DE; [2]University of Potsdam, DE; [3]University of Rostock, DE

1800 **E-PIPELINE: ELASTIC HARDWARE/SOFTWARE PIPELINES ON A MANY-CORE FABRIC**
Xi Zhang[1], Haris Javaid[1], Muhammad Shafique[2], Jorgen Peddersen[1], Joerg Henkel[2] and Sri Parameswaran[1]
[1]University of New South Wales, AU; [2]Karlsruhe Institute of Technology (KIT), DE

4.4 Exploring Reliability and Efficiency Tradeoffs at the Architectural Level

Chartreuse 1700 - 1830

Chair: **Todd Austin,** University of Michigan, US
Co-Chair: **Gunar Schirner,** Northeastern University, US

This session targets architectural solutions for energy-efficient and reliable memories and processors.

1700 **SOFT-ERROR RELIABILITY AND POWER CO-OPTIMIZATION FOR GPGPUS REGISTER FILE USING RESISTIVE MEMORY**
Jingweijia Tan[1], Zhi Li[2] and Xin Fu[1]
[1]University of Houston, US; [2]University of Kansas, US

1730 **ENERGY-EFFICIENT CACHE DESIGN IN EMERGING MOBILE PLATFORMS: THE IMPLICATIONS AND OPTIMIZATIONS**
Kaige Yan and Xin Fu, University of Houston, US

1800 **EXPLOITING DYNAMIC TIMING MARGINS IN MICROPROCESSORS FOR FREQUENCY-OVER-SCALING WITH INSTRUCTION-BASED CLOCK ADJUSTMENT**
Jeremy Constantin[1], Lai Wang[2], Georgios Karakonstantis[3], Anupam Chattopadhyay[2] and Andreas Burg[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]RWTH Aachen, DE; [3]Queen's University, GB

1815 **VARIABILITY-AWARE DARK SILICON MANAGEMENT IN ON-CHIP MANY-CORE SYSTEMS**
Muhammad Shafique[1], Dennis Gnad[1], Siddharth Garg[2] and Joerg Henkel[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]University of Waterloo, CA

4.5 Industrial Test and Validation Experiments

Meije 1700 - 1830

Chair: **Dan Alexandescu,** iRoC, FR
Co-Chair: **Emmanuel Simeu,** TIMA, FR

This session introduces test and validation industrial experiments. Each experiment addresses the challenges of system validation and test and shows lessons learned from industry

1700 **SYSTEMATIC APPLICATION OF THE ISO 26262 ON A SEOOC SUPPORT BY APPLYING A SYSTEMATIC REUSE APPROACH**
Alejandra Ruiz[1], Alberto Melzi[2] and Tim Kelly[3]
[1]TECNALIA, ES; [2]Centro Ricerche FIAT, IT; [3]University of York, GB

1715 **TIMING ANALYSIS OF AN AVIONICS CASE STUDY ON COMPLEX HARDWARE/SOFTWARE PLATFORMS**
Franck Wartel[1], Leonidas Kosmidis[2], Adriana Gogonel[3], Andrea Baldovin[4], Zoe Stephenson[5], Benoit Triquet[1], Eduardo Quinones[6], Code Lo[3], Enrico Mezzetti[7], Ian Broster[5], Jaume Abella[8], Liliana Cucu-Grosjean[3], Tullio Vardanega[4] and Francisco Cazorla[9]
[1]Airbus, FR; [2]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; [3]INRIA, FR; [4]University of Padova, IT; [5]Rapita Systems, Ltd., GB; [6]Barcelona Supercomputing Center, ES; [7]University of Padua, IT; [8]Barcelona Supercomputing Center (BSC-CNS), ES; [9]Barcelona Supercomputing Center and IIIA-CSIC, ES

1730 **SILICON PROOF OF THE INTELLIGENT ANALOG IP DESIGN FLOW FOR FLEXIBLE AUTOMOTIVE COMPONENTS**
Torsten Reich, H. D. Benjamin Prautsch, Uwe Eichler and René Buhl, Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS, DE

1745 **FAST OPTICAL SIMULATION FROM A REDUCED SET OF IMPULSE RESPONSES USING SYSTEMC AMS**
Fabien Teysseyre[1], David Navarro[1], Ian O'Connor[1], Francesco Cascio[2], Fabio Cenni[2] and Olivier Guillaume[2]
[1]École Centrale de Lyon, FR; [2]STMicroelectronic, FR

1800 **DESIGNER-LEVEL VERIFICATION -- AN INDUSTRIAL EXPERIENCE STORY**
Stephen Bergman[1], Gabor Bobok[1], Walter Kowalski[1], Shlomit Koyfman[2], Shiri Moran[2], Ziv Nevo[2], Avigail Orni[2], Viresh Paruthi[1], Wolfgang Roesner[1], Gil Shurek[2] and Vasantha Vuyyuru[1]
[1]IBM, US; [2]IBM, IL

1815 **MINIMUM CURRENT CONSUMPTION TRANSITION TIME OPTIMIZATION METHODOLOGY FOR LOW POWER CTS**
Vibhu Sharma, NXP Research, NL

4.6 Online Testing and Reliable Memories

Bayard 1700 - 1830

Chair: **Mihalis Psarakis,** University of Piraeus, GR
Co-Chair: **Cristiana Bolchini,** Politecnico di Milano, IT

Temperature- and power-aware solutions are proposed for self- and on-line testing, together with innovative fault detection and reconfiguration schemes for caches and emerging memory technologies

1700 **A DEFECT-AWARE RECONFIGURABLE CACHE ARCHITECTURE FOR LOW-VCCMIN DVFS-ENABLED SYSTEMS**
Michail Mavropoulos, Georgios Keramidas and Dimitris Nikolos, University of Patras, GR

1730 **TEMPERATURE-AWARE SOFTWARE-BASED SELF-TESTING FOR DELAY FAULTS**
Ying Zhang[1], Zebo Peng[2], Jianhui Jiang[3], Huawei Li[4] and Masahiro Fujita[5]
[1]Tongji University, Shanghai, China, CN; [2]Embedded Systems Lab, Linköping University, SE; [3]School of Software Engineering, Tongji University, CN; [4]Institute of Computing Technology, Chinese Academy of Sciences, CN; [5]VLSI Design and Education Center, University of Tokyo, JP

1800 **OPERATIONAL FAULT DETECTION AND MONITORING OF A MEMRISTOR-BASED LUT**
Nandha kumar Thulasiraman[1], Haider A.F. Almurib[1] and Fabrizio Lombardi[2]
[1]The University of Nottingham, MY; [2]Northeastern University, US

1815 **POWER-AWARE ONLINE TESTING OF MANYCORE SYSTEMS IN THE DARK SILICON ERA**
Mohammad-Hashem Haghbayan[1], Amir-Mohammad Rahmani[1], Mohammad Fattah[1], Pasi Liljeberg[1], Juha Plosila[1], Hannu Tenhunen[2] and Zainalabedin Navabi[3]
[1]University of Turku, FI; [2]KTH Royal Institute of Technology, SE; [3]Worcester Polytechnic Institute, US

4.7 How Resilient Are Emerging Technologies?

Les Bans 1700 - 1830

Chair: **Vikas Chandra,** ARM, US
Co-Chair: **Mehdi Tahoori,** KIT, DE

Many new technologies are being proposed as alternatives to conventional CMOS design. Resiliency, including robustness, reliability and fault modeling, will be a key factor in their success. This session includes results on several of these, as well as IP presentations on two others.

1700 **DIGITAL CIRCUITS RELIABILITY WITH IN-SITU MONITORS IN 28NM FULLY DEPLETED SOI**
Marine Saliva[1], Florian Cacho[1], Vincent Huard[1], Xavier Federspiel[1], Damien Angot[1], Ahmed Benhassain[1], Alain Bravaix[2] and Lorena Anghel[3]
[1]STMicroelectronics, FR; [2]IM2NP-ISEN, FR; [3]TIMA, FR

1730 **READ/WRITE ROBUSTNESS ESTIMATION METRICS FOR SPIN TRANSFER TORQUE (STT) MRAM CELL**
Elena Ioana Vatajelu[1], Rosa Rodriguez-Montañés[2], Marco Indaco[1], Michel Renovell[3], Paolo Prinetto[1] and Joan Figueras[2]
[1]Politecnico di Torino, IT; [2]Universitat Politecnica de Catalunya, ES; [3]LIRMM-CNRS,

1800 **FAULT MODELING IN CONTROLLABLE POLARITY SILICON NANOWIRE CIRCUITS**
Hassan Ghasemzadeh Mohammadi[1], Pierre-Emmanuel Gaillardon[2] and Giovanni De Micheli[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]École Polytechnique Fédérale de Lausanne (EPFL),

IPS **IP2-3, IP2-4**

4.8 Strength by Interdisciplinary Research: The Cadence Academic Network

Salle Lesdiguières 1700 - 1830

Organiser: **Patrick Haspel,** Cadence Academic Network, US
Chair: **Jürgen Haase,** edacentrum GmbH, DE

The Academic Network was launched by Cadence in 2007. The aim was to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence was established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems.

Specific examples of research directions in the cadence academic network will be given in three talks.

1700 **INTRODUCTION TO THE ACADEMIC NETWORK**
Patrick Haspel, Cadence Academic Network, US

1715 **DEPENDABILITY AND DESIGN-FOR-TESTABILITY**
Said Hamdioui, Delft University of Technology, NL

1740 **DIGITAL SYSTEM DESIGN**
Mladen Berekovic, TU Braunschweig, DE

1805 **SYSTEM LEVEL DEVELOPMENT USING VIRTUAL PROTOTYPING**
Michael Hübner, Ruhr-University Bochum, DE

1830 **EXHIBITION RECEPTION**
Several serving points inside the Exhibition Area

The Exhibition Reception will take place on Tuesday, March 10, 2015, from 1830-1930 in the exhibition area of the congress center, where free drinks for all conference delegates and exhibition visitors will be offered.

SPECIAL DAY

5.1 SPECIAL DAY Hot Topic: Applications of IoT

Salle Oisans 0830 - 1000

Organisers: **Ahmed Jerraya,** CEA, FR
Rolf Drechsler, University of Bremen/DFKI GmbH, DE
Chair: **Gabriela Nicolescu,** Ecole Polytechnique Montreal, CA
Co-Chair: **Ahmed Jerraya,** CEA, FR

Internet of things (IoT) applications is changing the landscape of the whole society and even non-traditional ICT intensive domains. More products in all market segments are emerging every day and is changing the way human and machines are interacting. This represents a great opportunity for innovators in industry and new vistas of research for academia. This session overview several application domains already impacted by this IoT wave.

0830 **IOT FOR HEALTHCARE**
Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH

0852 **IOT FOR SMART HOME**
Sylvain Paineau, Schneider Electric, FR

0914 **IOT FOR AUTOMOTIVE**
Juergen Hornung, Bosch, DE

0936 **IOT FOR SMART CITIES**
Levent Gurgen, CEA/LETI, FR

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.2 Hardware Trojan and Active Implementation Attacks

Belle-Etoile 0830 - 1000

Chair: **Paolo Maistri,** TIMA, FR
Co-Chair: **Viktor Fischer,** Hubert Curien Laboratory, FR

This session proposes novel techniques to detect hardware Trojans inserted at gate level and presents improvements and novel targets for fault attacks.

0830 **IMPROVED PRACTICAL DIFFERENTIAL FAULT ANALYSIS OF GRAIN-128**
Prakash Dey[1], Abhishek Chakraborty[2], Avishek Adhikari[1] and Debdeep Mukhopadhyay[2]
[1]Department of Pure Mathematics, University of Calcutta, Kolkata-[700019], IN; [2]Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur, Kharagpur-[721302], IN

0900 **A SCORE-BASED CLASSIFICATION METHOD FOR IDENTIFYING HARDWARE-TROJANS AT GATE-LEVEL NETLISTS**
Masaru Oya, Youhua Shi, Masao Yanagisawa and Nozomu Togawa, Waseda University, JP

0930 **HARDWARE TROJAN DETECTION FOR GATE-LEVEL ICS USING SIGNAL CORRELATION BASED CLUSTERING**
Burcin Cakir and Sharad Malik, Princeton University, US

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.3 Variability Challenges in Nanoscale Circuits

Stendhal 0830 - 1000

Chair: **Pablo Garcia del Valle,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Co-Chair: **Muhammad Shafique,** Karlsruhe Institute of Technology, DE

This session proposes new techniques to address variability related challenges in nanoscale chips. The topics addressed include retention time variations in DRAM and variations in the power delivery network.

0830 **EXPLOITING DRAM RESTORE TIME VARIATIONS IN DEEP SUB-MICRON SCALING**
Xianwei Zhang[1], Youtao Zhang[1], Bruce Childers[1] and Jun Yang[2]
[1]Department of Computer Science, University of Pittsburgh, US; [2]Electrical and Computer Engineering Department, University of Pittsburgh, US

0900 **ADAPTIVELY TOLERATE POWER-GATING-INDUCED POWER/GROUND NOISE UNDER PROCESS VARIATIONS**
Zhe Wang, Xuan Wang, Jiang Xu, Xiaowen Wu, Zhehui Wang, Peng Yang, Luan H. K. Duong, Haoran Li, Rafael K. V. Maeda and Zhifei Wang, HKUST, HK

0930 **ENERGY VERSUS DATA INTEGRITY TRADE-OFFS IN EMBEDDED HIGH-DENSITY LOGIC COMPATIBLE DYNAMIC MEMORIES**
Adam Teman[1], Georgios Karakonstantis[2], Robert Giterman[3], Pascal Meinerzhagen[4] and Andreas Burg[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]Queen's University, CH; [3]Ben-Gurion University, IL; [4]Intel Labs, US

0945 **RETENTION TIME MEASUREMENTS AND MODELLING OF BIT ERROR RATES OF WIDE-I/O DRAM IN MPSOCS**
Christian Weis[1], Matthias Jung[1], Peter Ehses[1], Cristiano Santos[2], Pascal Vivet[3], Sven Goossens[4], Martijn Koedam[4] and Norbert Wehn[1]
[1]University of Kaiserslautern, DE; [2]UFGRS, Porto Alegre and CEA-Leti, France, BR; [3]CEA-Leti, FR; [4]Eindhoven University of Technology, NL

IPS **IP2-6, IP2-7**

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.4 Emerging Technologies for NoCs

Chartreuse 0830 - 1000

Chair: **Ian O'Connor,** University of Lyon, FR
Co-Chair: **Davide Bertozzi,** University of Ferrara, IT

Several new technologies are enabling capabilities for NoCs. In this session, we demonstrate how to leverage optical, 3D and wireless methodologies to improve your NoCs. The first paper explores crosstalk mitigation techniques in optical NoCs. The second paper explores TSV minimization through virtual channels and the final paper deals with dynamic calibration in wireless NoCs.

0830 **COHERENT CROSSTALK NOISE ANALYSES IN RING-BASED OPTICAL INTERCONNECTS**
Luan H.K. Duong[1], Mahdi Nikdast[2], Jiang Xu[1], Zhehui Wang[1], Yvain Thonnart[3], Sébastien Le Beux[4], Peng Yang[1], Xiaowen Wu[1] and Zhifei Wang[1]
[1]The Hong Kong University of Science and Technology, HK; [2]École Polytechnique de Montréal, Montréal, CA; [3]CEA-Leti, FR; [4]Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

0900 **ENABLING VERTICAL WORMHOLE SWITCHING IN 3D NOC-BUS HYBRID SYSTEMS**
Changlin Chen, Marius Enachescu and Sorin Cotofana, Delft University of Technology, NL

0930 **A CLOSED LOOP TRANSMITTING POWER SELF-CALIBRATION SCHEME FOR ENERGY EFFICIENT WINOC ARCHITECTURES**
Andrea Mineo[1], Mohd Shahrizal Rusli[2], Maurizio Palesi[3], Giuseppe Ascia[1], Vincenzo Catania[1] and M. N. Marsono[2]
[1]University of Catania, IT; [2]Universiti Teknologi Malaysia, MY; [3]Kore University, IT

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.5 Critical Embedded Systems

Meije 0830 - 1000

Chair: **Lothar Thiele,** Swiss Federal Institute of Technology Zurich, CH
Co-Chair: **Iain Bate,** University of York, GB

The papers in this session focus on design concerns for safety-critical embedded systems. Topics include scheduling for engine-control tasks, fault tolerance, real-time communication, and safety and security in embedded systems.

0830 SUFFICIENT RESPONSE TIME ANALYSIS CONSIDERING DEPENDENCIES BETWEEN RATE-DEPENDENT TASKS
Timo Feld[1] and Frank Slomka[2]
[1]Institute of Embedded Systems / Real-Time Systems Ulm University, DE; [2]Ulm University, DE

0900 ENGINE CONTROL: TASK MODELLING AND ANALYSIS
Alessandro Biondi and Giorgio Buttazzo, Scuola Superiore Sant'Anna, IT

0930 EVALUATION OF DIVERSE COMPILING FOR SOFTWARE-FAULT TOLERANCE
Andrea Höller[1], Nermin Kajtazovic[2], Tobias Rauter[2], Kay Römer[2] and Christian Kreiner[2]
[1]TU Graz, AT; [2]Graz University of Technology, AT

0945 WORST-CASE COMMUNICATION TIME ANALYSIS OF NETWORKS-ON-CHIP WITH SHARED VIRTUAL CHANNELS
Eberle A Rambo and Rolf Ernst, TU Braunschweig, DE

IPS IP2-9, IP2-10

1000 COFFEE BREAK IN EXHIBITION AREA

5.6 Analyzing and Improving Memories

Bayard 0830 - 1000

Chair: **Bartomeu Alorda,** Balearic Islands University, ES
Co-Chair: **Panagiota Papavramidou,** IMAG, FR

Memories are a driving force behind virtually all IC designs. This session describes methods of improving memory architecture, robustness, and lifetime.

0830 ON THE STATISTICAL MEMORY ARCHITECTURE EXPLORATION AND OPTIMIZATION
Charalampos Antoniadis[1], Georgios Karakonstantis[2], Nestoras Evmorfopoulos[1], Andreas Burg[3] and George Stamoulis[1]
[1]University of Thessaly, GR; [2]Queen's University, GB; [3]École Polytechnique Fédérale de Lausanne (EPFL), CH

0900 ECRIPSE: AN EFFICIENT METHOD FOR CALCULATING RTN-INDUCED FAILURE PROBABILITY OF AN SRAM CELL
Hiromitsu Awano, Masayuki Hiromoto and Takashi Sato, Kyoto University, JP

0930 SUBPAGE PROGRAMMING FOR EXTENDING THE LIFETIME OF NAND FLASH MEMORY
Jung-Hoon Kim[1], Sang-Hoon Kim[2] and Jin-Soo Kim[3]
[1]Samsung Electronics Corp., KR; [2]KAIST, KR; [3]Sungkyunkwan University, KR

1000 COFFEE BREAK IN EXHIBITION AREA

5.7 Architectures and Design for Cyber-Physical Systems

Les Bans 0830 - 1000

Chair: **Rolf Ernst,** Technische Universität Braunschweig, DE
Co-Chair: **Paul Pop,** Technical University of Denmark, DK

The session covers architectures for non-volatile processors, mixed-criticality, reliable and self-aware systems, and design optimisation issues such as system synthesis for reliability and cost, online scheduling and FPGA acceleration.

0830 OPTIMIZED SELECTION OF RELIABLE AND COST-EFFECTIVE CYBER-PHYSICAL SYSTEM ARCHITECTURES
Nikunj Bajaj[1], Pierluigi Nuzzo[1], Michael Masin[2] and Alberto Sangiovanni-Vincentelli[1]
[1]University of California at Berkeley, US; [2]IBM Haifa Research Lab, IL

0900 SOFTWARE ASSISTED NON-VOLATILE REGISTER REDUCTION FOR ENERGY HARVESTING BASED CYBER-PHYSICAL SYSTEM
Mengying Zhao[1], Qingan Li[2], Mimi Xie[3], Yongpan Liu[4], Jingtong Hu[3] and Jason Xue[1]
[1]City University of Hong Kong, HK; [2]Wuhan University & City University of Hong Kong, CN; [3]Oklahoma State University, US; [4]Tsinghua University, CN

0930 A RE-ENTRANT FLOWSHOP HEURISTIC FOR ONLINE SCHEDULING OF THE PAPER PATH IN A LARGE SCALE PRINTER
Umar Waqas[1], Marc Geilen[1], Jack Kandelaars[2], Lou Somers[3], Twan Basten[1], Sander Stuijk[1], Patrick Vestjens[2] and Henk Corporaal[1]
[1]Eindhoven University of Technology, NL; [2]Oce Technologies, NL; [3]Oce technologies, NL

0945 MPIOV: SCALING HARDWARE-BASED I/O VIRTUALIZATION FOR MIXED-CRITICALITY EMBEDDED REAL-TIME SYSTEMS USING NON TRANSPARENT BRIDGES TO (MULTI-CORE) MULTI-PROCESSOR SYSTEMS
Daniel Muench[1], Michael Paulitsch[1], Oliver Hanka[1] and Andreas Herkersdorf[2]
[1]Airbus Group Innovation, DE; [2]TU Munich, DE

IPS IP2-11, IP2-12, IP2-13

1000 COFFEE BREAK IN EXHIBITION AREA

5.8 Hot Topic - The Next Generation of Virtual Prototyping: Ultra-fast yet Accurate Simulation of HW/SW Systems

Salle Lesdiguières 0830 - 1000

Organisers: **Oliver Bringmann,** University of Tübingen, DE
Daniel Müller-Gritschneder, Technische Universitaet München, DE
Chair: **Andy D. Pimentel,** University of Amsterdam, NL
Co-Chair: **Christian Haubelt,** University of Rostock, DE

This session addresses leading-edge solutions in the field of virtual prototyping. Employing techniques such as source-level software simulation, host-compiled firmware, OS and processor modeling, as well as abstract communication and peripheral models, it is possible to reach very high simulation speeds. With intelligent new out-of-order modeling, synchronization and temporal decoupling techniques, such ultra-fast simulation can be achieved while also maintaining a very high accuracy.

0830 ULTRA-FAST SOURCE-LEVEL TIMING SIMULATION – HIGH ACCURACY NEEDS EXACT CODE MATCHING
Oliver Bringmann, University of Tuebingen / FZI, DE

0852 HOST-COMPILED OPERATING SYSTEM AND PROCESSOR MODELING
Andreas Gerstlauer, The University of Texas at Austin, US

0915 **ABSTRACT COMMUNICATION MODELS FOR ACCURATE AND FAST SOC SIMULATION**
Daniel Mueller-Gritschneder, Technische Universität München, DE

0937 **INDUSTRIAL PERSPECTIVE ON ULTRA-HIGH SPEED AND TIMING-ACCURATE SOC AND PERIPHERAL MODELS**
Ajay Goyal, Infineon Technologies, IN

1000 **COFFEE BREAK IN EXHIBITION AREA**

IP2 Interactive Presentations, sponsored by Cadence Academic Network

1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP2-1 **COMPARISON OF MULTI-PURPOSE CORES OF KECCAK AND AES**
Panasayya Yalla, Ekawat Homsirikamol and Jens-Peter Kaps, George Mason University, US

IP2-2 **ON-LINE PREDICTION OF NBTI-INDUCED AGING RATES**
Rafal Baranowski[1], Farshad Firouzi[2], Saman Kiamehr[2], Chang Liu[1], Hans-Joachim Wunderlich[1] and Mehdi Tahoori[2]
[1]Stuttgart University, DE; [2]Karlsruhe Institute of Technology (KIT), DE

IP2-3 **RETRAINING BASED TIMING ERROR MITIGATION FOR HARDWARE NEURAL NETWORKS**
Jiachao Deng[1], Yuntan Fang[1], Zidong Du[1], Ying Wang[1], Huawei Li[1], Olivier Temam[2], Paolo Ienne[3], David Novo[3], Xiaowei Li[1], Yunji Chen[1] and Chengyong Wu[1]
[1]State Key Laboratory of Computer Architecture, ICT, CAS, Beijing, China †University of Chinese Academy of Sciences, Beijing, China, CN; [2]INRIA Saclay, France, FR; [3]École Polytechnique Fédérale de Lausanne (EPFL), CH

IP2-4 **DICTIONARY-BASED SPARSE REPRESENTATION FOR RESOLUTION IMPROVEMENT IN LASER VOLTAGE IMAGING OF CMOS INTEGRATED CIRCUITS**
Tenzile Berkin Cilingiroglu, Mahmoud Zangeneh, Aydan Uyar, W. Clem Karl, Janusz Konrad, Ajay Joshi, Bennett B. Goldberg and M. Selim Unlu, Boston University, US

IP2-5 **FAULT-BASED ATTACKS ON THE BEL-T BLOCK CIPHER FAMILY**
Philipp Jovanovic and Ilia Polian, University of Passau, DE

IP2-6 **ON THE PREMISES AND PROSPECTS OF TIMING SPECULATION**
Rong Ye[1], Feng Yuan[2], Jie Zhang[2] and Qiang Xu[2]
[1]Imperial College, GB; [2]The Chinese University of Hong Kong, HK

IP2-7 **IMPACT OF INTERCONNECT MULTIPLE-PATTERNING VARIABILITY ON SRAMS**
Ioannis Karageorgos[1], Michele Stucchi[2], Praveen Raghavan[2], Julien Ryckaert[2], Zsolt Tokei[2], Diederik Verkest[2], Rogier Baert[2], Sushil Sakhare[2] and Wim Dehaene[3]
[1]imec, BE; [2]IMEC, BE; [3]KU Leuven, imec, BE

IP2-8 **COHERENCE BASED MESSAGE PREDICTION FOR OPTICALLY INTERCONNECTED CHIP MULTIPROCESSORS**
Anouk Van Laer[1], Chamath Ellawala[1], Muhammad Ridwan Madarbux[1], Timothy M. Jones[2] and Philip M. Watts[1]
[1]University College London, GB; [2]University of Cambridge, GB

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IP2-9 **OPENMP AND TIMING PREDICTABILITY: A POSSIBLE UNION?**
Roberto Vargas[1], Eduardo Quinones[2] and Andrea Marongiu[3]
[1]Barcelona Supercomputing Center (BSC) and Technical University of Catalonia (UPC), ES; [2]Barcelona Supercomputing Center (BSC), ES; [3]Swiss Federal Institute of Technology in Zurich (ETHZ), CH

IP2-10 **SAHARA: A SECURITY-AWARE HAZARD AND RISK ANALYSIS METHOD**
Georg Macher[1], Harald Sporer[1], Reinhard Berlach[1], Eric Armengaud[2] and Christian Kreiner[1]
[1]Graz University of Technology, AT; [2]AVL List GmbH, AT

IP2-11 **CYBERPHYSICAL-SYSTEM-ON-CHIP (CPSOC) : A SELF-AWARE MPSOC PARADIGM WITH CROSS-LAYER VIRTUAL SENSING AND ACTUATION**
Nikil Dutt[1], Puneet Gupta[2], Nalini Venkatasubramanian[3] and Alex Nicolau[1]
[1]University of California Irvine, US; [2]University of California Los Angeles, US; [3],

IP2-12 **OCCUPANCY DETECTION VIA IBEACON ON ANDROID DEVICES FOR SMART BUILDING MANAGEMENT**
Andrea Corna, Lorenzo Fontana, Alessandro Antonio Nacci and Donatella Sciuto, Politecnico di Milano, IT

IP2-13 **A NEURAL MACHINE INTERFACE ARCHITECTURE FOR REAL-TIME ARTIFICIAL LOWER LIMB CONTROL**
Jason Kane, Qing Yang, Robert Hernandez, Willard Simoneau and Matthew Seaton, University of Rhode Island, US

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.1 SPECIAL DAY Hot Topic: Platforms for the IoT

Salle Oisans 1100 - 1230

Organisers: **Christoph Grimm,** TU Kaiserslautern, DE
Rolf Drechsler, University of Bremen/DFKI GmbH, DE
Chair: **Christoph Grimm,** TU Kaiserslautern, DE
Co-Chair: **Marie-Minerve Louerat,** University of Paris, FR

The pervasive networking of embedded systems enables the vision of the "Internet of Things". Appliances are built on top of and using hardware, software, and communication platforms. The presentations in this session cover the new and challenging requirements: The first presentation gives a visionary overview of how platforms will be used in an open, dynamic and organic way. To make these visions happen right now, technical challenges are addressed: in the second presentation, energy-awareness electronic platforms are in the focus. In the third presentation, an overview of software architectures for the IoT is given. Last but not least, standardized networking at semantic layer is required to enable machine-to-machine (M2M) communication and intelligent service discovery.

1100 **THE HUMAN INTRANET: WHERE SWARMS AND HUMANS MEET**
Jan Rabaey, UC Berkeley, US

1122 **ENERGY EFFICIENT ELECTRONICS FOR THE INTERNET OF THINGS**
Stefan Heinen, RWTH Aachen, DE

1144 **SOFTWARE ARCHITECTURES FOR THE INTERNET OF THINGS**
Mario Trapp, FhG IESE, DE

1206 **ONEM2M : A STANDARD FOR AN OPEN AND INTEROPERABLE M2M PLATFORM, THANKS TO SEMANTIC WEB TOOLS**
Marylin Arndt-Vincent, Orange Labs, FR

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.2 Physical Unclonable Functions

Belle-Etoile 1100 - 1230

Chair: **Ingrid Verbauwhede,** KUL, BE
Co-Chair: **Tim Güneysu,** Ruhr University Bochum, DE

Physically Unclonable Functions (PUF) have received much attention for fingerprinting and as secret key provider in electronic devices. This session presents novel constructions and attacks on Arbiter, Ring-Oscillator and DRAM PUFs.

1100 **EFFICIENT ATTACKS ON ROBUST RING OSCILLATOR PUF WITH ENHANCED CHALLENGE-RESPONSE SET**
Phuong Ha Nguyen, Durga Prasad Sahoo, Rajat Subhra Chakraborty and Debdeep Mukhopadhyay, Indian Institute of Technology Kharagpur, IN

1130 **A ROBUST AUTHENTICATION METHODOLOGY USING PHYSICALLY UNCLONABLE FUNCTIONS IN DRAM ARRAYS**
Maryam S. Hashemian[1], Bhanu Singh[1], Francis Wolff[1], Chris Papachristou[1], Steve Clay[2] and Daniel Weyer[2]
[1]Case Western Reserve University, US; [2]Rockwell Automation, US

1200 **A NOVEL MODELING ATTACK RESISTANT PUF DESIGN BASED ON NON-LINEAR VOLTAGE TRANSFER CHARACTERISTICS**
Arunkumar Vijayakumar and Sandip Kundu, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, US

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.3 Emerging Low Power Techniques

Stendhal 1100 - 1230

Chair: **Guillermo Payá Vayá,** Leibniz Universität Hannover, DE
Co-Chair: **Alberto Garcia-Ortiz,** U. Bremen, DE

Technology improvements towards the nanometric era are inducing new challenges which need to be addressed at all the abstration levels. This section focuses on the latest emerging approaches to cope with those challenges, as for example approximate computing, compressed sensing, asymmetric underlapped FinFET, etc.

1100 **ASYMMETRIC UNDERLAPPED FINFET BASED ROBUST SRAM DESIGN AT 7NM NODE**
Arun Goud Akkala[1], Rangharajan Venkatesan[2], Anand Raghunathan[1] and Kaushik Roy[1]
[1]Purdue University, US; [2]NVIDIA Corporation, US

1130 **QUALITY CONFIGURABLE REDUCE-AND-RANK FOR ENERGY EFFICIENT APPROXIMATE COMPUTING**
Arnab Raha, Swagath Venkataramani, Vijay Raghunathan and Anand Raghunathan, Purdue University, US

1200 **ULTRA-LOW-POWER ECG FRONT-END DESIGN BASED ON COMPRESSED SENSING**
Hossein Mamaghanian[1] and Pierre Vandergheynst[2]
[1]EPFL, CH; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH

1215 **GTFUZZ: A NOVEL ALGORITHM FOR ROBUST DYNAMIC POWER OPTIMIZATION VIA GATE SIZING WITH FUZZY GAMES**
Tony Casagrande and Nagarajan Ranganathan, University of South Florida, US

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

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6.4 Bridging the Moore's Law Gap with Application-Specific Architectures

Chartreuse 1100 - 1230

Chair: **Cristina Silvano,** Politecnico di Milano, IT
Co-Chair: **Lars Bauer,** KIT, DE

This session focuses on approximation, low-power, and high-performance optimization techniques for application-specific architectures, including neural networks, multicores and GPUs.

1100 **A ULTRA-LOW-ENERGY CONVOLUTION ENGINE FOR FAST BRAIN-INSPIRED VISION IN MULTICORE CLUSTERS**
Francesco Conti[1] and Luca Benini[2]
[1]Università di Bologna, IT; [2]Università di Bologna / ETH Zürich, IT

1130 **ELIMINATING INTRA-WARP CONFLICT MISSES IN GPU**
Bin Wang, Zhuo Liu, Xinning Wang and Weikuan Yu, Auburn University, US

1200 **RNA: A RECONFIGURABLE ARCHITECTURE FOR HARDWARE NEURAL ACCELERATION**
Fengbin Tu[1], Shouyi Yin[1], Peng Ouyang[1], Leibo Liu[2] and Shaojun Wei[1]
[1]Tsinghua University, CN; [2]Institute of Microelectronics and The National Lab for Information Science and Technology, Tsinghua University, CN

1215 **APPROXANN: AN APPROXIMATE COMPUTING FRAMEWORK FOR ARTIFICIAL NEURAL NETWORK**
Qian Zhang, Ting Wang, Ye Tian, Feng Yuan and Qiang Xu, The Chinese University of Hong Kong, HK

IPS **IP3-3, IP3-4**

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.5 Multimedia and Consumer Electronics

Meije 1100 - 1230

Chair: **Theo Theocharides,** University of Cyprus, CY
Co-Chair: **Marcello Coppola,** STMicroelectronics, FR

This session presents hardware and software architectures that enable effective implementations of multimedia and consumer electronics systems.

1100 **DRAM OR NO-DRAM? EXPLORING LINEAR SOLVER ARCHITECTURES FOR IMAGE DOMAIN WARPING IN 28 NM CMOS**
Michael Schaffner[1], Frank K. Gürkaynak[1], Aljoscha Smolic[2] and Luca Benini[3]
[1]Swiss Federal Institute of Technology in Zurich (ETHZ), CH; [2]Disney Research Zurich, CH; [3]Università di Bologna / Swiss Federal Institute of Technology in Zurich (ETHZ), CH

1130 **A SMALL NON-VOLATILE WRITE BUFFER TO REDUCE STORAGE WRITES IN SMARTPHONES**
Mungyu Son[1], Sungkwang Lee[1], Kyungho Kim[2], Sungjoo Yoo[1] and Sunggu Lee[1]
[1]POSTECH, KR; [2]Samsung Electronics, KR

1200 **CLUSTERING-BASED MULTI-TOUCH ALGORITHM FRAMEWORK FOR THE TRACKING PROBLEM WITH A LARGE NUMBER OF POINTS**
Shih-Lun Huang, Sheng-Yi Hung and Chung-Ping Chen, Graduate Institute of Electronics Engineering, National Taiwan University, TW

1215 **A LOW ENERGY 2D ADAPTIVE MEDIAN FILTER HARDWARE**
Ercan Kalali and Ilker Hamzaoglu, Sabanci University, TR

IPS **IP3-5, IP3-6, IP3-7**

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.6 Panel - The Future of Electronics, Semiconductor, and Design in Europe

Bayard 1100 - 1230

Organiser: **Marco Casale-Rossi,** Synopsys, US
Chair: **Giovanni De Micheli,** École Polytechnique Fédérale de Lausanne (EPFL), CH

For more than a decade, Europe has been the wireless continent; today, wireless has almost completely shifted to the U.S. and Asia. This shift has had a profound impact on the electronic, semiconductor, and design ecosystem: long-time leaders have disappeared, or have abandoned the wireless business/market. Europe needs to re-invent itself once again. Is there a future for electronics, and IC design and manufacturing in Europe? If so, what are the applications, and the technologies that will bring Europe back to the top of the world leadership? This panel session will gather executives from the semiconductor, IP, and R&D sectors to discuss the prospects of our industry in Europe.

1100 **PANELISTS**
Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH
Jalal Bagherli, Dialog Semiconductor, US
Thierry Collette, LETI, France, FR
Antun Domic, Synopsys, US
Horst Symanzik, Bosch Sensortec, DE
Sir Hossein Yassaye, Imagination Technologies, US

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.7 Application-Mapping Strategies for Many-Cores

Les Bans 1100 - 1230

Chair: **Amit Kumar Singh,** University of York, GB
Co-Chair: **Marc Geilen,** Eindhoven University of Technology, NL

This session deals with application performance. The first paper proposes a performance model to guide run-time mapping. The other two papers optimize performance, one by mapping tasks to match the parallelism of the underlying architecture, and the other by identifying shared memory sections to facilitate parallel execution.

1100 **ADAPTIVE ON-THE-FLY APPLICATION PERFORMANCE MODELING FOR MANY CORES**
Sebastian Kobbe, Lars Bauer and Joerg Henkel, Karlsruhe Institute of Technology (KIT), DE

1130 **CUSTOMIZATION OF OPENCL APPLICATIONS FOR EFFICIENT TASK MAPPING UNDER HETEROGENEOUS PLATFORM CONSTRAINTS**
Edoardo Paone[1], Francesco Robino[2], Gianluca Palermo[1], Vittorio Zaccaria[1], Ingo Sander[2] and Cristina Silvano[1]
[1]Politecnico di Milano, IT; [2]KTH Royal Institute of Technology, SE

1200 **ENABLING MULTI-THREADED APPLICATIONS ON HYBRID SHARED MEMORY MANYCORE ARCHITECTURES**
Tushar Rawat and Aviral Shrivastava, Arizona State University, US

IPS **IP3-8, IP3-9**

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

6.8 → 6.6

Session 6.8 is part of the exhibition program open to all exhibition visitors, but takes place as session 6.6 in the larger room Bayard (no presentations in room Lesdiguières). Please refer to session 6.6 for the details.

1230 **LUNCH BREAK,**
in front of the session room Salle Oisans and in the exhibition area
Keynote lectures from 1250 – 1420 (Room Oisans)

7.0 SPECIAL DAY Keynotes

1250 - 1420

1250 **SPECIAL DAY KEYNOTE: INDUSTRIE 4.0: FROM THE INTERNET OF THINGS TO CYBER-PHYSICAL PRODUCTION SYSTEMS**
Wolfgang Wahlster, German Research Center for Artificial Intelligence (DFKI), DE

1320 **SPECIAL DAY KEYNOTE: THE RISE OF IOT, AND THE ROLE OF EDA**
Antun Domic, Synopsys, US

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.1 SPECIAL DAY Hot Topic: Design Tools for the IoT

Salle Oisans 1430 - 1600

Organisers: **Frank Schirrmeister,** Cadence, US
Rolf Drechsler, University of Bremen/DFKI GmbH, DE
Chair: **Frank Schirrmeister,** Cadence, US

This sessions will describe challenges and solutions regarding the development aspects of the internet of things. Based on user challenges described by NXP and Intel, ARM and Cadence will describe IP and tool offerings for development of Embedded Software as well as SoCs in edge node, gateway and cloud devices.

1430 **IOT CHALLENGES AND OPPORTUNITIES**
Hannes Schwaderer, Intel, DE

1452 **IOT DEVELOPMENT FOR A CONNECTED CAR**
Marco Bekooij, NXP Semiconductors, NL

1514 **IF IT'S NOT ON THE INTERNET, IT'S JUST A THING: BUT WHAT ARE THE IOT PROBLEMS TO SOLVE?**
Remy Pottier, ARM, FR

1536 **IOT HARDWARE & MIXED SIGNAL DEVELOPMENT**
Ian Dennison, Cadence, GB

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.2 Hot Topic - Trading Accuracy for Efficient Computing

Belle-Etoile 1430 - 1600

Organisers: **Anand Raghunathan,** Purdue University, US
Akash Kumar, National University of Singapore, SG
Chair: **Muhammad Shafique,** KIT: Karlsruhe Institute of Technology, DE
Co-Chair: **Marc Geilen,** Eindhoven University of Technology, NL

This session will introduce inexact or approximate computing, a promising direction to improve the efficiency of computing in the face of diminishing benefits from scaling. Speakers will discuss the key challenges in the field and provide a vision for bringing these technologies to the mainstream. The session will cover approximate hardware, system level inexactness, and memory models. An application of the design principles to weather simulation will also be presented.

1430 COMPUTING APPROXIMATELY, AND EFFICIENTLY

Swagath Venkataramani[1], Srimat T. Chakradhar[2], Kaushik Roy[1] and Anand Raghunathan[1]
[1]Purdue University, US; [2]NEC Laboratories America, US

1452 NOVEL INEXACTNESS AWARE ALGORITHM CO-DESIGN FOR ENERGY EFFICIENT COMPUTATION

Guru Prakash Arumugam[1], Ayush Bhargava[1], Prashanth Srikanthan[1], Sreelatha Yenugula[1], John Augustine[1], Eli Upfal[2] and Krishna Palem[3]
[1]Indian Institute of Technology Madras, IN; [2]Brown University, US; [3]Rice University, US

1515 DESIGNING INEXACT SYSTEMS EFFICIENTLY USING ELIMINATION HEURISTICS

Shyamsundar Venkataraman[1], Akash Kumar[1], Jeremy Schlachter[2] and Christian Enz[2]
[1]National University of Singapore, SG; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH

1537 OPPORTUNITIES FOR ENERGY EFFICIENT COMPUTING: A STUDY OF INEXACT GENERAL PURPOSE PROCESSORS FOR HIGH-PERFORMANCE AND BIG-DATA APPLICATIONS

Peter Duben[1], Jeremy Schlachter[2], - Parishkrati[3], Sreelatha Yenugula[3], John Augustine[3], Christian Enz[2], K. Palem[4] and T. N. Palmer[5]
[1]Oxford University, GB; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH; [3]Indian Institute of Technology Madras, IN; [4]Rice University, Houston, US; [5]University of Oxford, GB

1600 COFFEE BREAK IN EXHIBITION AREA

7.3 Hot Topic - Advances in Hardware Trojans Detection

Stendhal 1430 - 1600

Organiser: **Julien Francq,** Airbus Defence & Space -- CyberSecurity, FR
Chair: **Giorgio Di Natale,** LIRMM, CNRS/University of Montpellier, FR

Hardware Trojans (HTs) are malicious modifications of an Integrated Circuit (IC) during its design flow. These added transistors could induce in the infected IC some malicious effects. Complete trust in ICs has been now lost because of the outsourcing of the fabrication of the ICs and the complexity of the IC design flow. This special session will present some advances in HT detection developed in French funded research project HOMERE.

1430 INTRODUCTION TO HARDWARE TROJAN DETECTION METHODS

Julien Francq[1] and Florian Frick[2]
[1]Cassidian, FR; [2]University of Stuttgart, DE

1445 NEW TESTING PROCEDURE FOR FINDING INSERTION SITES OF STEALTHY HARDWARE TROJANS

Sophie Dupuis, Papa-Sidy Ba, Marie-Lise Flottes, Giorgio Di Natale and Bruno Rouzeyre, LIRMM, FR

1500 HARDWARE TROJAN DETECTION BY DELAY AND ELECTROMAGNETIC MEASUREMENTS

X-T. Ngo[1], I Exurville[2], S Bhasin[1], Jean-Luc Danger[1], Sylvain Guilley[1], Z Najm[1], Jean Baptiste Rigaud[3] and Bruno Robisson[2]
[1]Télécom ParisTech, FR; [2]CEA, FR; [3]EMSE, FR

1530 A HIGH EFFICIENCY HARDWARE TROJAN DETECTION TECHNIQUE BASED ON FAST SEM IMAGING

Franck Courbon[1], Philippe Loubet-Moundi[2], Fournier Jacques[3] and Assia Tria[3]
[1]GEMALTO Security Labs/Ecole des Mines de Saint-Etienne, FR; [2]Gemalto, FR; [3]CEA Tech Region DPACA/LSAS, FR

1600 COFFEE BREAK IN EXHIBITION AREA

7.4 Routing Advances for Fault-tolerant and Multicast NoCs

Chartreuse 1430 - 1600

Chair: **Fabien Clermidy,** CEA, FR
Co-Chair: **Masoud Daneshtalab,** University of Turku, FI

NoCs are migrating into large-scale multicore systems which lead to new issues to be solved. In this session, we see how NoCs can tackle both faulty behaviors and performance bottlenecks. The first paper demonstrates low overhead multicast using surface-wave communication. The two other papers deal with low-overhead and low-latency fault-tolerance.

1430 MIXED WIRE AND SURFACE-WAVE COMMUNICATION FABRICS FOR DECENTRALIZED ON-CHIP MULTICASTING

Ammar Karkar[1], Kin-Fai Tong[2], Terrence Mak[3] and Alex Yakovlev[1]
[1]School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, GB; [2]Department of Electrical and Electronic Engineering, UCL, London, GB; [3]Department of Computer Science and Engineering, The Chinese University of Hong Kong, Hong Kong, CN

1500 D2-LBDR: DISTANCE-DRIVEN ROUTING TO HANDLE PERMANENT FAILURES IN 2D MESH NOCS

Rimpy Bisnhoi[1], Manoj Gaur[1], Vijay Laxmi[1] and Josè Flich[2]
[1]Malaviya National Institute of Technology, IN; [2]Associate Professor, Universitat Politècnica de València, ES

1530 SYNERGISTIC USE OF MULTIPLE ON-CHIP NETWORKS FOR ULTRA-LOW LATENCY AND SCALABLE DISTRIBUTED ROUTING RECONFIGURATION

Marco Balboni[1], Josè Flich[2] and Davide Bertozzi[1]
[1]University of Ferrara, IT; [2]Associate Professor, Universitat Politècnica de València, ES

1600 COFFEE BREAK IN EXHIBITION AREA

7.5 System Reliability: from Runtime to Design Languages

Meije 1430 - 1600

Chair: **Dirk Stroobandt,** University of Gent, BE
Co-Chair: **Diana Goehringer,** University of Bochum, DE

Over the last few years, reliability has become an increasingly relevant consideration for electronic systems. This session will address system reliability from design flow to run-time in both digital as well as analog systems.

1430 AXILOG: LANGUAGE SUPPORT FOR APPROXIMATE HARDWARE DESIGN

Amir Yazdanbakhsh[1], Divya Mahajan[1], Bradley Thwaites[1], Jongse Park[1], Anandhavel Nagendrakumar[1], Sindhuja Sethuraman[1], Kartik Ramkrishnan[2], Nishanthi Ravindran[2], Rudra Jariwala[2], Abbas Rahimi[3], Hadi Esmailzadeh[1] and Kia Bazargan[2]
[1]Georgia Institute of Technology, US; [2]University of Minnesota, US; [3]University of San Diego, US

1500 **IMPROVING MPSOC RELIABILITY THROUGH ADAPTING RUNTIME TASK SCHEDULE BASED ON TIME-CORRELATED FAULT BEHAVIOR**
Laura A Rozo Duque[1], Jose Monsalve[2] and Chengmo Yang[1]
[1]University of Delaware, US; [2]University of Delaware, CO

1530 **ACSEM: ACCURACY-CONFIGURABLE FAST SOFT ERROR MASKING ANALYSIS IN COMBINATORIAL CIRCUITS**
Florian Kriebel, Semeen Rehman, Duo Sun, Pau Vilimelis Aceituno, Muhammad Shafique and Joerg Henkel, Karlsruhe Institute of Technology (KIT), DE

1545 **ENERGY MINIMIZATION FOR FAULT TOLERANT SCHEDULING OF PERIODIC FIXED-PRIORITY APPLICATIONS ON MULTIPROCESSOR PLATFORMS**
Qiushi Han[1], Ming Fan[1], Linwei Niu[2] and Gang Quan[1]
[1]Florida International University, US; [2]West Virginia State University, US

IPS **IP3-11, IP3-12, IP3-13**

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.6 Test Power and 3-D Fault Tolerance

Bayard 1430 - 1600

Chair: **Juergen Schloeffel,** Mentor, DE
Co-Chair: **Sybille Hellebrand,** Universität Paderborn, DE

The section presents low power solutions for scan-based test and a new redundant TSV architecture for 3-D ICs

1430 **DP-FILL : A DYNAMIC PROGRAMMING APPROACH TO X-FILLING FOR MINIMIZING PEAK TEST POWER IN SCAN TESTS**
Satya A. Trinadh[1], Sobhan Babu Ch.[1], Shiv Govind Singh[1], Seetal Potluri[2] and Kamakoti V[2]
[1]Indian Institute of Technology Hyderabad, IN; [2]Indian Institute of Technology Madras, IN

1500 **A SCAN PARTITIONING ALGORITHM FOR REDUCING CAPTURE POWER OF DELAY-FAULT LBIST**
Nan Li[1], Elena Dubrova[2] and Gunnar Carlsson[3]
[1]Royal Institute of Technology, SE; [2]Ericsson AB/Royal Institute of Technology - KTH, SE; [3]Development Unit Radio, Ericsson AB, SE

1530 **ARCHITECTURE OF RING-BASED REDUNDANT TSV FOR CLUSTERED FAULTS**
Wei-Hen Lo, Kang Chi and TingTing Hwang, National Tsing Hua University, TW

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.7 Energy-efficient Computing

Les Bans 1430 - 1600

Chair: **Damien Querlioz,** CNRS-IEF, FR
Co-Chair: **Swaroop Ghosh,** University of South Florida, US

The papers in this session are all focused on energy efficient computing. In the first talk, the authors present approaches for accelerating learning algorithms for resistive cross-point arrays. The next paper considers what training schemes are most suitable when RRAM arrays are used to realize spiking neural networks. Finally, the last presentation will discuss how devices that offer the potential for non-volatile state retention can be employed in power gating architectures.

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1430 **TECHNOLOGY-DESIGN CO-OPTIMIZATION OF RESISTIVE CROSS-POINT ARRAY FOR ACCELERATING LEARNING ALGORITHMS ON CHIP**
Pai-Yu Chen, Deepak Kadetotad, Zihan Xu, Abinash Mohanty, Binbin Lin, Jieping Ye, Sarma Vrudhula, Jae-sun Seo, Yu Cao and Shimeng Yu, Arizona State University, US

1500 **SPIKING NEURAL NETWORK WITH RRAM: CAN WE USE IT FOR REAL-WORLD APPLICATION?**
Tianqi Tang[1], Lixue Xia[1], Boxun Li[1], Rong Luo[1], Yiran Chen[2], Yu Wang[1] and Huazhong Yang[1]
[1]Tsinghua University, CN; [2]University of Pittsburgh, US

1530 **COMPARATIVE STUDY OF POWER-GATING ARCHITECTURES FOR NONVOLATILE FINFET-SRAM USING SPINTRONICS-BASED RETENTION TECHNOLOGY**
Yusuke Shuto[1], Shuu'ichirou Yamamoto[1] and Satoshi Sugahara[2]
[1]Tokyo Institute of Technology, JP; [2]Tokyo Institute of Technology,

IPS **IP3-15, IP3-16**

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.8 Critical Research Areas Driven by Industry Transformations

Salle Lesdiguières 1430 - 1600

Organiser: **John Zhao,** MathWorks, US
Moderator: **Pieter Mostermann,** MathWorks, US

Increasing demands of electrification arise from connected vehicles, medical devices, smart-grid and microgrid technologies, and the IoT evolution of devices into smart, interconnected systems. Those systems must meet market requirements for not only more sophisticated functionality, but also improved performance and robustness. As a result, companies need to transform how they design, analyze, implement, and verify their systems. At the same time, embedded-system platforms have become increasingly diverse combinations of digital/analog electronics and software, ranging from FPGA/ARM platforms (e.g,. Xilinx Zynq and Altera SoC) to a diverse range of heterogeneous manycore systems.

To help companies leverage these trends in their product and system development, EDA and embedded-system researchers are called upon to focus their research on new kinds of issues that arise. This panel will explore the key research needs and opportunities that come from the transformations that industries must embrace.

1430 **PANEL PRESENTATIONS AND DISCUSSIONS, WITH Q&A**

1600 **COFFEE BREAK IN EXHIBITION AREA**

IP3 Interactive Presentations, sponsored by Cadence Academic Network

1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP3-1 STT MRAM-BASED PUFS
Elena Ioana Vatajelu[1], Giorgio Di Natale[2], Marco Indaco[1] and Paolo Prinetto[1]
[1]Politecnico di Torino, IT; [2]LIRMM, FR

IP3-2 SPATIAL AND TEMPORAL GRANULARITY LIMITS OF BODY BIASING IN UTBB-FDSOI
Johannes Maximilian Kühn[1], Dustin Peterson[1], Hideharu Amano[2], Oliver Bringmann[1] and Wolfgang Rosenstiel[1]
[1]Eberhard Karls Universität Tübingen, DE; [2]Keio University, JP

IP3-3 A HARDWARE IMPLEMENTATION OF A RADIAL BASIS FUNCTION NEURAL NETWORK USING STOCHASTIC LOGIC
Yuan Ji[1], Feng Ran[1], Cong Ma[2] and David Lilja[2]
[1]Shanghai University, CN; [2]University of Minnesota - Twin Cities, US

IP3-4 SODA: SOFTWARE DEFINED FPGA BASED ACCELERATORS FOR BIG DATA
Chao Wang, Xi Li and Xuehai Zhou, University of Science and Technology of China, CN

IP3-5 DYNAMIC RECONFIGURABLE PUNCTURING FOR SECURE WIRELESS COMMUNICATION
Liang Tang[1], Jude Angelo Ambrose[2], Akash Kumar[1] and Sri Parameswaran[2]
[1]National University of Singapore, SG; [2]University of New South Wales, AU

IP3-6 QR-DECOMPOSITION ARCHITECTURE BASED ON TWO-VARIABLE NUMERIC FUNCTION APPROXIMATION
Jochen Rust, Frank Ludwig and Steffen Paul, University of Bremen, DE

IP3-7 IN-PLACE MEMORY MAPPING APPROACH FOR OPTIMIZED PARALLEL HARDWARE INTERLEAVER ARCHITECTURES
Saeed Ur Rehman[1], Cyrille Chavet[2], Philippe Coussy[2] and Awais Sani[1]
[1]Lab-STICC / Université de Bretagne Sud, PK; [2]Lab-STICC / Université de Bretagne Sud, FR

IP3-8 MAXIMIZING COMMON IDLE TIME ON MULTI-CORE PROCESSORS WITH SHARED MEMORY
Chenchen Fu[1], Yingchao Zhao[2], Minming Li[3] and Jason Xue[3]
[1]Department of Computer Science, City University of Hong Kong, HK; [2]Department of Computer Science, Caritas Institute of Higher Education, Hong Kong, HK; [3]City University of Hong Kong, HK

IP3-9 MAXIMIZING IO PERFORMANCE VIA CONFLICT REDUCTION FOR FLASH MEMORY STORAGE SYSTEMS
Qiao Li[1], Liang Shi[2], Congming Gao[1], Kaijie Wu[1], Jason Chun Xue[3], Qingfeng Zhuge[1] and H.-M. Edwin Sha[4]
[1]Chongqing University, CN; [2]College of Computer Science, Chongqing University, CN; [3]City University of Hong Kong, HK; [4]Chongqing University and University of Texas at Dallas, CN

IP3-10 A HYBRID PACKET/CIRCUIT-SWITCHED ROUTER TO ACCELERATE MEMORY ACCESS IN NOC-BASED CHIP MULTIPROCESSORS
Yassin Mazloumi and Mehdi Modarressi, University of Tehran, IR

IP3-11 SEMIAUTOMATIC IMPLEMENTATION OF A BIOINSPIRED RELIABLE ANALOG TASK DISTRIBUTION ARCHITECTURE FOR MULTIPLE ANALOG CORES
Julius von Rosen[1], Markus Meissner[1] and Lars Hedrich[2]
[1]Goethe Universität Frankfurt, DE; [2]Goethe-Universitat Frankfurt a. M., DE

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IP3-12 POWER-EFFICIENT ACCELERATOR ALLOCATION IN ADAPTIVE DARK SILICON MANY-CORE SYSTEMS
Muhammad Usman Karim Khan, Muhammad Shafique and Joerg Henkel, Karlsruhe Institute of Technology (KIT), DE

IP3-13 THERMAL-AWARE FLOORPLANNING FOR PARTIALLY-RECONFIGURABLE FPGA-BASED SYSTEMS
Davide Pagano, Mikel Vuka, Marco Rabozzi, Riccardo Cattaneo, Donatella Sciuto and Marco D. Santambrogio, Politecnico di Milano, IT

IP3-14 FEEDBACK-BUS OSCILLATION RING: A GENERAL ARCHITECTURE FOR DELAY CHARACTERIZATION AND TEST OF INTERCONNECTS
Shi-Yu Huang[1], Meng-Ting Tsai[1], Kun-Han Tsai[2] and Wu-Tung Cheng[2]
[1]National Tsing Hua University, TW; [2]Mentor Graphics, US

IP3-15 ANALOG NEUROMORPHIC COMPUTING ENABLED BY MULTI-GATE PROGRAMMABLE RESISTIVE DEVICES
Vehbi Calayir, Mohamed Darwish, Jeffrey Weldon and Larry Pileggi, Carnegie Mellon University, US

IP3-16 AN ENERGY-EFFICIENT NON-VOLATILE IN-MEMORY ACCELERATOR FOR SPARSE-REPRESENTATION BASED FACE RECOGNITION
Yuhao Wang[1], Hantao Huang[1], Leibin Ni[1], Hao Yu[1], Mei Yan[1], Chuliang Weng[2], Wei Yang[2] and Junfeng Zhao[2]
[1]Nanyang Technological University, SG; [2]Shannon Laboratory, Huawei Technologies Co., Ltd, CN

8.1 SPECIAL DAY Panel: Security and Verification for the IoT

Salle Oisans 1700 - 1830

Organisers: **Dominique Borrione,** TIMA Lab, UGA, FR
Rolf Drechsler, University of Bremen/DFKI GmbH, DE
Chair: **Dominique Borrione,** TIMA Lab, UGA, FR
Co-Chair: **Guy Gogniat,** Lab-STICC, Université de Bretagne-Sud, Lorient, FR

1700 **PANELISTS**
Erdinç Öztürk, Ticaret University, TR
Guido Bertoni, STMicroelectronics, IT
Francois-Xavier Standaert, Université Catholique de Louvain, BE
Christoph Grimm, TU Kaiserslautern, DE
Sandip Kundu, University of Massachusetts Amherst, US

1930 **DATE PARTY**
in Museum of Grenoble (Musée de Grenoble, 5 Place de Lavalette, 38000 Grenoble, France)

8.2 Flash Memories & Numerical Approximation

Belle-Etoile 1700 - 1830

Chair: **Philippe Coussy,** Universite de Bretagne-Sud, FR
Co-Chair: **Zili Shao,** HongKong Polytechnic University, HK

This session presents papers on flash memories and numerical approximations. The first paper presents a new flash memory management scheme to extend the product lifetime of SSDs. The second paper describes a hardware accelerator approach for solving linear equations. The third paper describes an approach for automatically synthesizing non-linear 2D function approximations without requiring costly, and power-hungry, multipliers. Finally, the session ends with two interactive presentations that address progressive wear-leveling for flash memories, and security threats and countermeasures for solid-state drives.

1700 **HLC: SOFTWARE-BASED HALF-LEVEL-CELL FLASH MEMORY**
Han-Yi Lin[1] and Jen-Wei Hsieh[2]
[1]National Taiwan University, TW; [2]National Taiwan University of Science and Technology, TW

1730 **AHEAD: AUTOMATED FRAMEWORK FOR HARDWARE ACCELERATED ITERATIVE DATA ANALYSIS**
Ebrahim M. Songhori, Xuyang Lu and Farinaz Koushanfar, Rice University, US

1800 **DESIGN METHOD FOR MULTIPLIER-LESS TWO-VARIABLE NUMERIC FUNCTION APPROXIMATION**
Jochen Rust and Steffen Paul, University of Bremen, DE

IPS **IP4-1, IP4-2**

1930 **DATE PARTY**
in Museum of Grenoble (Musée de Grenoble, 5 Place de Lavalette, 38000 Grenoble, France)

8.3 Dynamic Thermal Management for Multi-cores

Stendhal 1700 - 1830

Chair: **Georgios Karakonstantis,** Queen's University, GB
Co-Chair: **José Luis Ayala,** Complutense University of Madrid, ES

This session covers the state-of-the-art in dynamic thermal management techniques for multi-core platforms in the mobile and high-performance computing domains. The issues addressed include thermal stress, thermal modeling and emerging cooling solutions.

1700 **A THERMAL STRESS-AWARE ALGORITHM FOR POWER AND TEMPERATURE MANAGEMENT OF MPSOCS**
Mehdi Kamal[1], Arman Iranfar[1], Ali Afzali-Kusha[1] and Massoud Pedram[2]
[1]University of Tehran, IR; [2]University of Southern California, US

1730 **PREDICTIVE DYNAMIC THERMAL AND POWER MANAGEMENT FOR HETEROGENEOUS MOBILE PLATFORMS**
Gaurav Singla[1], Gurinderjit Kaur[1], Ali Unver[2] and Umit Y Ogras[1]
[1]Arizona State University, US; [2]Intel Corporation, US

1800 **POWER-EFFICIENT CONTROL OF THERMOELECTRIC COOLERS CONSIDERING DISTRIBUTED HOT SPOTS**
Mohammad Javad Dousti and Massoud Pedram, University of Southern California, US

IPS **IP4-3, IP4-4**

1930 **DATE PARTY**
in Museum of Grenoble (Musée de Grenoble, 5 Place de Lavalette, 38000 Grenoble, France)

8.4 Industrial System Design Opportunities

Chartreuse 1700 - 1830

Chair: **Wehn Norbert,** University of Kaiserslautern, DE
Co-Chair: **David Raphael,** CEA-LIST, FR

This session introduces Innovative experiments from Industry that address the challenges of system design Each experiment presents a demonstrator and shows a substantial measurable economic and or strategic impact.

1700 **DSP BASED PROGRAMMABLE FHD HEVC DECODER**
Sangjo Lee[1], Joonho Song[2], Wonchang Lee[2], Doohyun Kim[2], Jaehyun Kim[2] and Shihwa Lee[2]
[1]SAMSUNG Electronics, KR; [2]Samsung Electronics,

1715 **ACCELERATING COMPLEX BRAIN-MODEL SIMULATIONS ON GPU PLATFORMS**
HoangAnh DuNguyen[1], Zaid Al-Ars[1], Georgios Smaragdos[2] and Christos Strydis[2]
[1]Delft University of Technology, NL; [2]Erasmus Medical Center, NL

1730 **A PACKET-SWITCHED INTERCONNECT FOR CONTROL APPLICATIONS ON ZYNQ WITH BEST-EFFORT AND REAL-TIME SERVICES**
Runan Ma[1], Axel Jantsch[2] and Zhida Hui[3]
[1]FuDan University, CN; [2]Vienna University of Technology, AT; [3]Memcom.Soc Microelectronics Ltd, CN

1745 **REDUCING TRACE SIZE IN MULTIMEDIA APPLICATIONS ENDURANCE TESTS**
Serge Vladimir Emteu Tchagou[1], Alexandre Termier[2], Jean-François Méhaut[3], Brice Videau[3], Miguel Santana[4] and René Quiniou[5]
[1]University of Grenoble Alpes, STMicroelectronics, FR; [2]University of Rennes [1], FR; [3]University of Grenoble Alpes, FR; [4]STMicroelectronics, FR; [5]INRIA Rennes, FR

1800 **EXPLORATION AND DESIGN OF EMBEDDED SYSTEMS INCLUDING NEURAL ALGORITHMS**
Jean-Marc Philippe[1], Alexandre Carbon[1], Olivier Brousse[2] and Michel Paindavoine[2]
[1]CEA LIST, FR; [2]GlobalSensing Technologies, FR

1815 **A NEW DISTRIBUTED FRAMEWORK FOR INTEGRATION OF DISTRICT ENERGY DATA FROM HETEROGENEOUS DEVICES**
Francesco Gavino Brundu[1], Edoardo Patti[1], Andrea Acquaviva[1], Michelangelo Grosso[2], Gaetano Rasconà[2], Salvatore Rinaudo[3] and Enrico Macii[1]
[1]Politecnico di Torino, IT; [2]ST-Polito s.c.ar.l., IT; [3]STMicroelectronics s.r.l., IT

1930 **DATE PARTY**
in Museum of Grenoble (Musée de Grenoble, 5 Place de Lavalette, 38000 Grenoble, France)

8.5 Hot Topic - Spintronics based Computing

Meije 1700 - 1830

Organisers: **Weisheng Zhao,** University Paris-Sud/CNRS, FR
Lionel Torres, LIRMM, CNRS/University of Montpellier, FR
Chair: **Lionel Torres,** LIRMM, CNRS/University of Montpellier, FR
Co-Chair: **Weisheng Zhao,** University Paris-Sud/CNRS, FR

Thanks to its non-volatility, fast data access, low power and infinite endurance, Spintronics (Nobel Prize 2007) is considered as one of the major technologies beyond CMOS to overcome the power and speed bottlenecks of advance computing systems. This topic is under intense study from device to system levels by both academics and industries. This session brings together the worldwide leading experts to share their recent results and discuss future challenges.

1700 **SPINTRONIC DEVICES AS KEY-ELEMENTS FOR ENERGY-EFFICIENT NEUROINSPIRED ARCHITECTURES**
Nicolas Locatelli[1], Adrien F. Vincent[2], Alice Mizrahi[2], Joseph S. Friedman[2], Damir Vodenicarevic[2], Joo-Von Kim[2], Jacques-Olivier Klein[2], Weisheng Zhao[3], Julie Grollier[4] and Damien Querlioz[2]
[1]Institut d'Electronique Fondamentale, Univ. Paris-Sud, CNRS, FR; [2]Institut d'Electronique Fondamentale, Univ. Paris-Sud, CNRS, FR; [3]Spintronics Interdisciplinary Center, Beihang University, Beijing, CN; [4]Unite Mixte de Physique CNRS/Thales and Universite Paris-Sud, FR

1720 **GIANT SPIN HALL EFFECT (GSHE) LOGIC DESIGN FOR LOW POWER APPLICATION**
Yaojun Zhang[1], Bonan Yan[1], Wenqing Wu[2], Hai Li[1] and Yiran Chen[1]
[1]University of Pittsburgh, US; [2]Qualcomm Incorporated, US

1740 **SPINTRONICS-BASED NONVOLATILE LOGIC-IN-MEMORY ARCHITECTURE TOWARDS AN ULTRA-LOW-POWER AND HIGHLY RELIABLE VLSI COMPUTING PARADIGM**
Takahiro Hanyu[1], Daisuke Suzuki[1], Naoya Onizawa[1], Shoun Matsunaga[2], Masanori Natsui[1] and Akira Mochizuki[1]
[1]Tohoku University, JP; [2]AC Technologies Co., Ltd., JP

1800 **POTENTIAL APPLICATIONS BASED ON NVM EMERGING TECHNOLOGIES**
Sophiane Senni[1], Raphael Martins Brum[1], Lionel Torres[2], Gilles Sassatelli[1], Abdoulaye Gamatie[1] and Bruno Mussard[3]
[1]LIRMM, FR; [2]LIRMM, CNRS/University of Montpellier, FR; [3]Crocus technology, FR

1815 **FROM DEVICE TO SYSTEM: CROSS-LAYER DESIGN EXPLORATION OF RACETRACK MEMORY**
Guangyu Sun[1], Chao Zhang[1], Hehe Li[2], Yue Zhang[3], Weiqi Zhang[1], Yizi Gu[2], Yinan Sun[2], Jacques-Olivier Klein[3], Dafine Ravelosona[3], Yongpan Liu[2], Weisheng Zhao[4] and Huazhong Yang[2]
[1]Peking University, CN; [2]Tsinghua University, CN; [3]Univ. Paris-Sud, FR; [4]Beihang University, CN

1930 **DATE PARTY**
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8.6 Statistical Answers to Analog/Mixed Signal Design and Test Problems

Bayard 1700 - 1830

Chair: **Jacob Abraham,** Univ. Texas Austin, US
Co-Chair: **Michel Renovell,** LIRMM/CNRS, FR

The session will demonstrate applications of Bayesian model fusion, machine learning classifiers, feature selection, virtual probe, and Quasi Monte Carlo for solving challenging design and test problems for analog and mixed signal circuits.

1700 **EFFICIENT BIT ERROR RATE ESTIMATION FOR HIGH-SPEED LINK BY BAYESIAN MODEL FUSION**
Chenlei Fang[1], Qicheng Huang[1], Fan Yang[1], Xuan Zeng[1], Xin Li[2] and Chenjie Gu[3]
[1]Fudan University, CN; [2]Carnegie Mellon University and Fudan University, US; [3]Strategic CAD Labs, Intel Corporation, US

1730 **FAST DEPLOYMENT OF ALTERNATE ANALOG TEST USING BAYESIAN MODEL FUSION**
John Liaperdos[1], Haralampos Stratigopoulos[2], Louay Abdallah[2], Yiorgos Tsiatouhas[3], Angela Arapoyanni[4] and Xin Li[5]
[1]Technological Educational Institute of Peloponnese, GR; [2]TIMA Laboratory, Université de Grenoble-Alpes/CNRS, FR; [3]University of Ioannina, GR; [4]National and Kapodistrian University of Athens, GR; [5]Carnegie Mellon University, US

1800 **BORDERSEARCH: AN ADAPTIVE IDENTIFICATION OF FAILURE REGIONS**
Markus Dobler[1], Manuel Harrant[2], Monica Rafaila[2], Georg Pelz[2], Wolfgang Rosenstiel[1] and Martin Bogdan[3]
[1]University of Tübingen, DE; [2]Infineon Technologies AG, DE; [3]University of Tübingen, Leipzig University, DE

1815 **A FAST SPATIAL VARIATION MODELING ALGORITHM FOR EFFICIENT TEST COST REDUCTION OF ANALOG/RF CIRCUITS**
Hugo Gonçalves[1], Xin Li[2], Miguel Correia[3], Vitor Tavares[3], John Carulli[4] and Kenneth Butler[5]
[1]CMU/FEUP, PT; [2]Carnegie Mellon University, US; [3]FEUP, PT; [4]GLOBALFOUNDRIES, US; [5]Texas Instruments, US

IPS **IP4-5, IP4-6**

1930 **DATE PARTY**
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8.7 Compilers and Tools for Performance

Les Bans 1700 - 1830

Chair: **Frank Hannig,** Erlangen University, DE
Co-Chair: **Christian Haubelt,** University of Rostock, DE

This session introduces different aspects of optimizing compiler technology in the context of embedded systems. The first paper shows that the performance of Android applications can be significantly improved by ahead-of-time compilation to C. The second paper shows how to generate efficient vector code from domain-specific (linear algebra) specifications. The first interactive presentation presents a technique to speed up the QEMU machine emulator by dynamic binary translation of vector instructions. The second one proposes a trace-based reuse distance profiler to help improving the memory profile of applications.

1700 **BYTECODE-TO-C AHEAD-OF-TIME COMPILATION FOR ANDROID DALVIK VIRTUAL MACHINE**
Hyeong-Seok Oh, Ji Hwan Yeo and Soo-Mook Moon, Seoul National University, KR

1730 **A BASIC LINEAR ALGEBRA COMPILER FOR EMBEDDED PROCESSORS**
Nikolaos Kyrtatas, Daniele Giuseppe Spampinato and Markus Püschel, Swiss Federal Institute of Technology in Zurich (ETHZ), CH

1800 **VARSHA: VARIATION AND RELIABILITY-AWARE APPLICATION SCHEDULING WITH ADAPTIVE PARALLELISM IN THE DARK-SILICON ERA**
Nishit Kapadia and Sudeep Pasricha, Colorado State University, US

IPS **IP4-7, IP4-8**

1930 **DATE PARTY**
in Museum of Grenoble (Musée de Grenoble, 5 Place de Lavalette, 38000 Grenoble, France)

8.8 Share a Fab - Multi Project Wafers Enable Your Innovations

Salle Lesdiguières 1700 - 1830

Moderator: **Jürgen Haase,** edacentrum GmbH, DE

Today most innovations in the major industries include the use of dedicated chips. However, extremely high IC fabrication costs and foundries accepting only orders with high quantities are substantial obstacles for innovations developed from SMEs, start-ups, universities and research organisations.

The solution is that many of these innovators team up and share a fab run by using the opportunities offered by Multi Project Wavers (MPWs). European service providers like Europractice and CMP provide the access to MPW runs as well as the required know-how and tooling.

In the tutorial part of this session first-time users as well as experienced users will be provided with comprehensive information about the available semiconductor technologies, new design methodologies and possible applications. In the best practice part of the session users of such services will share their experience with the MPW concept with the audience and present projects and products realized by utilizing MPW opportunities.

1700 **INTRODUCTION**
Jürgen Haase, edacentrum GmbH, DE

1705 **THE EUROPRACTICE MPW SERVICE AS AN ENABLER FOR LOW COST ASIC PROTOTYPING FOR R&D AND PRODUCT DEVELOPMENT**
Carl Das, IMEC/Europractice, BE

1725 **CMP MPW SERVICES FOR IC PROTOTYPING AND LOW VOLUME PRODUCTION**
Jean-Christophe Crébier, CMP, FR

1745 **THE ASSOCIATIVE MEMORY ASIC DEVELOPMENT FOR HIGH ENERGY PHYSICS SINCE 2003 TO 2015, IMPORTANCE OF IMEC SUPPORT**
Alberto Annovi, INFN Pisa, IT
Paola Giannetti, INFN Pisa, IT

1800 **A FEEDBACK FROM MPW USER**
Paul Hyland, Microelectronic Circuit Centre Ireland (MCCI), IE

1815 **DISCUSSION**

1930 **DATE PARTY**
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9.1 SPECIAL DAY Hot Topic: Game-changing Innovative Technology Platforms for Health Care

Salle Oisans 0830 - 1000

Organiser: **Jo De Boeck,** IMEC, BE
Chair: **Jo De Boeck,** IMEC, BE

After an introductory talk on the future impact of electronics in health care innovation, the panel of experts from industry will discuss the main trends they see and the challenges this presents for technology and care providers.

0830 **GAME CHANGING INNOVATION IN TECHNOLOGY AND DESIGN FOR EFFECTIVE HEALTH CARE**
Chris Van Hoof, IMEC, BE

0900 **ADVANCED SELF-POWERED SYSTEMS OF INTEGRATED SENSORS AND TECHNOLOGIES**
Veena Misra, ASSIST, NC State University, US

0930 **HEALTHCARE IN AN INTEGRATED DIGITAL WORLD**
Jean-Paul Linnartz, Philips, NL

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.2 Hot Topic - Transparent Use of Accelerators in Heterogeneous Computing Systems

Belle-Etoile 0830 - 1000

Organisers: **Christian Plessl,** University of Paderborn, DE
Heiner Giefers, IBM Research Zurich, CH
Chair: **Christian Plessl,** University of Paderborn, DE
Co-Chair: **Heiner Giefers,** IBM Research Zurich, CH

This hot topic session discusses recent research for transparent compilation and offloading of computational hotspots from CPUs to accelerators, in particular, many-core processors and FPGAs. The overarching objective of these approaches is to make the performance and energy-efficiency benefits of heterogeneous computing available to a broader spectrum of applications and users by reducing or even obviating the effort for porting applications.

0830 **TRANSPARENT ACCELERATION OF PROGRAM EXECUTION USING RECONFIGURABLE HARDWARE**
Nuno Paulino[1], João Canas Ferreira[1], João Bispo[2] and João M. P. Cardoso[2]
[1]INESC TEC and Faculty of Engineering, PT; [2]University of Porto, PT

0852 **ACCELERATING ARITHMETIC KERNELS WITH COHERENT ATTACHED FPGA COPROCESSORS**
Heiner Giefers, Raphael Polig and Christoph Hagleitner, IBM Research Zurich, CH

0915 **TRANSPARENT OFFLOADING OF COMPUTATIONAL HOTSPOTS FROM BINARY CODE TO XEON PHI**
Marvin Damschen[1], Heinrich Riebler[2], Gavin Vaz[2] and Christian Plessl[2]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]University of Paderborn, DE

0937 **TRANSPARENT LINKING OF COMPILED SOFTWARE AND SYNTHESIZED HARDWARE**
David Thomas[1], Shane T. Fleming[1], George A. Constantinides[1] and Dan R. Ghica[2]
[1]Imperial College London, GB; [2]University of Birmingham, GB

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.3 NoC Optimization

Stendhal 0830 - 1000

Chair: **Marcello Coppola,** STMicroelectronics, FR
Co-Chair: **José Flich,** Universidad Politecnica de Valencia, ES

As NoCs are becoming mature technology, the time is coming to develop sophisticated system-level optimization techniques. In this session, several distinct optimization techniques are addressed. The first paper presents a

novel approach to traffic isolation, the second paper deals with power-saving technique exploration and the final paper develops customized NoCs for emerging biomedical applications.

0830 **PHASENOC: TDM SCHEDULING AT THE VIRTUAL-CHANNEL LEVEL FOR EFFICIENT NETWORK TRAFFIC ISOLATION**
Anastasios Psarras[1], Ioannis Seitanidis[1], Chrysostomos Nicopoulos[2] and Giorgos Dimitrakopoulos[1]
[1]Democritus University of Thrace, GR; [2]University of Cyprus, CY

0900 **RATE-BASED VS DELAY-BASED CONTROL FOR DVFS IN NOC**
Mario R. Casu and Paolo Giaccone, Politecnico di Torino, Department of Electronics and Telecommunications, IT

0930 **NOC-ENABLED MULTICORE ARCHITECTURES FOR STOCHASTIC ANALYSIS OF BIOMOLECULAR REACTIONS**
Turbo Majumder[1], Xian Li[2], Paul Bogdan[3] and Partha Pande[2]
[1]Indian Institute of Technology Delhi, IN; [2]Washington State University, US; [3]University of Southern California, US

IPS **IP4-9, IP4-10**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.4 Advanced Trends in Alternative Technologies

Chartreuse 0830 - 1000

Chair: **Martin Trefzer,** University of York, GB
Co-Chair: **Yvain Thonnart,** CEA-Leti, FR

As technology evolves, "information" is no longer limited to charge-based representations of 1s and 0s. In this session, the first presented paper discusses work where qubits are stored as the internal states of an atomic ion. The second presentation considers labs on chip — where reactants are moved through valves and channels to solve problems such as protein analysis, disease diagnosis, etc. Finally, the last presentation discusses the use of optical waveguides to move data from point-to-point, thus eliminating higher latency electrical interconnect.

0830 **OPTIMIZATION OF QUANTUM COMPUTER ARCHITECTURE USING A RESOURCE-PERFORMANCE SIMULATOR**
Muhammad Ahsan and Jungsang Kim, Duke University, US

0900 **VOLUME-ORIENTED SAMPLE PREPARATION FOR REACTANT MINIMIZATION ON FLOW-BASED MICROFLUIDIC BIOCHIPS WITH MULTI-SEGMENT MIXERS**
Chi-Mei Huang[1], Chia-Hung Liu[2] and Juinn-Dar Huang[1]
[1]Department of Electronics Engineering, National Chiao Tung University, TW; [2]National Chiao Tung University, TW

0930 **THERMAL AWARE DESIGN METHOD FOR VCSEL-BASED ON-CHIP OPTICAL INTERCONNECT**
Hui Li[1], Alain Fourmigue[2], Sébastien Le Beux[1], Xavier Letartre[1], Ian O'Connor[1] and Gabriela Nicolescu[2]
[1]Ecole Centrale de Lyon, FR; [2]Ecole Polytechnique de Montréal, CA

IPS **IP4-11, IP4-12**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.5 Modeling and Simulation of Extra-Functional Properties

Meije 0830 - 1000

Chair: **Sylvian Kaiser,** DOCEA Power, FR
Co-Chair: **Sander Stuijk,** TU Eindhoven, NL

This session deals with modeling and simulating extra-functional system properties. The first paper presents a framework to accurately model the power and timing of hardware models without requiring a full micro-architectural simulation of the hardware module to extract signal transitions. The second paper presents a method to extend Design Space Exploration (DSE) of

systems with Out-of-Order execution by accurately predicting the performance of CPUs with different cache configurations within reasonable time. The third paper is about an approach that constructs a learning-based thermal model for a given (black-box) multi-core processor running a given application mix.

0830 **DYNAMIC POWER AND PERFORMANCE BACK-ANNOTATION FOR FAST AND ACCURATE FUNCTIONAL HARDWARE SIMULATION**
Dongwook Lee, Lizy Kurian John and Andreas Gerstlauer, The University of Texas at Austin, US

0900 **FAST AND PRECISE CACHE PERFORMANCE ESTIMATION FOR OUT-OF-ORDER EXECUTION**
Roeland Douma, Sebastian Altmeyer and Andy Pimentel, University of Amsterdam, NL

0930 **A CALIBRATION BASED THERMAL MODELING TECHNIQUE FOR COMPLEX MULTICORE SYSTEMS**
Devendra Rai and Lothar Thiele, Swiss Federal Institute of Technology in Zurich (ETHZ), CH

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.6 Design, Synthesis and Validation of Analog Circuits

Bayard 0830 - 1000

Chair: **Marie-Minerve Louerat,** LIP6/CNRS, FR
Co-Chair: **Georges Gielen,** ESAT - KU Leuven, BE

The session presents new synthesis and validation approaches to analog circuit design. Two design papers shade new light on Tunnel FETs and an ADC.

0830 **KNOWLEDGE-INTENSIVE, CAUSAL REASONING FOR ANALOG CIRCUIT TOPOLOGY SYNTHESIS IN EMERGENT AND INNOVATIVE APPLICATIONS**
Alex Doboli, Fanshu Jiao and Sergio Montano, State University of New York at Stony Brook, US

0900 **A CNN-INSPIRED MIXED SIGNAL PROCESSOR BASED ON TUNNEL TRANSISTORS**
Behnam Sedighi, Indranil Palit, Xiaobo Sharon Hu and Michael Niemier, University of Notre Dame, US

0930 **LAYOUT-AWARE SIZING OF ANALOG ICS USING FLOORPLAN & ROUTING ESTIMATES FOR PARASITIC EXTRACTION**
Nuno Lourenco, Ricardo Martins and Nuno Horta, Instituto de Telecomunicações, Instituto Superior Técnico – TU Lisbon, PT

0945 **INITIAL TRANSIENT RESPONSE OF OSCILLATORS WITH LONG SETTLING TIME**
Hans-Georg Brachtendorf and Bittner Kai, University of Applied Sciences of Upper Austria, AT

IPS **IP4-14, IP4-15, IP4-16, IP4-17**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.7 Test Generation, Fault Simulation and Diagnosis

Les Bans 0830 - 1000

Chair: **Jacob Abraham,** The University of Texas at Austin, US
Co-Chair: **Bernd Becker,** University Freiburg, DE

Speeding-up the test process is crucial from a technical and economical point of view. Novel methods are presented to accelerate silicon debug, fault simulation, test generation and diagnosis.

0830 **QUICK ERROR DETECTION TESTS WITH FAST RUNTIMES FOR EFFECTIVE POST-SILICON VALIDATION AND DEBUG**
David Lin[1], Eswaran S[2], Sharad Kumar[2], Eric Rentschler[3] and Subhasish Mitra[1]
[1]Stanford University, US; [2]Freescale Semiconductor, IN; [3]Advanced Micro Devices, US

0900 **GPU-ACCELERATED SMALL DELAY FAULT SIMULATION**
Eric Schneider[1], Stefan Holst[2], Michael Kochte[1], Xiaoqing Wen[2] and Hans-Joachim Wunderlich[1]
[1]University of Stuttgart, DE; [2]Kyushu Institute of Technology, JP

0930 **FAULT SIMULATION WITH PARALLEL EXACT CRITICAL PATH TRACING IN MULTIPLE CORE ENVIRONMENT**
Maksim Gorev, Raimund Ubar and Sergei Devadze, Tallinn University of Technology, EE

0945 **ON THE AUTOMATIC GENERATION OF SBST TEST PROGRAMS FOR IN-FIELD TEST**
Andreas Riefert[1], Riccardo Cantoro[2], Matthias Sauer[1], Matteo Sonza Reorda[2] and Bernd Becker[1]
[1]University of Freiburg, DE; [2]Politecnico di Torino, IT

IPS **IP4-18, IP4-19, IP4-20, IP4-21**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.8 Hot Topic - Monolithic 3D: A Path to Real 3D Integrated Chips

Salle Lesdiguières 0830 - 1000

Organisers: **Pierre-Emmanuel Gaillardon,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH
Chair: **Giovanni De Micheli,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Co-Chair: **Ian O'Connor,** Institut des Nanotechnologies de Lyon, FR

As compared to standard 3D technologies, 3D Monolithic Integration (3DMI) overcomes the vertical connectivity challenge through the use of nano-scale inter-layer vias, which are orders-of-magnitude smaller than TSVs. In this hot topic session, we cover 3DMI for actual (FDSOI) and emerging (CNFETs and RRAM) technologies, and identify its promises from a design perspective.

0830 **A COMPREHENSIVE STUDY OF MONOLITHIC 3D CELL ON CELL DESIGN USING COMMERCIAL 2D TOOL**
Olivier Billoint[1], Hossam Sarhan[1], Iyad Rayane[2], Maud Vinet[1], Perrine Batude[1], Claire Fenouillet-Beranger[1], Olivier Rozeau[1], Gérald Cibrario[1], Fabien Deprat[1], Aurélien Fustier[1], Jean-Eric Michallet[1], Olivier Faynot[1], Ogun Turkyilmaz[1], Jean-Frederic Christmann[1], Sébastien Thuries[1] and Fabien Clermidy[1]
[1]CEA-Leti, FR; [2]Mentor Graphics, FR

0900 **MONOLITHIC 3D INTEGRATION: A PATH FROM CONCEPT TO REALITY**
Max M. Shulaker, Tony F. Wu, Mohamed M. Sabry, Hai Wei, H.-S. Philip Wong and Subhasish Mitra, Stanford University, US

0930 **A ULTRA-LOW-POWER FPGA BASED ON MONOLITHICALLY INTEGRATED RRAMS**
Pierre-Emmanuel Gaillardon, Xifan Tang, Jury Sandrini, Maxime Thammasack, Somayyeh Rahimian Omam, Davide Sacchetto, Yusuf Leblebici and Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH

1000 **COFFEE BREAK IN EXHIBITION AREA**

IP4 Interactive Presentations, sponsored by Cadence Academic Network

1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP4-1 **PWL: A PROGRESSIVE WEAR LEVELING TO MINIMIZE DATA MIGRATION OVERHEADS FOR NAND FLASH DEVICES**
Fu-Hsin Chen[1], Ming-Chang Yang[2], Yuan-Hao Chang[3] and Tei-Wei Kuo[4]
[1]Department of Computer Science and Information Engineering, National Taiwan University, TW; [2]Graduate Institute of Networking and Multimedia, National Taiwan University, TW; [3]Institute of Information Science, Academia Sinica, TW; [4]Academia Sinica & National Taiwan University, TW

IP4-2 **TOWARDS TRUSTABLE STORAGE USING SSDS WITH PROPRIETARY FTL**
Xiaotong Cui[1], Minhui Zou[1], Liang Shi[2] and Kaijie Wu[1]
[1]Chongqing University, CN; [2]College of Computer Science, Chongqing University, CN

IP4-3 **USER-SPECIFIC SKIN TEMPERATURE-AWARE DVFS FOR SMARTPHONES**
Begum Birsen Egilmez[1], Gokhan Memik[1], Seda Ogrenci-Memik[1] and Oğuz Ergin[2]
[1]Northwestern University, US; [2]TOBB University of Economics and Technology, TR

IP4-4 **FORMAL PROBABILISTIC ANALYSIS OF DISTRIBUTED DYNAMIC THERMAL MANAGEMENT**
Shafaq Iqtedar[1], Osman Hasan[2], Muhammad Shafique[3] and Joerg Henkel[3]
[1]National University of Sciences and Technology (NUST), Islamabad, PK; [2]National University of Sciences and Technology (NUST), Islamabad, ; [3]Karlsruhe Institute of Technology (KIT), DE

IP4-5 **A HYBRID QUASI MONTE CARLO METHOD FOR YIELD AWARE ANALOG CIRCUIT SIZING TOOL**
Engin Afacan, Günhan Dündar, Gonenc Berkol, Ali Emre Pusane and İsmail Faik Baskaya, Bogazici University, TR

IP4-6 **FEATURE SELECTION FOR ALTERNATE TEST USING WRAPPERS: APPLICATION TO AN RF LNA CASE STUDY**
Manuel Barragan[1] and Gildas Leger[2]
[1]TIMA Laboratory, FR; [2]Instituto de Microelectronica de Sevilla, IMSE-CNM, (CSIC - Universidad de Sevilla), ES

IP4-7 **IMPROVING SIMD CODE GENERATION IN QEMU**
Sheng-Yu Fu[1], Jan-Jan Wu[2] and Wei-Chung Hsu[1]
[1]Department of Computer Science National Taiwan University, TW; [2]Institute of Information Science Academia Sinica, TW

IP4-8 **REUSE DISTANCE ANALYSIS FOR LOCALITY OPTIMIZATION IN LOOP-DOMINATED APPLICATIONS**
Christakis Lezos, Grigoris Dimitroulakos and Konstantinos Masselos, University of Peloponnese, GR

IP4-9 **TAPP: TEMPERATURE-AWARE APPLICATION MAPPING FOR NOC-BASED MANY-CORE PROCESSORS**
Di Zhu, Lizhong Chen, Timothy Pinkston and Massoud Pedram, University of Southern California, US

IP4-10 **MALLEABLE NOC: DARK SILICON INSPIRED ADAPTABLE NETWORK ON CHIP**
Haseeb Bokhari[1], Haris Javaid[2], Muhammad Shafique[3], Joerg Henkel[3] and Sri Parameswaran[1]
[1]University of New South Wales, AU; [2]Google Inc., ; [3]Karlsruhe Institute of Technology (KIT), DE

IP4-11 **TOPOLOGY IDENTIFICATION FOR SMART CELLS IN MODULAR BATTERIES**
Sebastian Steinhorst and Martin Lukasiewycz, TUM CREATE, SG

IP4-12 **LVS CHECK FOR PHOTONIC INTEGRATED CIRCUIT - CURVILINEAR FEATURE EXTRACTION AND VALIDATION**
Ruping Cao[1], Julien Billoudet[1], John Ferguson[1], Lionel Couder[2], John Cayo[2], Alexandre Arriordaz[1] and Ian O'Connor[3]
[1]Mentor Graphics Corp, FR; [2]Mentor Graphics Corp, US; [3]Lyon Institute of Nanotechnology, FR

IP4-13 **FP-SCHEDULING FOR MODE-CONTROLLED DATAFLOW: A CASE STUDY**
Alok Lele[1], Orlando Moreira[2] and Kees van Berkel[2]
[1]Eindhoven University of Technology, NL; [2]Ericsson B.V., NL

IP4-14 **AGEING SIMULATION OF ANALOGUE CIRCUITS AND SYSTEMS USING ADAPTIVE TRANSIENT EVALUATION**
Felix Salfelder and Lars Hedrich, Goethe-Universitat Frankfurt a. M., DE

IP4-15 **A TOOL FOR THE ASSISTED DESIGN OF CHARGE REDISTRIBUTION SAR ADCS**
Stefano Brenna[1], Andrea Bonetti[2], Andrea Bonfanti[1] and Andrea L. Lacaita[1]
[1]Politecnico di Milano, IT; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH

IP4-16 **DETECTION OF ASYMMETRIC AGING-CRITICAL VOLTAGE CONDITIONS IN ANALOG POWER-DOWN MODE**
Michael Zwerger and Helmut Graeb, Technische Universitaet Muenchen, DE

IP4-17 **HIGH PERFORMANCE SINGLE SUPPLY CMOS INVERTER LEVEL UP SHIFTER FOR MULTI–SUPPLY VOLTAGES DOMAINS**
José-C. García[1], Juan A. Montiel-Nelson[1], J. Sosa[1] and Saeid Nooshabadi[2]
[1]Institute for Applied Microelectronics, ES; [2]Department of Electrical and Computer Engineering of Michigan Technological University, US

IP4-18 **EXPLORING THE IMPACT OF FUNCTIONAL TEST PROGRAMS RE-USED FOR POWER-AWARE TESTING**
Aymen Touati[1], Alberto Bosio[2], Luigi Dilillo[2], Patrick Girard[2], Arnaud Virazel[2], Paolo Bernardi[3] and Mateo Sonza Reorda[3]
[1]LIRMM, FR; [2]LIRMM-UM2/CNRS, FR; [3]Politecnico di Torino, IT

IP4-19 **A BREAKPOINT-BASED SILICON DEBUG TECHNIQUE WITH CYCLE-GRANULARITY FOR HANDSHAKE-BASED SOC**
Hsin-Chen Chen[1], Chen-Rong Wu[1], Katherine Shu-Min Li[2] and Kuen-Jon Lee[1]
[1]National Cheng Kung University, TW; [2]National Sun Yat-sen University, TW

IP4-20 **FAULT DIAGNOSIS IN DESIGNS WITH EXTREME LOW PIN TEST DATA COMPRESSORS**
Subhadip Kundu[1], Parthajit Bhattacharya[1] and Rohit Kapur[2]
[1]Synopsys India, IN; [2]Synopsys Inc., US

IP4-21 **OPTIMIZING DYNAMIC TRACE SIGNAL SELECTION USING MACHINE LEARNING AND LINEAR PROGRAMMING**
Charlie Shucheng Zhu and Sharad Malik, Princeton University, US

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.1 SPECIAL DAY Hot Topic: Wearable Medical Applications

Salle Oisans 1100 - 1230

Organiser: **Jo De Boeck,** IMEC, BE
Chair: **Renzo Dal Molin,** Sorin Group, FR
Co-Chair: **Chris Van Hoof,** IMEC, BE

Wearable devices are hot. This session will treat opportunities in technology and application for devices that assist in prevention and monitoring in selected cases.

1100 **MOBILE HEALTH MONITORING: ADOPTION AND SYSTEM CHALLENGES**
David Shanes, BioTelemetry, Inc., US

1130 **WEARABLE DEVICE FOR PHYSICAL AND EMOTIONAL HEALTH MONITORING**
Srinivasan Murali, SmartCardia, CH

1200 **GAIT ANALYSIS FOR FALL PREDICTION USING HIERARCHICAL TEXTILE-BASED CAPACITIVE SENSOR ARRAYS**
Rebecca Baldwin, University of Maryland, Baltimore County, US
Rebecca Baldwin, Stanislav Bobovych, Ryan Robucci, Nilanjan Banerjee and Chintan Patel, University of Maryland, Baltimore County, US

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.2 Emerging Memory Architectures

Belle-Etoile 1100 - 1230

Chair: **Luca Perniola,** CEA-Leti, FR
Co-Chair: **Pierre-Emmanuel Gaillardon,** École Polytechnique Fédérale de Lausanne (EPFL), CH

Memories are of utmost importance in modern electronic systems. Emerging memory technologies hold a lot of promise to further integration density and performance levels, while reducing energy consumption. In this session, the first two papers introduce innovative solutions for better control of the endurance limitations of novel memories, while the last two papers investigate the gains in performance metrics from a system-level perspective.

1100 **HRERAM: A HYBRID RECONFIGURABLE RESISTIVE RANDOM-ACCESS MEMORY**
Miguel Angel Lastras-Montaño, Amirali Ghofrani and Kwang-Ting Cheng, UCSB, US

1130 **NCODE: LIMITING HARMFUL WRITES TO EMERGING MOBILE NVRAM THROUGH CODE SWAPPING**
Kan Zhong, Duo Liu, Linbo Long, Xiao Zhu, Weichen Liu, Qingfeng Zhuge and Edwin Sha, Chongqing University, CN

1200 **SYSTEM LEVEL EXPLORATION OF A STT-MRAM BASED LEVEL 1 DATA-CACHE**
Manu Komalan[1], Jose Ignacio Gomez[2], Christian Tenllado[2], Francisco Tirado Fernandez[2] and Francky Catthoor[3]
[1]imec, UCM(Universidad Complutense de Madrid), ES; [2]Universidad Complutense de Madrid, ES; [3]IMEC, BE

1215 **HIGH PERFORMANCE AXI-4.0 BASED INTERCONNECT FOR EXTENSIBLE SMART MEMORY CUBES**
Erfan Azarkhish[1], Igor Loi[1], Davide Rossi[1] and Luca Benini[2]
[1]University of Bologna, IT; [2]Università di Bologna / Swiss Federal Institute of Technology in Zurich (ETHZ), CH

IPS **IP5-1, IP5-2**

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.3 Modern Architectures for Real-Time Systems

Stendhal 1100 - 1230

Chair: **Benny Akesson,** Czech Technical University in Prague, CZ
Co-Chair: **Rodolfo Pellizzoni,** University of Waterloo, CA

Introducing modern architectures, such as multicore platforms, in real-time systems is challenging. The papers in this session make a contribution in this direction by discussing new scheduling techniques for parallel real-time tasks, multicore architectures, and mixed-criticality systems.

1100 **THE FEDERATED SCHEDULING OF CONSTRAINED-DEADLINE SPORADIC DAG TASK SYSTEMS**
Sanjoy Baruah, The University of North Carolina at Chapel Hill, US

1130 **RUN AND BE SAFE: MIXED-CRITICALITY SCHEDULING WITH TEMPORARY PROCESSOR SPEEDUP**
Pengcheng Huang, Pratyush Kumar, Georgia Giannopoulou and Lothar Thiele, Swiss Federal Institute of Technology in Zurich (ETHZ), CH

1200 **MULTI-CORE FIXED-PRIORITY SCHEDULING OF REAL-TIME TASKS WITH STATISTICAL DEADLINE GUARANTEE**
Tianyi Wang[1], Linwei Niu[2], Shaolei Ren[1] and Gang Quan[1]
[1]Florida International University, US; [2]West Virginia State University, US

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.4 Energy Aware Data Center: Design and Management

Chartreuse 1100 - 1230

Chair: **Carlo Cavazzoni,** Cineca, IT
Co-Chair: **Andreas Burg,** École Polytechnique Fédérale de Lausanne (EPFL), CH

The session covers various topics in improving data center energy efficiency, from hardware acceleration, scheduling to cooling.

1100 **MEMORY FAST-FORWARD: A LOW COST SPECIAL FUNCTION UNIT TO ENHANCE ENERGY EFFICIENCY IN GPU FOR BIG DATA PROCESSING**
Eunhyeok Park[1], Junwhan Ahn[2], Sungpack Hong[3], Sungjoo Yoo[1] and Sunggu Lee[1]
[1]POSTECH, KR; [2]SNU, KR; [3]Oracle, US

1130 **POWER MINIMIZATION FOR DATA CENTER WITH GUARANTEED QOS**
Shuo Liu[1], Soamar Homsi[1], Ming Fan[1], Shaolei Ren[1], Gang Quan[1] and Shangping Ren[2]
[1]Florida International University, US; [2]Illinois Institute of Technology, US

1200 **ENERGY-AWARE COOLING FOR HOT-WATER COOLED SUPERCOMPUTERS**
Christian Conficoni[1], Andrea Bartolini[2], Andrea Tilli[1], Gianpietro Tecchiolli[3] and Luca Benini[2]
[1]Università di Bologna, IT; [2]Università di Bologna / ETH Zürich, IT; [3]Eurotech, IT

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.5 Reconfigurable Architectures and Applications

Meije 1100 - 1230

Chair: **Christian Plessl,** University of Paderborn, DE
Co-Chair: **Enno Lübbers,** Intel Labs Europe, DE

Reconfigurable computing has vast potential for enhancing the performance of applications especially when using architectural optimizations. This session has two papers that focus on architectural enhancements while the third demonstrates a hardware accelerated bioinformatics application

1100 **HYBRID ADAPTIVE CLOCK MANAGEMENT FOR FPGA PROCESSOR ACCELERATION**
Alexandru Gheolbanoiu[1], Lucian Petrica[1] and Sorin Cotofana[2]
[1]University POLITEHNICA of Bucharest, RO; [2]Delft University of Technology, NL

1130 **A SCALABLE AND HIGH-DENSITY FPGA ARCHITECTURE WITH MULTI-LEVEL PHASE CHANGE MEMORY**
Chunan Wei, Ashutosh Dhar and Deming Chen, University of Illinois, Urbana-Champaign, US

1200 **FPGA ACCELERATED DNA ERROR CORRECTION**
Anand Ramachandran, Yun Heo, Wen-mei Hwu, Jian Ma and Deming Chen, University of Illinois at Urbana-Champaign, US

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.6 Circuit Design and Test: From Characterization to Measurement

Bayard 1100 - 1230

Chair: **Salvador Mir,** TIMA/CNRS, FR
Co-Chair: **Christoph Grimm,** TU Kaiserslautern, DE

This session covers eye-diagram analysis for high-speed circuits, statistical digital library characterization, analog test ordering in the context of muti-site testing, and estimation of defect detection probability of analog test.

1100 **FAST EYE DIAGRAM ANALYSIS FOR HIGH-SPEED CMOS CIRCUITS**
Seyed Nematollah Ahmadyan[1], Chenjie Gu[2], Suriyaprakash Natarajan[2], Eli Chiprout[2] and Shobha Vasudevan[1]
[1]University of Illinois at Urbana-Champaign, US; [2]Intel, US

1130 **STATISTICAL LIBRARY CHARACTERIZATION USING BELIEF PROPAGATION ACROSS MULTIPLE TECHNOLOGY NODES**
Li Yu[1], Sharad Saxena[2], Christopher Hess[2], Ibrahim Elfadel[3], Dimitri Antoniadis[1] and Duane Boning[1]
[1]Massachusetts Institute of Technology, US; [2]PDF Solutions, Inc, US; [3]Masdar Institute of Science and Technology, AE

1200 **COMBINING ADAPTIVE ALTERNATE TEST AND MULTI-SITE**
Gildas Leger, Instituto de Microelectronica de Sevilla, IMSE-CNM, (CSIC - Universidad de Sevilla), ES

1215 **A METHOD FOR THE ESTIMATION OF DEFECT DETECTION PROBABILITY OF ANALOG/RF DEFECT-ORIENTED TESTS**
John Liaperdos[1], Angela Arapoyanni[2] and Yiorgos Tsiatouhas[3]
[1]Technological Educational Institute of Peloponnese, Dept of Computer Engineering, GR; [2]National and Kapodistrian University of Athens, Dept. of Informatics and Telecommunications, GR; [3]University of Ioannina, GR

IPS **IP5-5, IP5-6**

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.7 Expanding the Applicability of Formal Methods

Les Bans 1100 - 1230

Chair: **Barbara Jobstmann,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Co-Chair: **Christoph Scholl,** University Freiburg, DE

The first two papers propose improved solutions for error diagnosis and software bounded model checking. The next two papers are devoted to abstraction and synthesis techniques between RTL and high-level models of on-chip communication networks. Then the first IP expands the applicability of equivalence checkers to asynchronous circuits. The last two IPs present emerging applications of model checking.

1100 **AUTOMATED RECTIFICATION METHODOLOGIES TO FUNCTIONAL STATE-SPACE UNREACHABILITY**
Ryan Berryhill and Andreas Veneris, University of Toronto, CA

1130 **OVER-APPROXIMATING LOOPS TO PROVE PROPERTIES USING BOUNDED MODEL CHECKING**
Priyanka Darke, Bharti Chimdyalwar, Venkatesh R, Ulka Shrotri and Ravindra Metta, TCS, IN

1200 **AUTOMATIC EXTRACTION OF MICRO-ARCHITECTURAL MODELS OF COMMUNICATION FABRICS FROM REGISTER TRANSFER LEVEL DESIGNS**
Sebastiaan Joosten and Julien Schmaltz, Eindhoven University of Technology, NL

1215 **GALS SYNTHESIS AND VERIFICATION FOR XMAS MODELS**
Frank Burns, Danil Sokolov and Alex Yakovlev, Newcastle University, GB

IPS **IP5-7, IP5-8, IP5-9**

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

10.8 From IP to EDA Tools Enterprise Management: What is so special?

Salle Lesdiguières 1100 - 1230

Moderator: **Gabrièle Saucier,** Design and Reuse, FR
Panelists: **Huy-Nam Nguyen,** Bull S.A.S., FR
Philippe Quinio, STMicroelectronics International, CH

IPs are today part of any Electronic Systems and it is more and more urgent to trace, monitor and more generally "manage" IPs in systems or products. The key feature of such a management is its multidisciplinary facet implying multiple management views and actors (IP Engineering, IP Sourcing, IP Procurement..).

Today an IP management platform needs to be a next generation web application hosted on an intranet server and receiving data from multiple sources (Design DB, IP Delivery DB, Product Shipment DB, Legal and Financial reports..). It aims at providing a reliable follow up to all of these departments such as IP Entry, IP Delivery, IP tracing in products… It delivers results (fee and royalty calculation for instance) as well as expertise for decision making (planning the future in terms of IP expenses, cost per product..).

The introductory talk will show how such a portal can be configured to fulfill the needs of an enterprise and what are the required "special" technical features missing in management tools presently available on the market.

Specific views namely Engineering view and Legal aspects will be commented by 2 speakers from companies veteran in IP management.

It will also be demonstrated that an amazing and straightforward extension concerns EDA Tool license management and optimization including integrated license monitoring. Such an extension aims at optimizing the tool cost for large enterprises using extensively and at a large scale a variety of development tools and gives an unique corporate global view on IP and Tools.

1100 **IP AND EDA TOOL NEXT GENERATION MANAGEMENT PLATFORM: WHAT ARE THE FEATURES REQUIRED?**
Gabrièle Saucier, Design and Reuse, FR

1130 **BEST PRACTICE: THE IP QUALIFICATION VIEW**
Huy-Nam Nguyen, Bull S.A.S., FR

1145 **BUSINESS AND LEGAL: THE SOURCING RISK**
Philippe Quinio, STMicroelectronics International, CH

1205 **QUESTIONS AND AUDIENCE COMMENTS**

1230 **LUNCH BREAK,**
in Les Écrins
Keynote lecture from 1320 - 1350 (Room Oisans)

11.0 SPECIAL DAY Keynote

1315 - 1350

Chair: **Jo De Boeck,** IMEC, BE
Co-Chair: **David Atienza,** École Polytechnique Fédérale de Lausanne (EPFL), CH

1315 **BEST IP AWARD PRESENTATION**
Oliver Bringmann, University of Tuebingen / FZI, DE

1320 **BIOELECTRONIC MEDICINES - HERALDING IN A NEW THERAPEUTIC APPROACH**
Kristoffer Famm, GSK, GB

11.1 SPECIAL DAY Hot Topic: Implantable Medical Applications

Salle Oisans 1400 - 1530

Organiser: **Jo De Boeck,** IMEC, BE
Chair: **Refet Firat Yazicioglu,** IMEC, BE
Co-Chair: **Jean-Paul Linnartz,** Philips, NL

Implantable devices obviously have stringent technical requirements dictated by the specific functionality in the body. This session brings expert views from industry leaders in the field and insight in the challenges for integrated circuits in emerging biomedical devices.

1400 **ACTIVE IMPLANTABLE MEDICAL DEVICES**
Renzo Dal Molin, Sorin Group, FR

1430 **TOWARDS NEXT GENERATION DEEP BRAIN STIMULATION**
Michael Decré, Medtronic Eindhoven Design Center, NL

1500 **INTEGRATED CIRCUITS AND MICROSYSTEMS FOR EMERGING BIOMEDICAL DEVICES**
Minkyu Je, DGIST, Daegu Gyeongbuk Institute of Science and Technology, KR

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.2 Variability and Robustness for Emerging Technologies

Belle-Etoile 1400 - 1530

Chair: **Edith Beigne,** CEA-Leti, FR
Co-Chair: **Andy Tyrrell,** University of York, GB

Issues relating to smaller device sizing and novel technologies require more consideration of variability when designing systems and the related robustness of such systems. The first paper in this session considers the modelling of resistive switching random access memory and used in a number of designs to illustrate various properties and characteristics of such devices, including speed-power performance, variability and a neuromorphic computing application. The second paper introduces methods for improving the performance of Spin-Torque Transfer RAM (STTRAM) to reduce worst-case write latency and improve power over more global methods. The third paper proposes a joint optimization of the reliability at device circuit and architecture level. The device level is mainly considered through the energy barrier, circuit level through the transistor controlling the writing current and the architecture level through the error code correction scheme complexity. The final paper in the session compare sub-10nm node TFETs against the projected FinFETs of the same node at 0.25V in both inverter chains and in synthesizing a LEON3 processor.

1400 **VARIATION-AWARE, RELIABILITY-EMPHASIZED DESIGN AND OPTIMIZATION OF RRAM USING SPICE MODEL**
Haitong Li[1], Zizhen Jiang[2], Peng Huang[3], Yi Wu[2], Hong-Yu Chen[2], Bin Gao[3], Xiaoyan Liu[3], Jinfeng Kang[3] and H.-S. Philip Wong[2]
[1]Stanford University & Peking University, ; [2]Stanford University, ; [3]Peking University,

1430 **IMPACT OF PROCESS-VARIATIONS IN STTRAM AND ADAPTIVE BOOSTING FOR ROBUSTNESS**
Seyedhamidreza Motaman, Swaroop Ghosh and Nitin Rathi, University of South Florida, US

1500 **DEVICE/CIRCUIT/ARCHITECTURE CO-DESIGN OF RELIABLE STT-MRAM**
Zoha Pajouhi, Xuanyao Fong and Kaushik Roy, Purdue University, US

1515 **SUB-10 NM FINFETS AND TUNNEL-FETS: FROM DEVICES TO SYSTEMS**
Ankit Sharma, Arun Goud Akkala and Kaushik Roy, Purdue University, US

IPS **IP5-10, IP5-11**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.3 Hot Topic - Multi/Many-Core Programming: Where Are We Standing?

Stendhal 1400 - 1530

Organisers: **Jeronimo Castrillon,** Technische Universität Dresden, DE
Rainer Leupers, RWTH Aachen, DE
Chair: **Norbert Wehn,** Technische Universität Kaiserslautern, DE
Co-Chair: **Ayse K. Coskun,** Boston University, US

Multi-processor systems have been in wide use for about ten years. During this time, several programming models have appeared in different domains. In particular, the academic community has been active in devising methods, often model-driven, to program heterogeneous embedded multi-processor platforms. This session analyzes the current standing from different perspectives, namely, from researchers working in methods in academia, from companies offering solutions and from companies requiring solutions.

1400 **5% OR 5X? THE PERFORMANCE GAP IN SIMD OPTIMIZATION, AND POSSIBLE SOLUTIONS**
Ben Juurlink, TU Berlin, DE

1415 **MODEL-BASED DESIGN OF REAL-TIME SYSTEMS**
Lothar Thiele, Swiss Federal Institute of Technology in Zurich (ETHZ), CH

1430 **PROGRAMMING ADAPTIVE AND ENERGY-EFFICIENT MANY-CORES**
Jeronimo Castrillon, Technische Universität Dresden, DE

1445 **CONFIDENCE IN THE USE OF SOFTWARE TOOLS ACCORDING TO THE ISO 26262 IN AUTOMOTIVE MULTICORE APPLICATIONS**
Ralph Jessenberger, BeOne Frankfurt GmbH, DE

1500 **AUTOMOTIVE MULTICORE MICROCONTROLLER SIMULATION, DEBUGGING AND ANALYSIS USING VIRTUAL PROTOTYPES**
Victor Reyes, Synopsys Inc., US

1515 **APPLYING MULTICORE COMPILER RESEARCH INTO INDUSTRIAL PRACTICES: AN EARLY EXPERIENCE REPORT**
Weihua Sheng, Silexica Software Solutions GmbH, DE

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.4 Logic Synthesis: the Faithful, the Approximate and the Stochastic

Chartreuse 1400 - 1530

Chair: **Alex Yakovlev,** University of Newcastle, GB
Co-Chair: **Mohamed Sabry,** Stanford University, US

Logic synthesis is evolving from traditional frameworks with fully-defined Boolean functions to account for the flexibilities afforded by observability don't cares, to generate smaller circuits through approximation and improve power-performance tradeoffs by taming stochastic computation.

1400 **A NEW APPROXIMATE ADDER WITH LOW RELATIVE ERROR AND CORRECT SIGN CALCULATION**
Junjun Hu[1] and Weikang Qian[2]
[1]Shanghai Jiao Tong University, CN; [2]Shanghai Jiao Tong University (SJTU), CN

1430 **TOWARDS BINARY CIRCUIT MODELS THAT FAITHFULLY CAPTURE PHYSICAL SOLVABILITY**
Matthias Fuegger[1], Robert Najvirt[1], Thomas Nowak[2] and Ulrich Schmid[1]
[1]TU Wien, AT; [2]École Normale Supérieure, FR

1500 **A COUPLING AREA REDUCTION TECHNIQUE APPLYING ODC SHIFTING**
Yi Diao[1], Tak-Kei Lam[2], Xing Wei[1] and Yu-Liang Wu[2]
[1]The Chinese University of Hong Kong, CN; [2]The Chinese University of Hong Kong, HK

1515 **A GENERAL DESIGN OF STOCHASTIC CIRCUIT AND ITS SYNTHESIS**
Zheng Zhao and Weikang Qian, Shanghai Jiao Tong University (SJTU), CN

IPS **IP5-12, IP5-13, IP5-14**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.5 Ultra-low Power Devices for Health and Rehabilitation

Meije 1400 - 1530

Chair: **Georgios Karakonstantis,** Queen's University, GB
Co-Chair: **José M. Moya,** Technical University of Madrid, ES

The session addresses scientific contribution in the field of ultra-low power devices and communication for medical, health and rehabilitation application. The first paper presents an innovative wearable device to assist writing rehabilitation. The next two papers cover different key aspects related to signal processing approaches for wireless compression and low-power coding for future Internet-of-Things (IoT) devices.

1400 **PAPER, PEN AND INK: AN INNOVATIVE SYSTEM AND SOFTWARE FRAMEWORK TO ASSIST WRITING REHABILITATION**
Leonardo Guardati[1], Filippo Casamassima[1], Elisabetta Farella[2] and Luca Benini[3]
[1]University of Bologna, IT; [2]Fondazione Bruno Kessler, IT; [3]Università di Bologna / Swiss Federal Institute of Technology in Zurich (ETHZ),

1430 **AN ALL-DIGITAL SPIKE-BASED ULTRA-LOW-POWER IR-UWB DYNAMIC AVERAGE THRESHOLD CROSSING SCHEME FOR MUSCLE FORCE WIRELESS TRANSMISSION**
Amirhossein Shahshahani[1], Masoud Shahshahani[1], Maurizio Martina[1], Guido Masera[1], Danilo Demarchi[2], Marco Crepaldi[3], Paolo Motto Ros[3] and Alberto Bonanno[3]
[1]Politecnico di Torino, IT; [2]Politecnico di Torino / Istituto Italiano di Tecnologia@PoliTo, IT; [3]Istituto Italiano di Tecnologia@PoliTo, IT

1500 **A PULSED-INDEX TECHNIQUE FOR SINGLE-CHANNEL, LOW-POWER, DYNAMIC SIGNALING**
Shahzad Muzaffar, Jerald Yoo, Ayman Shabra and Ibrahim (Abe) Elfadel, Masdar Institute of Science and Technology, AE

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.6 Video Architectures for Multimedia and Communications

Bayard 1400 - 1530

Chair: **Frederic Petro,** TIMA, FR
Co-Chair: **Marcello Coppola,** STMicroelectronics, FR

This session presents innovative work in video architectures and algorithms used in multimedia and communication systems.

1400 **SAPPHIRE: AN ALWAYS-ON CONTEXT-AWARE COMPUTER VISION SYSTEM FOR PORTABLE DEVICES**
Swagath Venkataramani[1], Victor Bahl[2], Xian-Sheng Hua[2], Jie Liu[2], Jin Li[2], Matthai Phillipose[2], Bodhi Priyantha[2] and Mohammed Shoaib[2]
[1]Purdue University, US; [2]Microsoft Research, US

1430 **APPROXIMATE ASSOCIATIVE MEMRISTIVE MEMORY FOR ENERGY-EFFICIENT GPUS**
Abbas Rahimi[1], Amirali Ghofrani[2], Kwang-Ting Cheng[2], Luca Benini[3] and Rajesh Gupta[1]
[1]UC San Diego, US; [2]UC Santa Barbara, US; [3]Università di Bologna / Swiss Federal Institute of Technology in Zurich (ETHZ), IT

1500 **PLATFORM-AWARE DYNAMIC CONFIGURATION SUPPORT FOR EFFICIENT TEXT PROCESSING ON HETEROGENEOUS SYSTEM**
Mi Sun Park[1], Omesh Tickoo[2], Vijaykrishnan Narayanan[1], Mary Jane Irwin[1] and Ravi Iyer[2]
[1]The Pennsylvania State University, US; [2]Intel Labs, US

1515 **A DEBLOCKING FILTER HARDWARE ARCHITECTURE FOR THE HIGH EFFICIENCY VIDEO CODING STANDARD**
Cláudio Diniz[1], Muhammad Shafique[2], Felipe Dalcin[1], Sergio Bampi[1] and Joerg Henkel[2]
[1]Federal University of Rio Grande do Sul (UFRGS), BR; [2]Karlsruhe Institute of Technology (KIT), DE

IPS **IP5-15, IP5-16**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.7 Exploiting Dark Silicon

Les Bans 1400 - 1530

Chair: **Olivier Heron,** CEA LIST, FR
Co-Chair: **Domenik Helms,** OFFIS, DE

The advent of the dark silicon area, raises the need for accurately, yet effectively regarding thermal properties of the system. Employing advanced power gating techniques will additionally raise the achievable gain. Both will be presented in this session.

1400 **MATEX: EFFICIENT TRANSIENT AND PEAK TEMPERATURE COMPUTATION FOR COMPACT THERMAL MODELS**
Santiago Pagani[1], Jian-Jia Chen[2], Muhammad Shafique[1] and Joerg Henkel[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]TU Dortmund, DE

1430 **DISTRIBUTED REINFORCEMENT LEARNING FOR POWER LIMITED MANY-CORE SYSTEM PERFORMANCE OPTIMIZATION**
Zhuo Chen and Diana Marculescu, Carnegie Mellon University, US

1500 **AN ENERGY-EFFICIENT VIRTUAL CHANNEL POWER-GATING MECHANISM FOR ON-CHIP NETWORKS**
Amirhossein Mirhosseini[1], Mohammad Sadrosadati[1], Ali Fakhrzadehgan[2], Mehdi Modarressi[3] and Hamid Sarbazi-Azad[1]
[1]Sharif University of Technology, IR; [2]University of Texas at Austin, US; [3]University of Tehran, IR

1515 **M-DTM: MIGRATION-BASED DYNAMIC THERMAL MANAGEMENT FOR HETEROGENEOUS MOBILE MULTI-CORE PROCESSORS**
Young Geun Kim, Minyong Kim, Jae Min Kim and Sung Woo Chung, Korea University, KR

IPS **IP5-17, IP5-18**

1530 **COFFEE BREAK IN EXHIBITION AREA**

THURSDAY 12 MARCH, 2015

DATE15
March 9 – 13, 2015, Grenoble, France
THU

11.8 Exhibition Keynote - Designing Systems for the Connected Autonomous Future: An Industry Perspective

Salle Lesdiguières 1400 - 1500

Organiser: **John Zhao,** MathWorks, US
Chair: **Jürgen Haase,** edacentrum GmbH, DE

Speaker to be announced in the online program.

Will I ever travel in an autonomous vehicle? Will my refrigerator really order food automatically from my grocery store? Can the watch I wear in the future warn me about an impending heart attack? Innovations at the SoC and board level are poised to provide the necessary computational power with low cost and high flexibility to make these products. However, designing the systems of the future -- whether an automobile, connected industrial machinery, medical device, consumer electronics, or an aerospace guidance system -- requires advances not only in embedded systems and software, but how they are designed and verified.

In this keynote, an expert from industry will discuss trends and innovations in systems that are incorporating more electronic content than ever before, and describe model-based development approaches that companies are using to create the system functionality that will power our connected autonomous future.

1400 **EXHIBITION KEYNOTE MATHWORKS**

1530 **COFFEE BREAK IN EXHIBITION AREA**

12.8 Tutorial: An Industry Approach to FPGA/ARM System Development and Verification

Salle Lesdiguières 1500 - 1730

Organiser: **John Zhao,** MathWorks, US

MATLAB and Simulink provide a rich environment for embedded-system development, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as MPSoC. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows. Functional verification throughout the design process improves coverage and test-case generation while reducing the time and resources required.

In this set of tutorial sessions, you will learn

- How to implement an application that leverages the FPGA and ARM core of a Zynq SOC
- The flexibility and diversity of the approach through examples that include prototyping a motor control algorithm and a video-processing algorithm.
- A HW/SW co-design workflow that combines system level design and simulation with automatic code generation
- Successful use of the HW/SW co-design workflow in commercial development
- Functional verification using MATLAB and Simulink in a SystemVerilog workflow illustrated by a detailed example

1500 **INTRODUCTION**

1505 **TUTORIAL, PART 1**

1600 **TUTORIAL, PART 2**

1645 **TUTORIAL, PART 3**

IP5 Interactive Presentations, sponsored by Cadence Academic Network

1530 - 1600

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP5-1 TOWARDS SYSTEMATIC DESIGN OF 3D PNML LAYOUTS

Robert Perricone[1], Yining Zhu[2], Katherine Sanders[1], X. Sharon Hu[1] and Michael Niemier[1]
[1]University of Notre Dame, US; [2]Zhejiang University, CN

IP5-2 DESTINY: A TOOL FOR MODELING EMERGING 3D NVM AND EDRAM CACHES

Matt Poremba[1], Sparsh Mittal[2], Dong Li[2], Jeffrey Vetter[3] and Yuan Xie[4]
[1]Pennsylvania State University, US; [2]Oak Ridge National Lab, US; [3]Oak Ridge National Lab and Georgia Institute of Technology, US; [4]University of California, Santa Barbara, US

IP5-3 BIG-DATA STREAMING APPLICATIONS SCHEDULING WITH ONLINE LEARNING AND CONCEPT DRIFT DETECTION

Karim Kanoun[1] and Mihaela van der Schaar[2]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]University of California, Los Angeles, US

IP5-4 DESIGN FLOW AND RUN-TIME MANAGEMENT FOR COMPRESSED FPGA CONFIGURATIONS

Christophe Huriaux[1], Antoine Courtay[1] and Olivier Sentieys[2]
[1]University of Rennes [1] - IRISA, FR; [2]INRIA, FR

IP5-5 EMPIRICAL MODELLING OF FDSOI CMOS INVERTER FOR SIGNAL/POWER INTEGRITY SIMULATION

Wael Dghais and Jonathan Rodriguez, Instituto de Telecomunicações, PT

IP5-6 ON-CHIP MEASUREMENT OF BANDGAP REFERENCE VOLTAGE USING A SMALL FORM FACTOR VCO BASED ZOOM-IN ADC

Osman Erol[1], Sule Ozev[1], Chandra K. H. Suresh[2], Rubin Parekhji[3] and Lakshmanan Balasubramanian[3]
[1]ASU, US; [2]NYU-Abu Dhabi, AE; [3]TI, IN

IP5-7 LOGICAL EQUIVALENCE CHECKING OF ASYNCHRONOUS CIRCUITS USING COMMERCIAL TOOLS

Arash Saifhashemi[1], Hsin-Ho Huang[2], Priyanka Bhalerao[3] and Peter Beerel[2]
[1]Intel, US; [2]University of Southern California, US; [3]yahoo, US

IP5-8 MAY-HAPPEN-IN-PARALLEL ANALYSIS OF ELECTRONIC SYSTEM LEVEL MODELS USING UPPAAL MODEL CHECKING

Che-Wei Chang and Rainer Doemer, University of California Irvine, US

IP5-9 VERIFYING SYNCHRONOUS REACTIVE SYSTEMS USING LAZY ABSTRACTION

Kumar Madhukar[1], Mandayam Srivas[2], Bjorn Wachter[3], Daniel Kroening[3] and Ravindra Metta[1]
[1]Tata Research Development and Design Center, IN; [2]Chennai Mathematical Institute, IN; [3]University of Oxford, GB

IP5-10 SPINTASTIC: SPIN-BASED STOCHASTIC LOGIC FOR ENERGY-EFFICIENT COMPUTING

Rangharajan Venkatesan[1], Swagath Venkataramani[2], Xuanyao Fong[2], Kaushik Roy[2] and Anand Raghunathan[2]
[1]NVIDIA Corporation, US; [2]Purdue University, US

IP5-11 LEAKAGE POWER REDUCTION FOR DEEPLY-SCALED FINFET CIRCUITS OPERATING IN MULTIPLE VOLTAGE REGIMES USING FINE-GRAINED GATE-LENGTH BIASING TECHNIQUE

Ji Li, Qing Xie, Yanzhi Wang, Shahin Nazarian and Massoud Pedram, University of Southern California, US

IP5-12 SUBHUNTER: A HIGH-PERFORMANCE AND SCALABLE SUB-CIRCUIT RECOGNITION METHOD WITH PRÜFER-ENCODING

Hong-Yan Su, Chih-Hao Hsu and Yih-Lang Li, National Chiao Tung University, TW

IP5-13 TIMING VERIFICATION FOR ADAPTIVE INTEGRATED CIRCUITS

Rohit Kumar[1], Bing Li[2], Yiren Shen[1], Ulf Schlichtmann[2] and Jiang Hu[1]
[1]Texas A&M University, College Station, US; [2]Technische Universität München, DE

IP5-14 A ROBUST APPROACH FOR PROCESS VARIATION AWARE MASK OPTIMIZATION

Jian Kuang, Wing-Kai Chow and Evangeline Young, The Chinese University of Hong Kong, HK

IP5-15 FASTTREE: A HARDWARE KD-TREE CONSTRUCTION ACCELERATION ENGINE FOR REAL-TIME RAY TRACING

Xingyu Liu, Yangdong Deng, Yufei Ni and Zonghui Li, Institute of Microelectronics, Tsinghua University, CN

IP5-16 REVERSE LONGSTAFF-SCHWARTZ AMERICAN OPTION PRICING ON HYBRID CPU/FPGA SYSTEMS

Christian Brugger, Javier Alejandro Varela, Norbert Wehn, Songyin Tang and Ralf Korn, University of Kaiserslautern, DE

IP5-17 ACCURATE ELECTROTHERMAL MODELING OF THERMOELECTRIC GENERATORS

Mohammad Javad Dousti[1], Antonio Petraglia[2] and Massoud Pedram[1]
[1]University of Southern California, US; [2]Federal University of Rio de Janeiro, BR

IP5-18 EFFICIENCY-DRIVEN DESIGN TIME OPTIMIZATION OF A HYBRID ENERGY STORAGE SYSTEM WITH NETWORKED CHARGE TRANSFER INTERCONNECT

Qing Xie[1], Younghyun Kim[2], Donkyu Baek[3], Yanzhi Wang[1], Massoud Pedram[1] and Naehyuck Chang[4]
[1]University of Southern California, US; [2]Purdue University, US; [3]Korea Advanced Institute of Science and Technology, KR; [4]Seoul National University, KR

12.1 SPECIAL DAY Hot Topic: Technology and Design Platforms for Diagnostics

Salle Oisans 1600 - 1730

Organiser: **Jo De Boeck,** IMEC, BE
Chair: **Chris Van Hoof,** IMEC, BE
Co-Chair: **Minkyu Je,** Daegu Gyeongbuk Institute of Science and Technology (DGIST), KR

Key to an efficient and effective treatment is early, fast and precise diagnose. This session showcases some of the recent advances and future potential of technologies that help enable the above mentioned requirements for patient centric care.

1600 ULTRAFLEXIBLE INTEGRATED CIRCUITS FOR IMPERCEPTIBLE BIO-SENSORS

Teppei Araki, University of Tokyo, JP

1630 NANOELECTRONICS FOR DISRUPTIVE DIAGNOSTIC PLATFORMS

Liesbet Lagae, IMEC, BE

1700 AN ULTRA-LOW POWER DUAL-MODE ECG MONITOR FOR HEALTHCARE AND WELLNESS

Daniele Bortolotti, University of Bologna, IT

12.2 Solver Advances and Emerging Applications

Belle-Etoile 1600 - 1730

Chair: **Julien Schmaltz,** Eindhoven University of Technology, NL
Co-Chair: **Gianpiero Cabodi,** Politecnico di Torino, IT

The first three papers of this session present strong advances to the scalability of Boolean and arithmetic solvers.

1600 SOLVING DQBF THROUGH QUANTIFIER ELIMINATION
Karina Gitina, Ralf Wimmer, Sven Reimer, Matthias Sauer, Christoph Scholl and Bernd Becker, University of Freiburg, DE

1630 FORMAL VERIFICATION OF SEQUENTIAL GALOIS FIELD ARITHMETIC CIRCUITS USING ALGEBRAIC GEOMETRY
Xiaojun Sun[1], Priyank Kalla[2], Tim Pruss[1] and Florian Enescu[3]
[1]University of Utah, US; [2]University of utah, US; [3]Georgia State University, US

1700 A UNIVERSAL MACRO BLOCK MAPPING SCHEME FOR ARITHMETIC CIRCUITS
Xing Wei, Yi Diao, Tak-Kei Lam and Yu-Liang Wu, The Chinese University of Hong Kong, HK

1715 TOWARDS AN ACCURATE RELIABILITY, AVAILABILITY AND MAINTAINABILITY ANALYSIS APPROACH FOR SATELLITE SYSTEMS BASED ON PROBABILISTIC MODEL CHECKING
Khaza Anuarul Hoque[1], Otmane Ait Mohamed[1] and Yvon Savaria[2]
[1]Concordia University, CA; [2]Polytechnique Montreal, CA

12.3 Patterning, Pairing, Placement and Packing

Stendhal 1600 - 1730

Chair: **Dirk Stroobandt,** Ghent University, BE
Co-Chair: **Patrick Groeneveld,** Synopsys, US

Place-and-route remain at the core of physical design, but must address a variety of important objectives, constraints and concerns. They can be added by standard-cell design to improve routing congestion while keeping area small.

1600 AN EFFECTIVE TRIPLE PATTERNING AWARE GRID-BASED DETAILED ROUTING APPROACH
Zhiqing Liu, Chuangwen Liu and Evangeline Young, The Chinese University of Hong Kong, HK

1630 SIMULTANEOUS TRANSISTOR PAIRING AND PLACEMENT FOR CMOS STANDARD CELLS
Ang Lu, Hsueh-Ju Lu, En-Jang Jang, Yu-Po Lin, Chun-Hsiang Hung, Chun-Chih Chuang and Rung-Bin Lin, Yuan Ze University, TW

1700 A TSV NOISE-AWARE 3-D PLACER
Yu-min Lee, Chun Chen, Jia-xing Song and Kuan-te Pan, National Chiao Tung University, TW

1715 IDENTIFYING REDUNDANT INTER-CELL MARGINS AND ITS APPLICATION TO REDUCING ROUTING CONGESTION
Woohyun Chung, Seongbo Shim and Youngsoo Shin, Korea Advanced Institute of Science and Technology, KR

12.4 High-Level Specifications and Models

Chartreuse 1600 - 1730

Chair: **Marc Geilen,** TU Eindhoven, NL
Co-Chair: **Laurence Pierre,** TIMA Lab, FR

This session presents different aspects of high-level specifications and models. The first paper introduces a new model of computation, fixed-priority process networks to address the need of determinism for multiprocessor applications. The second paper proposes an approach to detect and resolve potential synchronization problems between a discrete event simulation and timed dataflow simulation. The third paper presents a framework for checking the logical consistency of requirements in specifications written in a subset of natural language.

1600 MODELS FOR DETERMINISTIC EXECUTION OF REAL-TIME MULTIPROCESSOR APPLICATIONS
Peter Poplavko[1], Dario Socci[2], Paraskevas Bourgos[3], Marius Bozga[3] and Saddek Bensalem[3]
[1]Universite Joseph Fourier / Verimag, FR; [2]Verimag, ; [3]Verimag, FR

1630 PRE-SIMULATION SYMBOLIC ANALYSIS OF SYNCHRONIZATION ISSUES BETWEEN DISCRETE EVENT AND TIMED DATA FLOW MODELS OF COMPUTATION
Liliana Andrade[1], Torsten Maehne[1], Alain Vachoux[2], Cédric Ben Aoun[1], François Pecheux[1] and Marie-Minerve Louerat[3]
[1]Pierre et Marie Curie University, LIP6, FR; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH; [3]University Pierre et Marie Curie, FR

1700 FORMAL CONSISTENCY CHECKING OVER SPECIFICATIONS IN NATURAL LANGUAGES
Rongjie Yan[1], Chih-Hong Cheng[2] and Yesheng Chai[3]
[1]Institute of Software, Chinese Academy of Sciences, CN; [2]ABB Corporate Research, DE; [3]School of Computer Science & Technology, Soochow University, CN

12.5 New Perspectives in Next-Generation Medical Systems

Meije 1600 - 1730

Chair: **Martin Rajman,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Co-Chair: **Giovanni De Micheli,** École Polytechnique Fédérale de Lausanne (EPFL), CH

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1600 TACKLING THE BOTTLENECK OF DELAY TABLES IN 3D ULTRASOUND IMAGING
Aya Ibrahim[1], Pascal Hager[2], Andrea Bartolini[3], Federico Angiolini[1], Marcel Arditi[4], Luca Benini[3] and Giovanni De Micheli[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]Swiss Federal Institute of Technology in Zurich (ETHZ), CH; [3]Università di Bologna / ETH Zürich, IT; [4]EPFL, CH

1630 INTEGRATED CMOS RECEIVER FOR WEARABLE COIL ARRAYS IN MRI APPLICATIONS
Benjamin Sporrer[1], Luca Bettini[2], Christian Vogt[2], Andreas Mehmann[2], Jonas Reber[3], Josip Marjanovic[3], Thomas Burger[2], David Brunner[3], Gerhard Tröster[2], Klaas P. Prüssmann[3] and Qiuting Huang[2]
[1]Integrated Systems Laboratory, Swiss Federal Institute of Technology (ETH), CH; [2]Swiss Federal Institute of Technology in Zurich (ETHZ), CH; [3]Swiss Federal Institute of Technology in Zurich (ETHZ) / University of Zurich (UZH), CH

1700 TACTILE PROSTHETICS IN WISESKIN
John Farserotu[1], Jean-Dominique Decotignie[1], Vladimir Kopta[1], Daniel Camilo Rojas Quirós[1], Pierre-Nicolas Volpe[1], Jacek Baborowski[1], Christian Enz[2], Stéphanie Lacour[2], Hadrien Michaud[2], Roberto Martuzzi[2], Volker Koch[3], Huaiqi Huang[3], Tao Li[3] and Christian Antfolk[4]
[1]CSEM, CH; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH; [3]BFH, CH; [4]Lundt University, SE

12.6 Medical Design Automation: Is All That Simulation and Model Reduction Getting Into Your "Head"?

Bayard 1600 - 1730

Organisers: **Luca Daniel,** MIT, US
Luis Miguel Silveira, INESC-ID, PT
Chair: **Luca Daniel,** MIT, US
Co-Chair: **Luis Miguel Silveira,** INESC-ID, PT

Tools and techniques originally developed by the Electronic Design Automation community for parasitic extraction, model reduction, or circuit simulation are having deep impact in alternative and exiting fields outside of the

circuit world. In particular, this session shows several applications of such techniques to analyzing the functionality of the brain and of the nervous system, as well aiding the design of biomedical and medical instrumentation and diagnostics.

1600 **THE OLD, THE NEW, AND THE RECYCLED – EDA ALGORITHMS IN CONNECTOMIC**
Lou Scheffer, Howard Hughes Medical Institute, US

1630 **COMPUTATIONAL MODELING AND SIMULATION OF SYNCHRONIZED FIRING BEHAVIORS OF THE BRAIN**
Peng Li, Texas A&M, US

1700 **ELECTROMAGNETIC POWER DEPOSITION ANALYSIS TOOL FOR HIGH RESOLUTION MAGNETIC RESONANCE IMAGING BRAIN SCANS**
Jorge F. Villena[1], Athanasios G. Polimeridis[1], Lawrence L. Wald[2], Elfar Adalsteinsson[1], Jakob K. White[1] and Luca Daniel[1]
[1]Massachusetts Institute of Technology, US; [2]Massachusetts General Hospital, Harvard Medical School, US

12.7 Brain Health and Mental Disorders: new challenges for electronic engineers

Les Bans 1600 - 1730

Organiser: **Jo De Boeck,** IMEC, US
Chair: **Pablo Laguna,** CIBER-BBN, ES
Co-Chair: **Josep Maria Haro,** Parc Sanitari Sant Joan de Deu, ES

Taking well-known biomarkers of mental disorders together with some other indicators from physiological signals, a multiparametric marker can be elaborated from these constellations of individual data. This session will highlight the relevance of this kind of disorders, the proposed approach and where future opportunities lie for the broad DATE community.

1600 **TOWARDS A QUANTITATIVE MEASUREMENT OF MENTAL DISORDERS**
Jordi Aguiló, CIBER-BBN, Centro Nacional de Microelectrónica, Universitat Autònoma de Barcelona, ES

1615 **IMPROVING THE MONITORING AND THE UNDERSTANDING OF MENTAL DISORDERS**
Giovanni de Girolamo[1] and Josep Maria Haro[2]
[1]IRCCS Fatebenefratelli, IT; [2]Parc Sanitari Sant Joan de Deu, ES

1640 **WORLD ANALYSIS OF NON-INVASIVE CARDIOVASCULAR SIGNALS FOR THE MONITORING OF PSYCHOPHYSIOLOGICAL STATES**
Michele Orini[1] and Pablo Laguna[2]
[1]Institute of Cardiovascular Science, University College London, GB; [2]CIBER-BBN,

1705 **HEALTHCARE IN AN INTEGRATED DIGITAL WORLD**
Arben Merkoçi, Catalan Institution for Research and Advanced Studies (ICREA) and Institut Català de Nanociència i Nanotecnologia (ICN2), ES

W01 1st Workshop on Model-Implementation Fidelity (MiFi)

Meije 0830 — 1600

General Chairs **Suzanne Lesecq,** CEA-Leti-MINATEC Campus, FR
Anca Molnos, CEA-Leti, Grenoble, FR

Programme Committee Members
Saddek Bensalem, Université Joseph Fourier, FR
Kees Goossens, Eindhoven Univ. of Technology, NL
Koji Inoue, Kyoto University, JP
Vania Joloboff, INRIA, FR
Diana Marculescu, Carnegie Mellon University, US
Eugenio Villar, University of Cantabria, ES

Local Chairs **Christian Fabre,** CEA-Leti, Grenoble, FR
Julien Mottin, CEA, FR

In early design stages, software and platform developers work with abstractions of the hardware in the form analytical models, simulators, or estimators for, e.g., power consumptions, voltage and frequency scaling and control, application throughput, communication bandwidth. These abstractions are utilized to verify the correctness of software algorithms, predict their potential behavior, e.g., performance, energy, in an actual environment, and take decisions accordingly.

This workshop addresses the difficulties involved in assessing the fidelity of abstract, high-level models versus the real platform. Participants will be given several perspectives on the issue, starting with industrial practices, to academic formal, analytical methods, as well as simulation-based virtual platform approaches. Several of these methods will be shown at work, in a demonstration session. The organizers aim to have interactive sessions and lively discussions about the applicability and practicality of the presented methods.

The attendees will get a glance into current, advanced solutions for models and analysis of complex heterogeneous systems, in a keynote by Kim Grüttner, OFFIS - Institute for Information Technology, Germany. The topic of system models will be further detailed by a regular paper on how to balance the accuracy of high-level power analysis vs. the overhead by making use of ordered graphs, which are demonstrated on an Odroid development system consisting of an ARM big.LITTLE multi-core.

The challenging task of building abstract system-level models that faithfully capture performance information along to functional behavior will be covered in the keynote of Prof. Saddek Bensalem from University of Grenoble, France. On a related subject, two regular papers will address, first, the design and verification of state-charts extended with probabilistic transition, costs/rewards, and state invariants, and second, the memory vs. performance trade-off for streaming applications modelled by synchronous data-flow graphs.

Last but not least, the audience will be introduced to two design-flows that target fast prototyping on SoC platforms. The first, SimSoC, is a simulation framework based on SystemC able to certify that the execution of a binary program on an Instruction Set Simulator of a target architecture, e.g., ARM, produces the expected results. The second, CompSOC, is a platform that includes a formal modeling framework as a suitable entry point for application design. Software applications can be developed independently, and then executed on an FPGA platform without interference, hence their behaviour is guaranteed to respect the design constraints.

0830 **OPENING SESSION**
Panelists: Suzanne Lesecq and Anca Molnos, CEA-Leti, FR

0845 **SESSION 1: POWER AND PERFORMANCE MODELS OF PARALLEL SYSTEMS**
Kees Goossens, Eindhoven Univ. of Technology, NL,

0845 **KEYNOTE: EMPOWERING MIXED-CRITICAL SYSTEM ENGINEERS IN THE DARK SILICON ERA: TOWARDS POWER, TEMPERATURE AND AGING ANALYSIS OF HETEROGENEOUS MPSOCS AT SYSTEM-LEVEL**
Speaker: Kim Grüttner, OFFIS - Institute for Information Technology, DE

0930 **REGULAR PAPER: POWER-PROPORTIONAL MODELLING FIDELITY**
Ashur Rafiev[1], Fei Xia[2], Alexei Iliasov[1], Rem Gensh[1], Ali Aalsaud[1], Alexander Romanovsky[1] and Alex Yakovlev[1]
[1]Newcastle University, GB; [2]University of Newcastle upon Tyne, GB

1000 **REGULAR PAPER: IMPLEMENTATION-AWARE BUFFER-THROUGHPUT TRADEOFF IN EMBEDDED STREAM APPLICATIONS**
Kamyar Mirzazad Barijough[1], Matin Hashemi[1], Volodymyr Khibin[2] and Soheil Ghiasi[2]
[1]Sharif University of Technology, IR; [2]University of California, Davis, US

1030 **COFFEE BREAK**

1100 **SESSION 2: SOC DESIGN-FLOWS FOR FAST PLATFORM PROTOTYPING**
Eugenio Villar, University of Cantabria, ES, Contact Eugenio Villar

1100 **REGULAR PAPER: SIMSOC: A FAST PROVEN FAITHFUL FULL SYSTEM VIRTUAL PROTOTYPING FRAMEWORK**
Vania Joloboff[1], Jean-Francois Monin[2] and Xiaomu Shi[2]
[1]INRIA, FR; [2]University of Grenoble, FR

1130 **REGULAR PAPER: A COMPOSABLE AND PREDICTABLE MPSOC DESIGN FLOW FOR MULTIPLE REAL-TIME APPLICATIONS**
Seyed-Hosein Attarzadeh-Niaki[1], Ekrem Altinel[1], Martijn Koedam[2], Anca Molnos[3], Ingo Sander[4] and Kees Goossens[5]
[1]KTH Royal Institute of Technology, SE; [2]Eindhoven university of technology, NL; [3]CEA LETI, FR; [4]Royal Institute of Technology, SE; [5]Eindhoven Univ. of Technology, NL

1200 **LUNCH BREAK**

1300 **SESSION 3: VERIFICATION AND IMPLEMENTATION OF EMBEDDED SYSTEMS FROM HIGH-LEVEL MODELS**
Vania Joloboff, INRIA, FR

1300 **KEYNOTE: BUILDING FAITHFUL HIGH-LEVEL MODELS AND PERFORMANCE EVALUATION OF EMBEDDED SYSTEM**
Saddek Bensalem, Université Joseph Fourier, FR

1345 **REGULAR PAPER: ANALYSIS AND IMPLEMENTATION OF EMBEDDED SYSTEM MODE**
Bojan Nokovic and Emil Sekerinski, McMaster University, CA

1415 **COFFEE BREAK**

1500 **DEMO AND POSTER SESSION**
Julien Mottin, CEA-Leti, FR

W02 Design Automation of Things: EV Battery Packs

Bayard 0830 — 1630

Organisers
Naehyuck Chang, Korea Advanced Institute of Science and Technology (KAIST), KR
Massimo Poncino, Politecnico di Torino, IT
Sebastian Steinhorst, TUM CREATE, SG

Large battery packs are an integral part of electric vehicles and smart grid applications. A large battery pack consists of hundreds or even thousands of cells that need to be monitored and controlled by complex battery management systems.

There exists a multitude of open design challenges in the domain of battery pack design and battery management systems:

- Costs of battery packs are a major issue. While the production of battery cells is very expensive, the question is how design automation methodologies can help to reduce system, production, operational, and maintenance costs.
- With new requirements such as fast charging or active cell balancing in large battery packs, how can a battery management system guarantee a safe and reliable operation?
- The design of battery packs is in general domain-specific. How can design automation methods and new architectures make large battery packs modular and scalable?

This workshop discusses current and future challenges in battery pack design that are relevant for the design automation community. It comprises tutorial talks that give a background on electrochemistry aspects and state-of-the-art industrial approaches as well as talks that present recent advances in the domain of battery management and pack design methodologies.

The workshop complements the track A3 "Automotive Systems and Smart Energy Systems" by giving a detailed insight into the domain of battery pack design methodologies. Therefore, this workshop would be highly relevant for all participants of the A3 tracks as well as for others who want to learn which design automation approaches can be applied in the exciting domain of battery system design.

0830 **SESSION 1: BATTERY CHALLENGES IN EV DESIGN**
Chair: Naehyuck Chang, Korea Advanced Institute of Science and Technology (KAIST), KR

0830 **ELECTRIC VEHICLE DESIGN – BATTERY PACK CHALLENGES**
Patrick Groeneveld, Synopsys, US

0930 **FROM ELECTROCHEMISTRY TO BATTERY CELLS – CONTROL AND MONITORING CHALLENGES**
Jochen Friedl, TUM CREATE, SG

1000 **COFFEE BREAK**

1030 **SESSION 2: EFFICIENT BATTERY MANAGEMENT SYSTEM DESIGN**
Chair: Massimo Poncino, Politecnico di Torino, IT

1030 **CHARACTERIZATION AND MODELING OF ELECTRIC VEHICLE POWER CONSUMPTION AND BATTERY USAGE**
Speakers: Naehyuck Chang[1] and Sheldon Tan[2]
[1]Korea Advanced Institute of Science and Technology (KAIST), KR; [2]UC Riverside, US

1100 **ACTIVE CELL BALANCING AND VERIFICATION METHODOLOGIES IN THE BMS DOMAIN**
Speaker: Martin Lukasiewycz, TUM CREATE, SG

1130 **SMART CELL ARCHITECTURES FOR SCALABLE BATTERY PACKS**
Speaker: Sebastian Steinhorst, TUM CREATE, SG

1200 **LUNCH BREAK**

1300 **SESSION 3: MODELING AND SIMULATION FOR BETTER BATTERIES**
Chair: Sebastian Steinhorst, TUM CREATE, SG

1300 **MODELING ISSUES FOR BATTERY PACKS: ACCURACY VS. SIMULATION COMPLEXITY**
Speaker: Massimo Poncino, Politecnico di Torino, IT

1330 **MULTIPHYSICS, MULTISCALE SIMULATION OF A COMPLETE LI-ION BATTERY PACK AND SUB-SYSTEMS**
Speaker: Vincent Delafosse, ANSYS, US

1400 **CORRELATED STATISTICAL MODEL OF BATTERY CAPACITY AND RESISTANCE AND MANAGEMENT OF CELL-TO-CELL VARIATION IN MULTIPLE-CELL BATTERY PACK**
Speaker: Donghwa Shin , Yeungnam University, KR

1430 **BATTERY SIMULATION IN THE ETAS LABCAR ENVIRONMENT**
Speaker: Ingo Altmann, ETAS, DE

1500 **POSTER SESSION / COFFEE BREAK**

W03 2nd International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2015)

Stendhal 0830 – 1630

General Co-Chairs
Philippe Coussy, Universite de Bretagne Sud / Lab-STICC, FR
Nikil Dutt, University of California, Irvine, US

Programme Committee Co-Chairs
Jeff Krichmar, University of California, US
Philippe Coussy, Universite de Bretagne Sud / Lab-STICC, FR

Programme Committee Members
Romain Brette, ENS, FR
Yiran Chen, Dept. of Electrical and Computer Engineering University of Pittsburgh, US
Jorg Conradt, Technische Universitat Munchen, DE
Nikil Dutt, University of California, Irvine, US
Karlheinz Meier, Heidelberg University, DE
Vijaykrishnan Narayanan, Pennsylvania State University, US
Steve Furber, University of Manchester, GB
Narayan Srinivasa, HRL, US

Speakers
Todd Hylton, Brain Corporation, US
Giacomo Indiveri, ETHZ, CH
Romain Brette, ENS, FR
Rajit Manohar, Cornell University, US
Jorg Conradt, Technische Universitat Munchen, DE
Steve Furber, University of Manchester, GB
Anders Lansner, KTH, SE
Kristofor Carlson, University of California – Irvine, US

Biological neural systems are well known for their robust and power-efficient operation in highly noisy environments. Biological circuits are made up of low-precision, unreliable and massively parallel neural elements with highly reconfigurable and plastic connections. Two of the most interesting properties of the neural systems are its self-organizing capabilities and its template architecture. Recent research in biologically-plausible neural networks has demonstrated interesting principles about learning and neural computation. Understanding and applying these principles to practical problems is only possible if large-scale neural simulators or circuits can be constructed. This workshop will outline key modelling abstractions for the brain and focus on recent neural network models. Aspects of neuronal processing and computational issues related to modelling these processes will be discussed. Hardware and software solutions readily usable by neuroscientists and computer scientists and efficient enough to construct very large networks comparable to brain networks will be presented.

NeuComp 2015 is the second edition of a DATE workshop designed to attract both newcomers to neuromorphic computing, as well as neuromorphic researchers who wish to interact with the DATE community to stimulate new ideas, topics and collaborations. Since this is a hot area but one that is probably new to a large segment of the DATE community, half of the workshop will be devoted to a comprehensive introduction to Neuromorphic and Brain-Based Computing, where the audience will be exposed to basic definitions, key concepts, abstractions, design flows, and design constraints; also some highly visible research projects will be presented as exemplars to provide an overview of existing and emerging solutions in this domain. The other half of the event will create a forum for interactive discussion and exchange of ideas and experiences between researchers through posters and demonstrations, with the goal of highlighting details on applicability, performance, and strengths of current solutions. Our aim is for attendees to learn about emerging Neuromorphic and Brain-Based computing techniques, highlight publicly available modelling and simulation tools, and view directions for longer term research.

Topics of interest

- Authors are invited to submit original unpublished works on topics from a wide range of Neuromorphic and Brain-Based computing areas, including but not limited to:
- Formal models
- Hardware architectures
- Software tools
- Systems and applications
- Simulation Infrastructures

0830 **SESSION 0**

0830 **NEUROMORPHIC COMPUTING AND THE BRAIN: INSIGHTS, CHALLENGES AND MISUNDERSTANDINGS**
Speaker: Todd Hylton, Brain Corporation, US

0900 **SESSION 1**

0900 **ON-LINE LEARNING IN REAL-TIME BEHAVING NEUROMORPHIC SYSTEMS**
Speaker: Giacomo Indiveri, ETHZ, CH

0930 **THE BRAIN SIMULATOR**
Speaker: Romain Brette, ENS, FR

1000 **BREAK & POSTER/DEMO SESSION 1**

1000 **TBD**

1100 **SESSION 2**

1100 **DIGITAL NEUROMORPHIC SYSTEMS**
Speaker: Rajit Manohar, Cornell Univ., US

1130 **COMPUTATIONAL NEUROSCIENCE FOR TECHNOLOGY: EVENT-BASED VISION SENSORS AND INFORMATION PROCESSING**
Speaker: Jorg Conradt, Technische Universitat Munchen, DE

1300 **SESSION 3**

1300 **THE SPINNAKER PROJECT**
Speaker: Steve Furber, University of Manchester, GB

1330 **BIOLOGICAL INSPIRATION, FUNCTIONALITY AND HARDWARE IMPLEMENTATION ASPECTS OF BCPNN**
Speaker: Anders Lansner, KTH, SE

1400 **TOOLS AND FRAMEWORKS FOR CONSTRUCTING SPIKING NEURAL NETWORK MODELS OF BRAIN CIRCUITS**
Speaker: Kristofor Carlson, University of California – Irvine, US

1430 **BREAK & POSTER/DEMO SESSION 2**

1600 **WRAP-UP & CLOSING SESSION**

FRIDAY 13 MARCH, 2015

DATE15
March 9 – 13, 2015, Grenoble, France
FRI

W04 DUHDe – 2nd Workshop on Design Automation for Understanding Hardware Designs

Berlioz 0830 — 1630

Organisers
Goerschwin Fey, Univ. of Bremen, DE
Emmanuelle Encrenaz-Tiphene, UPMC/LIP6, FR

Programme Committee Members
Valeria Bertacco, University of Michigan, US
Lyes Benalycherif, STMicroelectronics, FR
Ian Harris, University of Californa Irvine, US
Masahiro Fujita, University of Tokyo, JP
Franco Fummi, Universita' di Verona, IT
Maksim Jenihhin, Tallinn University of Technology, EE
Tun Li, National University of Defense Technology, School of Computer, CN
Eli Arbel, IBM, IL
Raik Brinkmann, OneSpin Solutions GmbH, DE

Understanding a hardware design is tough. When entering a large team as a new member, when extending a legacy design, or when documenting a new design, lacks in understanding the details of a design are major obstacles for productivity. In software engineering topics like software maintenance, software understanding, reverse engineering are well established in the research community and partially tackled by tools. In the hardware area the re-use of IP-blocks, the growing size of designs and design teams leads to similar problems. Understanding of hardware requires deep insight into concurrently operating units, optimizations to reduce the required area, and specially tailored functional units for a particular use.

The workshop is of interest to practitioners working in circuit design and to researchers interested in design automation.

The aim of the 2nd Workshop on Design Automation for Understanding Hardware Designs (DUHDe) is to gather a community for these topics in electronic design automation. The workshop is not limited to the following topics in design understanding but includes:

- Design descriptions from the ESL down to RTL
- Extraction of high-level properties
- Localization of code implementing particular functionality
- Hardware design evolution: feature integration, feature interactions
- Innovative GUIs for designs
- Managing documentation of hardware designs
- Analysis of interaction between hardware and software
- Formal methods for design understanding
- Scalable approaches to design understanding

0830 **OPENING SESSION**
Speakers: Goerschwin Fey[1] and Emmanuelle Encrenaz-Tiphene[2]
[1]Univ. of Bremen, DE; [2]UPMC/LIP6, FR

0840 **INVITED TALK 1**

0840 **PRACTICAL APPLICATIONS OF HARDWARE DESIGN UNDERSTANDING USING FORMAL METHODS**
Speaker: Eli Arbel, IBM Research, Haifa, IL

0915 **TECHNICAL SESSION 1**

0915 **SYSTEMC-BASED LOOSE MODELS: RTL ABSTRACTION FOR DESIGN UNDERSTANDING**
Authors: Saif Abrar Syed, Maksim Jenihhin and Jaan Raik, Tallinn University of Technology, EE

0945 **ECORE MODEL GENERATION FROM SYSTEMC/C++ IMPLEMENTATIONS**
Authors: Jannis Stoppe[1] and Rolf Drechsler[2]
[1]Universität Bremen, DE; [2]University of Bremen/DFKI, DE

1010 **TOWARDS ANALYSING FEATURE LOCATIONS THROUGH TESTING TRACES WITH BUT4REUSE**
Authors: Jabier Martinez[1], Jan Malburg[2], Tewfik Ziadi[3] and Goerschwin Fey[4]
[1]SnT, University of Luxembourg, LU; [2]University of Bremen, DE; [3]LiP6, University Pierre and Marie Curie, FR; [4]Univ. of Bremen, DE

1035 **COFFEE BREAK**

1100 **INVITED TALK 2**

1100 **ASSERTION MINING**
Speaker: Shobha Vasudevan, University of Illinois at Urbana-Champaign, US

1150 **POSTER TEASERS**

1200 **LUNCH**

1313 **TECHNICAL SESSION 2**

1313 **LEARNING GRAMMARS FOR ASSERTION CREATION FROM NATURAL LANGUAGE**
Authors: Christopher Harris[1] and Ian Harris[2]
[1]University of California Irvine , US; [2]University of Californa Irvine, US

1325 **A BINDING METHOD FOR HIERARCHICAL TESTABILITY USING RESULTS OF TEST ENVIRONMENT GENERATION**
Authors: Jun Nishimaki[1], Toshinori Hosokawa[2] and Hideo Fujiwara[3]
[1]Graduate School of Industrial Technology, Nihon University, JP; [2]Nihon University, JP; [3]Faculty of Informatics, Osaka Gakuin University, JP

1350 **INVITED TALK 3**

1350 **PARALLELIZATION OF SYSTEMC-TLM SIMULATIONS, AND MODELLING OF TIME AND POWER CONSUMPTION**
Speaker: Matthieu Moy, Verimag, Grenoble, FR

1440 **POSTER SESSION AND COFFEE BREAK**

1530 **TECHNICAL SESSION 3**

1530 **A SIMULATOR TO UNDERSTAND THE EFFECTS OF FAULT INJECTION ATTACKS ON A MICROCONTROLLER**
Authors: Nicolas Moro[1], Karine Heydemann[2], Bruno Robisson[3] and Emmanuelle Encrenaz-Tiphene[4]
[1]CEA, FR; [2]LIP6 / University Pierre et Marie Curie, FR; [3]CEA-Leti, FR; [4]UPMC/LIP6, FR

1555 **PANEL**

1555 **DESIGN UNDERSTANDING - AT WHAT ABSTRACTION LEVEL IS THE PAIN MOST INTENSE?**
Panelists: Lyes Benalycherif[1], Dominique Borrione[2], Franco Fummi[3] and Jaan Raik[4]
[1]STMicroelectronics, FR; [2]TIMA, FR; [3]Universita' di Verona, IT; [4]Tallinn University of Technology, Department of Computer Engineering, EE

W05 3D Integration Technology, Architecture, Design, Package, Automation, and Test

Belle-Etoile 0815 – 1730

General Chairs **Saqib Khursheed,** University of Liverpool, GB
Pascal VIVET, CEA-Leti, FR

Panel Chair **Françoise von Trapp,** 3D InCites, US

Programme Committee Chairs
Christian Weis, Microelectronic System Research Group, DE
Makoto Nagata, Kobe University, JP

Steering Committee Members
Erik Jan Marinissen, IMEC, BE
Qiang Xu, The Chinese University of Hong Kong, HK

Publication Chairs
Bjørn B. Larsen, NTNU, NO
Andy Heinig, Fraunhofer IIS/EAS, DE

3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. To produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges. Previous five editions of this workshop took place in conjunction with DATE 2010, DATE 2011, DATE 2012, DATE 2013 and DATE 2014.

TOPIC AREAS

You are invited to participate and submit your contributions to the DATE 2015 Friday Workshop on 3D Integration. The areas of interest include (but are not limited to) the following topics:

- 3D technologies: chip-on-chip, micro-bumping, contactless, and through-silicon-vias interconnect
- TSV formation, perm./temp. wafer (de-)bonding
- 3D architectures and design space exploration
- 3D combinations of logic, memory, analog, RF
- Application, product, or test chip case studies
- 3D design methods and EDA tools
- Signal and power integrity, and ESD in 3D
- Thermo(-mechanical) analysis and -aware design
- Chip-package co-design for 3D
- Test, design-for-test, and debug techniques for 3D
- Wafer test access, KGD test, thin-wafer handling
- Economic benefit/cost trade-off studies
- Standardization initiatives

The workshop program contains the following elements:

- An invited keynote and an invited talk.
- A special session on "3D memories" and another special session on "die-package co-design".
- A panel session on "Will 3D Integration Break Down Memory Bandwidth Barriers? How and When?".
- A technical session with 5 regular presentations.
- Two poster sessions.

0815 **SESSION 1: OPENING AND 1ST KEYNOTE**
Chair: Pascal VIVET, CEA-Leti, FR

0815 **WELCOME ADDRESS**
Speaker: Pascal VIVET, CEA-Leti, FR

0820 **KEYNOTE: "COMPUTING IN 3D"**
Speaker: Paul Franzon, North Carolina State University, US

0900 **SPECIAL SESSION: "3D MEMORIES"**
Chair: Christian Weis, Microelectronic System Research Group, DE

0900 **TSV STACKING DESIGN AND PACKAGING FOR HIGH BANDWIDTH MEMORIES WITH 1GHZ SAMPLING DIGITIZED NOISE MONITOR**
Speaker: Kazuki Fukuoka, Renesas Electronics, JP

0920 **HOW 3D MEMORY IS CHANGING COMPUTING**
Speaker: Robert Patti, Tezzaron Semiconductor, US

0940 **3D MEMORIES: FACTS AND FICTION**
Speaker: Andreas Hansson, ARM Ltd, GB

1000 **POSTER SESSION AND COFFEE BREAK**

1030 **SESSION 2: INVITED TALK AND PANEL**
Moderator: Françoise von Trapp, 3D InCites, US

1030 **INVITED TALK: "TESTING OF 3D ICS: HYPE, MYTHS, AND REALITIES"**
Speaker: Krishnendu Chakrabarty, Duke University, US

1100 **PANEL: "WILL 3D INTEGRATION BREAK DOWN MEMORY BANDWIDTH BARRIERS? HOW AND WHEN?"**
Brendan Farley[1], Denis Dutoit[2], Hsien-Hsin S. Lee[3], Geert Van der Plas[4] and Mustafa Badaroglu[5]
[1]XILINX, US; [2]CEA LETI, FR; [3]TSMC, TW; [4]IMEC, BE; [5]Qualcomm, US

1200 **LUNCH BREAK**

1300 **SPECIAL SESSION: "DIE-PACKAGE CO-DESIGN BENEFITS AND CHALLENGES"**
Chair: Herb Reiter, EDA2ASIC, US

1300 **THE 3D-IC ECOSYSTEM TODAY AND HOW TO STRENGTHEN IT FURTHER**
Speaker: Herb Reiter, EDA2ASIC, US

1320 **DATA HANDLING FOR CHIP-PACKAGE-BOARD CO-DESIGN AND DESIGN RULE CHECK**
Speaker: Andy Heinig, Fraunhofer IIS/EAS, DE

1340 **SILICON-PACKAGE CO-DESIGN CHALLENGES FROM 2D TO 3D**
Speaker: Georg Kimmich , STMicrolectronics, FR

1400 **IC DESIGN ASPECTS OF DIE-PACKAGE CO-DESIGN**
Speaker: John Ferguson, Mentor Graphics Corp, US

1430 **POSTER SESSION AND COFFEE BREAK**

1500 **SESSION 3: TEST AND TECHNOLOGY CHALLENGES FOR 3D ICS**
Chair: Makoto Nagata, Kobe University, JP, Contact Makoto Nagata

1500 **IMPACT OF MULTI-VT TECHNIQUE IN ELIMINATING THERMAL RUNAWAY DURING TESTING OF 3D CHIPS**
Authors: Seetal Potluri[1], Satya Trinadh Adireddy[2], S. G. Singh[2], Sobhan Babu Ch.[2] and Kamakoti Veezhinathan[1]
[1]IIT Madras, IN; [2]IIT Hyderabad, IN

1518 **3D-IC SESSION-BASED VS SESSION-LESS TEST SCHEDULING: A CASE STUDY**
Authors: Marie-Lise Flottes, Joao Azevedo, Giorgio Di Natale and Bruno Rouzeyre , LIRMM, FR

1536 **3D IC TEST THROUGH LOW NOISE POWER LINE METHODOLOGY**
Authors: Alberto Pagani and Allessandro Motta, STMicroelectronics, IT

1554 **BROADBAND METAL-INSULATOR-METAL CAPACITORS ON SILICON INTERPOSER FOR LOW IMPEDANCE POWER DISTRIBUTION NETWORK**
Authors: Nao Ueda[1], Cesar Roda Neve[2], Mikael Detalle[2], Eric Beyne[2], Geert Van der Plas[2] and Makoto Nagata[1]
[1]Kobe University, JP; [2]IMEC, BE

1612 **A TSV TO TSV, A TSV TO METAL INTERCONNECTS, AND A TSV TO ACTIVE DEVICE COUPLING CAPACITANCE: ANALYSIS AND RECOMMENDATIONS**
Author: Khaled Mohamed, Mentor Graphics, EG

1628 **POSTER LIST**

1628 **A NEW CONTACTLESS SUBSTRATE SHIPPER FOR ULTRATHIN, 3D, LENSED OR BUMBED WAFERS**
Author: Jorgen Lundgren, Entegris GmbH, DE

1628 **TEST AND RECONFIGURATION OF TSV DEFECT IN 3D-IC**
Author: Mohamed Benabdeladhim, Dept. of Physics, Faculty of Science of Monastir, TN

W06 Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN)

Chartreuse 0830 — 1630

General Co-Chairs

Lorena Anghel, TIMA, FR
Olivier Heron, CEA, FR

Programme Committee Co-Chairs

Elena Gramatova, University of Technology in Bratislava, SK
Maksim Jenihhin, Tallinn University of Technology, EE

Programme Committee Members

Oliver Bringmann, University of Tübingen, DE
Florian Cacho, STMicroelectronics, FR
Luigi Dilillo, LIRMM, FR
Adrian Evans, Iroc, FR
Dimitris Gizopoulos, University of Athens, Department of Informatics & Telecommunications, GR
Said Hamdioui, Delft University of Technology, NL
Domenik Helms, OFFIS, DE
Viacheslav Izosimov, The Royal Institute of Technology (KTH), SE
Artur Jutman, Testonica Lab, EE
Zdenek Kotasek, FIT VUT in Brno, CZ
Hans Manhaeve, Ridgetop Europe, BE
Alberto Nannarelli, DTU, DK
Ozcan Ozturk, Bilkent University, TR
Zdenek Pliva, Technical University Liberec, CZ
Salvatore Pontarelli, University of Rome "Tor Vergata", IT
Dhiraj Pradhan, University of Bristol, GB
Mihalis Psarakis, University of Piraeus, GR
Jaan Raik, Tallinn University of Technology, Department of Computer Engineering, EE
Chiara Sandionigi, CEA, FR
Andreas Steininger, Vienna University of Technology, AT
Walter Stechele, Technische Universität München, DE
Viera Stopjakova, FEI STU, SK
Mehdi Tahoori, KIT, DE
Elena Vatajelu, Politecnico de Torino, IT
Heinrich T. Vierhaus, BTU Cottbus, DE

Action Chair **Marco Ottavi,** University of Roma, IT

Each year, the MEDIAN project Workshops provide an event where ideas are exchanged and discussed, and new cooperations are created as researchers from the academic and industrial domains share their recent findings, theories and on-going scientific and practical works in the dependable system designs and their applications. Constant advances in manufacturing yield and field reliability are important enabling factors for electronic devices pervading our lives, from medical to consumer electronics, from railways to the automotive and avionics scenarios. At the same time, both technology and architectures are today at a turning point.

In year 2015 the workshop will provide an open forum for presentations and will challenge the participants to think and discuss hot research topics. Prospective authors are encouraged to submit their work regarding the following topics (but not limited to):

- How to address test, fault tolerance and lifetime extension in heterogeneous low-power multicore systems?
- How to tackle cross-layer optimizations for design, test and reliability of multicore systems at nanoscale?
- How to test and verify reliable embedded systems without time and effort explosions?

A wider scope of topics relevant to the workshop includes the following:

- Methodologies/techniques for manufacturing reliable nanoscale devices
- System level design, on-line testing/fault tolerance
- Dependability Evaluation and Validation/Debug Methodologies
- Fault tolerance for space applications
- Fault tolerance for transportation systems
- Fault tolerance for medical devices

0830 OPENING SESSION
Co-Chairs: Lorena Anghel, TIMA, FR, Contact Lorena Anghel
Olivier Heron, CEA, FR

0830 WELCOME PRESENTATION

0840 KEYNOTE
Chair: Elena Gramatova, University of Technology in Bratislava, SK

0840 RELIABILITY CHALLENGES FOR CYBER-PHYSICAL SYSTEMS
Speaker: Zebo Peng, Linköping University, SE

0940 PAPER SESSION I: FAULT TOLERANCE AND TEST TECHNIQUES FOR LOW POWER DESIGN
Chair: Elena Gramatova, University of Technology in Bratislava, SK

0940 BTI ANALYSIS FOR HIGH PERFORMANCE AND LOW POWER SRAM SENSE AMPLIFIER DESIGNS
Authors: Innocent Agbo[1], Mottaqiallah Taouil[1], Said Hamdioui[2], Halil Kukner[3], Pieter Weckx[4], Praveen Raghavan[3] and Francky Catthoor[3]
[1]Delft UT, NL; [2]Delft University of Technology, NL; [3]IMEC, BE; [4]IMEC vzw, BE

1000 POWER-AWARE ONLINE DETECTION OF HARDWARE DEFECTS FOR MANYCORE SYSTEMS WITH DVFS SUPPORT
Authors: Mohammad-Hashem Haghbayan[1], Amir-Mohammad Rahmani[2], Mohammad Fattah[1], Pasi Liljeberg[1], Juha Plosila[1] and Hannu Tenhunen[1]
[1]University of Turku, FI; [2]Turku Center for Computer Science (TUCS), Finland, FI

1020 POSTER SESSION AND COFFEE BREAK

1020 A NEW ADAPTIVE SYSTEM FOR SOFTWARE-BASED TEST GENERATION OF PROCESSORS
Authors: Jan Hudec[1] and Elena Gramatova[2]
[1]Slovak UT, SK; [2]University of Technology in Bratislava, SK

1020 RADIATION IMPACT ON MECHANICAL APPLICATION DRIVEN BY FPGA-BASED CONTROLLER
Authors: Jakub Podivínský[1], Marcela Simkova [2] and Zdenek Kotasek[2]
[1]Brno UT, CZ; [2]FIT VUT in Brno, CZ

1020 A FAULT RESILIENT ROUTING ALGORITHM FOR HETEROGENEOUS 3D NOCS
Authors: Masoumeh Ebrahimi[1], Ronak Salamat[2], Nader Bagherzadeh[3] and Masoud Daneshtalab[4]
[1]university of Turku, FI; [2]Univ. California, US; [3]University of California Irvine, US; [4]UTU, FI

1020 MIXED CRITICALITY METRIC FOR SAFETY-CRITICAL CYBER-PHYSICAL SYSTEMS ON MULTI-CORE ARCHITECTURES
Authors: Viacheslav Izosimov[1] and Erik Levholt[2]
[1]The Royal Institute of Technology (KTH), SE; [2]Svenska Grindmatriser AB, SE

1020 SECURED CONNECTIVITY OF DISTRIBUTED AGENTS IN PRESENCE OF MANY NOC FAULT.
Authors: Mohammad Fattah, Pasi Liljeberg and Juha Plosila, University of Turku, FI

1020 ON AGING OF LATCHES' ROBUSTNESS
Authors: Martin Omana[1], Luz Antuanet Adanaque Infante[1], Cecilia Metra[2] and Daniele Rossi [3]
[1]Univ. Bologna, IT; [2]University of Bologna, IT; [3]Univ. Southampton, GB

1020 INFLUENCE OF RECONFIGURATION TECHNIQUES FOR DYNAMICALLY SCHEDULED SUPERSCALAR PROCESSORS ON POWER CONSUMPTION
Authors: Tobias Koal[1], Robert Karas[1], Heinrich Theodor Vierhaus[1] and Mario Schölzel[2]
[1]BTU Cottbus, DE; [2]IHP and Univ. Potsdam, DE

1020 **EXTENDED CHECKERS FOR CONTROL PART OF ROUTERS IN NETWORK-ON-CHIPS**
Authors: Ranganathan Hariharan[1], Behrad Niazmand[1], Thomas Hollstein[2], Jaan Raik[2] and Gert Jervan[1]
[1]Tallinn UT, EE; [2]Tallinn University of Technology, EE

1020 **SIMULATION FRAMEWORK FOR OPTIMIZING SRAM POWER CONSUMPTION UNDER RELIABILITY CONSTRAINT**
Authors: Florian Cacho[1], Erwan Piriou[2], Olivier Heron[3] and Vincent Huard[1]
[1]STMicroelectronics, FR; [2]CEA LIST, FR; [3]CEA, FR

1120 **PAPER SESSION II: VERIFICATION AND TEST TECHNIQUES FOR RELIABLE DESIGN**
Chair: Olivier Heron, CEA, FR, Contact Olivier Heron

1120 **EVALUATION OF FAILURES MASKING ACROSS THE SOFTWARE STACK**
Authors: Thiago Santini[1], Paolo Rech[1], Anderson Luiz Sartor[2], Ulisses Brisolara Corrêa[3], Luigi Carro[4] and Flavio Wagner[4]
[1]Federal University of Rio Grande do Sul, BR; [2]Federal University of Rio Grande do Sul (UFRGS), BR; [3]Instituto Federal de Educação, Ciência e Tecnologia Sul-rio-grandense, BR; [4]UFRGS, BR

1140 **A NOVEL FORMAL VERIFICATION FRAMEWORK FOR FUTURE MPSOC ARCHITECTURES**
Authors: Christian Schöler[1], René Krenz-Baath[1] and Roman Obermaisser[2]
[1]Hochschule Hamm-Lippstadt, DE; [2]University of Siegen, DE

1200 **LUNCH**

1300 **INVITED TALK**
Chair: Maksim Jenihhin, Tallinn University of Technology, EE, Contact Maksim Jenihhin

1300 **TECHNOLOGY SCALING AND RELIABILITY CHALLENGES IN THE MULTICORE ERA**
Speaker: Vincent Huard, STMicroelectronics, FR

1340 **PAPER SESSION III: DEPENDABLE SYSTEMS AND COMPONENTS**
Chair: Maksim Jenihhin, Tallinn University of Technology, EE, Contact Maksim Jenihhin

1340 **EFFICIENT ONLINE TESTING OF AN ARRAY OF RECONFIGURABLE RISC PROCESSORS**
Authors: S. Pagliarini[1], Salvatore Pontarelli[2], JImson Mathew[3], Dhiraj K. Pradhan[3], Ioannis Sourdis[4], D.A. Khan[5], A. Malek[5], S. Tzilis[5], Georgios Smaragdos[6] and Christos Strydis[6]
[1]Univ. of Bristol, GB; [2]University of Rome "Tor Vergata", IT; [3]University of Bristol, GB; [4]Chalmers Univeristy of Technology, SE; [5]Chalmers UT, SE; [6]Erasmus Medical Center, NL

1400 **MEASURING AND IDENTIFYING AGING-CRITICAL PATHS IN FPGAS**
Authors: Petr Pfeifer[1], Jaan Raik[2], Maksim Jenihhin[2], Raimund Ubar[2] and Zdenek Pliva[1]
[1]Technical University Liberec, CZ; [2]Tallinn University of Technology, EE

1420 **DYNAMIC VOLTAGE SCALING WITH FAULT-TOLERANCE FOR LIFETIME OPERATION**
Authors: Jorge Semião[1], Carlos Leong[2], Ruben Cabral[2], Marcelino Santos[2], Isabel Teixeira[2] and Paulo Teixeira[2]
[1]Univ. Algarve, PT; [2]INESC-ID, PT

1440 **COFFEE BREAK**

1500 **PAPER SESSION IV: DEPENDABLE MULTICORE SYSTEMS AND PROCESSORS TESTING AND SELF-REPAIR**
Chair: Lorena Anghel, TIMA, FR, Contact Lorena Anghel

1500 **SOFTWARE-BASED SELF-REPAIR FOR HETEROGENOUS MULTI-CORE SYSTEMS**
Authors: Sebastian Müller[1] and Mario Schölzel[2]
[1]Heinrich Theodor Vierhaus – Brandenburg UT, DE; [2]IHP and Univ. Potsdam, DE

1520 **UNIVERSAL PSEUDO-RANDOM GENERATION OF ASSEMBLER CODES FOR PROCESSORS**
Authors: Ondrej Cekan, Marcela Simkova and Zdenek Kotasek, FIT VUT in Brno, CZ

1540 **EXPLORING CHECK-POINTING AND ROLLBACK RECOVERY UNDER SELECTIVE SBST IN CHIP MULTI-PROCESSORS**
Authors: Michael Skitsas[1], Chrysostomos Nicopoulos[2] and Maria Michael[2]
[1]Univ. Cyprus, CY; [2]University of Cyprus, CY

1600 **DISCUSSION AND CLOSING SESSION**
Co-Chairs: Lorena Anghel, TIMA, FR, Contact Lorena Anghel
Olivier Heron, CEA, FR, Contact Olivier Heron

W07 Designing with Uncertainty - Opportunities & Challenges

Salle Lesdiguières 0830 — 1630

General Chairs **James Alfred Walker,** University of York, GB
Andy M. Tyrrell, University of York, GB

Programme Committee Chairs
Martin A. Trefzer, University of York, GB
Simon J. Bale, University of York, GB

Over the past 20 years, computing devices have rapidly improved in performance and function density enabled by the continuous shrinking of technology sizes. However, as device sizes have now approached atomistic scales the statistical nature of intrinsic device variations becomes prevalent. Fabrication yields decrease drastically and failure rates increase significantly as a result, because every physical instance of a design behaves in a stochastically different manner. Despite great efforts and advances in technology and novel materials the laws of Physics and Chemistry will always apply and intrinsic variability, device mismatch and noise will always be present at the lowest levels of any system. Therefore, large complex systems need to be designed taking certain levels of 'uncertainty' at lower levels into consideration. In turn, when assembling larger entities from smaller components, a certain amount of 'uncertainty' in behaviour needs to be expected. In this vein, it is as much about understanding, modelling and predicting variability and noise, as it is about thinking about ways to 'embrace intrinsic variations' and build systems that can robustly function despite these effects.

This workshop aims to highlight and address these challenges. It brings together people from different strands of device and circuit design, and provides a venue to collectively talk about emerging trends and the future development of the field. The technical programme will address a diverse range of research areas related to 'designing with uncertainty', such as:

- Variability modelling, prediction, fabrication and solutions
- Predicting future technologies
- Performance Improvement through Reconfiguration
- Designing with unreliable components
- Fault-tolerant design, recovery through reconfiguration
- Electronic design optimisation
- Design for test, built-in self test
- New and emerging devices (biological, carbon, etc.)
- Innovative design techniques (e.g. bio-inspired)

0830 OPENING SESSION
Speaker: Andy M. Tyrrell, University of York, GB

0840 INVITED KEYNOTE 1
Chair: Andy M. Tyrrell, University of York, GB

0840 PANDA: PROGRAMMABLE ANALOGUE AND DIGITAL ARRAY
Speaker: James Alfred Walker, University of York, GB

0920 SESSION 1
Chair: Andy M. Tyrrell, University of York, GB

0920 THERMAL-AWARE ADAPTIVE ENERGY MINIMIZATION OF OPENMP PARALLEL APPLICATIONS
Authors: Rishad Shafik, Anup Das, Sheng Yang, Geoff Merrett and Bashir Al-Hashimi, University of Southampton, GB

0930 CHARACTERIZATION OF RANDOM TELEGRAPH NOISE AND ITS IMPACT ON RELIABILITY OF SRAM SENSE AMPLIFIERS
Authors: Javier Martin-Martinez[1], Javier Diaz Fortuny[1], Montserrat Nafria Maqueda[1], Xavier Aymerich Humet[1], Elisenda Roca Moreno[2], Francisco Fernandez[3] and Antonio Rubio[4]
[1]Universitat Autònoma de Barcelona (UAB), ES; [2]de Microelectrónica de Sevilla, CSIC and Universidad de Sevilla, ES; [3]IMSE, CSIC and University of Sevilla, ES; [4]Universitat Politècnica de Catalunya (UPC), ES

0940 RELIABLE COMPUTATION WITH UNRELIABLE COMPUTERS
Authors: Kier Dugan[1], Andrew D. Brown[1], Jeff S. Reeve[1], Rob M. Mills[1] and Steve Furber[2]
[1]University of Southampton, GB; [2]University of Manchester, GB

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0950 A MULTI CYCLE CAPTURE TEST GENERATION METHOD FOR LOW CAPTURE POWER DISSIPATION
Authors: Hiroshi Yamazaki[1], Jun Nishimaki[2], Toshinori Hosokawa[1] and Masayoshi Yoshimura[3]
[1]Nihon University, JP; [2]Graduate School of Industrial Technology, Nihon University, JP; [3]Kyoto Sangyo University, JP

1000 PROBABILISTIC ANALYSIS OF POWER AND TEMPERATURE UNDER PROCESS VARIATION FOR ELECTRONIC SYSTEM DESIGN
Authors: Ivan Ukhov, Petru Eles and Zebo Peng, Linköping University, SE

1010 MEASURING THE IMPACT OF VARIABILITY ON THE PANDA ARCHITECTURE
Authors: Simon J. Bale, James Alfred Walker, Pedro Burmester Campos, Martin A. Trefzer and Andy M. Tyrrell, University of York, GB

1030 COFFEE/TEA BREAK

1100 INVITED KEYNOTE 2
Chair: James Alfred Walker, University of York, GB

1100 PREDICTIVE TECHNOLOGY FOR ADVANCED NODE DESIGN EXPLORATION
Speaker: Robert Aitken, ARM, US

1140 SESSION 2
Chair: James Alfred Walker, University of York, GB

1140 ABSTRACTING TCAD MODELS ABOVE THE CIRCUIT LEVEL
Authors: Domenik Helms[1], Reef Eilers[1], Malte Metzdorf[1] and Wolfgang Nebel[2]
[1]OFFIS, DE; [2]Oldenburg University and OFFIS, DE

1150 ON THE HARDWARE TROJANS DETECTION, USING MIXED-SIGNAL ICS
Authors: Georgina Kalogeridou[1], Nicolas Sklavos[2], Andew W. Moore[1] and Odysseas Koufopavlou[3]
[1]Computer Laboratory, University of Cambridge, GB; [2]Technological Educational Institute of Patras, GR; [3]Electrical & Computer Engineering Department, University of Patras, HELLAS, GR

1200 LUNCH BREAK

1300 INVITED KEYNOTE 3
Chair: Simon J. Bale, University of York, GB

1300 FACTORING VARIABILITY IN THE TCAD BASED DESIGN-TECHNOLOGY CO-OPTIMISATION
Speaker: Asen Asenov, University of Glasgow, GB

1340 SESSION 3
Chair: Simon J. Bale, University of York, GB

1340 STATISTICAL LIFETIME ANALYSIS IN MEMRISTIVE CROSSBAR
Authors: Peyman Pouyan[1], Esteve Amat[1] and Antonio Rubio[2]
[1]Universitat Politècnica de Catalunya (UPC), Barcelona, ES; [2]Universitat Politècnica de Catalunya (UPC), ES

1350 FAST PARAMETRIC FAULT MODELING OF NANOSCALE INTEGRATED CIRCUITS
Authors: Hassan Ghasemzadeh Mohammadi, Pierre-Emmanuel Gaillardon and Giovanni De Micheli, EPFL, CH

1400 RELIABILITY ANALYSIS OF COMPARATORS
Authors: Illani Mohd Nawi, Basel Halak and Mark Zwolinski, University of Southampton, GB

1410 HIGH-SIGMA PERFORMANCE ANALYSIS USING MULTI-OBJECTIVE EVOLUTIONARY ALGORITHMS
Authors: James Alfred Walker, Simon J. Bale, Martin A. Trefzer and Andy M. Tyrrell, University of York, GB

1430 COFFEE BREAK

1500 **INVITED KEYNOTE 4**
Chair: Martin A. Trefzer, University of York, GB

1500 **CONFIGURABLE ANALOGUE DESIGN: CONQUERING VARIABILITY IN AN UNCERTAIN WORLD**
Speaker: Peter Wilson, university of southampton, GB

1540 **NETWORKING SESSION**
Chair: Martin A. Trefzer, University of York, GB

1540 **POSTER PRESENTATIONS OF THE SHORT TALKS FROM SESSIONS 1, 2 & 3.**

1620 **CLOSING SESSION**
Speaker: Andy M. Tyrrell, University of York, GB

FRIDAY 13 MARCH, 2015

DATE15
March 9 – 13, 2015, Grenoble, France
FRI

W08 W08 Heterogeneous Architectures and Design Methods for Embedded Image Systems

Sept Laux 4 0830 – 1700

General Co-Chairs

Dietmar Fey, Friedrich-Alexander University Erlangen-Nürnberg, DE
Frank Hannig, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Anton Lokhmotov, ARM Research, Cambridge, GB

Programme Committee Members

Albert Cohen, INRIA, FR
Andrew Davison, Imperial College London, GB
Diana Goehringer, Ruhr-University Bochum, DE
Richard Membarth, DFKI, Saarbrücken, DE
Muhammad Shafique, Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), DE
David Thomas, Imperial College London, GB
Zain Ul-Abdin, Halmstad University, SE
Dong Ping Zhang, AMD, Sunnyvale, CA, US

Mobile devices, such as smartphones and tablets, are ubiquitous in our everyday life. Such gadgets facilitate picture/video recording and playback, offer an almost inexhaustible number of applications using 2D and 3D graphics, and computer vision applications (e.g., face and object recognition, augmented reality). Other application areas of image systems, requiring highest computing capabilities while having stringent resource and power budgets as well as hard real-time constraints, are systems characterized by close-to-sensor processing, such as advanced driver assistance systems, mobile scanners, and smart devices used in medical and industrial imaging.

To scale computing performance in the future, the energy efficiency of images systems has to be significantly improved. This is why systems will be comprised more and more of heterogeneous hardware with specialized and different processor cores based on accelerators e.g. Digital Signal Processors (DSPs), embedded Graphics Processing Units (GPUs), FPGAs, or dedicated hardware. Furthermore, new 3D integrated circuit technologies are an emerging trend and allow for a higher integration of compute cores, memory and sensors to reduce communication latency, improve bandwidth leading to lower energy consumption. However, design and test, as well as parallel programming of such Heterogeneous Image Systems (HIS) are challenging tasks.

On the one hand, methodologies for designing novel hardware technologies and customizable architecture platforms are required. On the other hand, design methods are needed, which concentrate on algorithm development rather than on low level implementation details. Consequently, non-software engineering experts are shielded from the difficulty of parallel heterogeneous programming.

Topics of the workshop include, but are not limited to:

- Heterogeneous architectures of image systems
- 3D architectures and memory chip-stacked systems for image processing
- Architectures for smart cameras, smart sensors and close-to-sensor processing systems
- FPGA cameras, distributed smart camera systems
- Design methods and tools for heterogeneous image processing systems (embedded processors, DSPs, GPUs, FPGAs)
- Algorithm design for heterogeneous image processing
- Domain-specific programming abstractions and parallel patterns

The workshop will also present some of the architectures, tools, and results achieved in the DFG Research Training Group on Heterogeneous Image Systems (http://hbs.fau.de/lang-pref/en/) and the FP7 project CARP (http://carpproject.eu).

0830 **WELCOME AND INTRODUCTION**
Speakers: Dietmar Fey and Frank Hannig, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

0845 **KEYNOTE SPEECH 1**

0845 **VISION SENSORS WITH PIXEL-PARALLEL CELLULAR PROCESSOR ARRAYS**
Speaker: Piotr Dudek, University of Manchester, GB

0930 **SESSION 1: SMART VISION ARCHITECTURES AND HETEROGENEOUS MPSOCS**
Chair: François Berry, Université Blaise Pascal Clermont-Ferrand, FR

0930 **INVITED TALK: APPROACHING APPLICATION REQUIREMENTS WITH ADAPTIVE HETEROGENEOUS MPSOC**
Speaker: Diana Goehringer, Ruhr-University Bochum, DE

1000 **ESTIMATING THE POTENTIAL SPEEDUP OF COMPUTER VISION APPLICATIONS ON EMBEDDED MULTIPROCESSORS**
Authors: Vítor Schwambach[1], Cleyet-Merle Sebastien[2], Alain Issard[1] and Stéphane Mancini[3]
[1]STMicroelectronics, FR; [2]ST Micorelectronics, FR; [3]TIMA Laboratory, FR

1030 **COFFEE BREAK**

1100 **SESSION 2: DOMAIN-SPECIFIC LANGUAGES AND SCHEDULING TECHNIQUES FOR HETEROGENEOUS COMPUTING**
Chair: Frank Hannig, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1100 **INVITED TALK: ANYDSL: A COMPILER-FRAMEWORK FOR DOMAIN-SPECIFIC LIBRARIES & LANGUAGES (DSLLS)**
Speaker: Richard Membarth, DFKI, Saarbrücken, DE

1130 **A COMPARATIVE STUDY OF SCHEDULING TECHNIQUES FOR MULTIMEDIA APPLICATIONS ON SIMD PIPELINES**
Authors: Mehmet Ali Arslan, Flavius Gruian and Krzysztof Kuchcinski, Lund University, SE

1200 **LUNCH**

1300 **KEYNOTE SPEECH 2**

1300 **DREAMCAM: A MODULAR FPGA-BASED SMART CAMERA ARCHITECTURE**
Speaker: François Berry, Université Blaise Pascal Clermont-Ferrand, FR

1345 **SESSION 3: CAMERAS AND ACCELERATORS**
Chair: Piotr Dudek, University of Manchester, GB

1345 **INVITED TALK: ACCELERATED IMAGE PROCESSING: EXPERIENCE FROM THE CARP PROJECT**
Speaker: Elnar Hajiyev, Realeyes, GB

1415 **AUTOMATIC OPTIMIZATION OF HARDWARE ACCELERATORS FOR IMAGE PROCESSING**
Authors: Oliver Reiche, Konrad Häublein, Marc Reichenbach, Frank Hannig, Jürgen Teich and Dietmar Fey, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1445 **FAST-FORWARD PRESENTATION OF POSTERS**

1445 **EFFICIENT IMPLEMENTATION OF GIVENS QR DECOMPOSITION ON VLIW DSP ARCHITECTURE FOR ORTHOGONAL MATCHING PURSUIT IMAGE RECONSTRUCTION**
Authors: Mohamed Najoui, Anas Hatim, Mounir Bahtat and Said Belkouch, University of Cadi Ayyad, Marrakech, MA

1449 **A GRAPH-PARTITION BASED SCHEDULING POLICY FOR HETEROGENEOUS ARCHITECTURES**
Authors: Hao Wu, Daniel Lohmann and Wolfgang Schröder-Preikschat, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1453 **A HOLISTIC APPROACH FOR MODELLING AND SYNTHESIS OF IMAGE PROCESSING APPLICATIONS TO HETEROGENEOUS COMPUTING**
Authors: Christian Hartmann, Anna Yupatova, Marc Reichenbach, Dietmar Fey and Reinhard German, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

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1457 **GENERATION AND VALIDATION OF CUSTOM MULTIPLICATION IP BLOCKS FROM THE WEB**
Author: Minas Dasygenis, Department of Informatics and Telecommunications Engineering, University of Western Macedonia, Greece, GR

1500 **COFFEE BREAK AND POSTERS**

1600 **SESSION 4: TECHNOLOGIES FOR SMART SENSORS**
Chair: Dietmar Fey, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1600 **INVITED TALK: SMART AND ULTRAFAST CMOS IMAGE SENSORS: THE DREAM COME TRUE WITH 3D HETEROGENEOUS MICROELECTRONIC**
Speaker: Wilfried Uhring, Université de Strasbourg, FR

1630 **CONCEPT FOR A CMOS IMAGE SENSOR SUITED FOR ANALOG IMAGE PRE-PROCESSING**
Authors: Lan Shi[1], Christopher Soell[1], Andreas Baenisch[1], Robert Weigel[1], Jürgen Seiler[1] and Thomas Ussmueller[2]
[1]Friedrich-Alexander-Universität Erlangen-Nürnberg, DE; [2]University of Innsbruck, AT

1700 **CLOSING**

W09 International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)

Sept Laux 5 0830 — 1630

General Chairs **Gabriela Nicolescu,** Polytechnique Montréal, CA
Jiang Xu, Hong Kong University of Science and Technology, CN
Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

Programme Committee Chair
Mahdi Nikdast, Polytechnique Montréal, CA

Invited Speakers
Antonio La Porta, IBM, Zurich Research Laboratory, CH
Davide Bertozzi, University of Ferrara, IT
Fabiano Hessel, PUCRS, BR
Ian O'Connor, Lyon Institute of Nanotechnology, FR
John Ferguson, Mentor Graphics Corp, US
Josè Flich, Universidad Politecnica de Valencia, ES
Olivier Sentieys, INRIA - University of Rennes 1, FR
Sandro Bartolini, Università di Siena, IT
Sebastien Cremer, STMicroelectronics, FR
Yaoyao Ye, Huawei Technologies Co. Ltd., CN
Yvain Thonnart, CEA, LETI, MINATEC, FR

Multiprocessor System-on-Chip (MPSoC) is becoming the standard for high-performance computing systems. The performance of an MPSoC is determined not only by the performance of its processing cores and memories, but also by how efficiently they collaborate with one another. As the technology advances and allows the integration of many processing cores, metallic interconnects in MPSoCs will consume significant power while imposing high latency and low bandwidth. Shifting to the many-core era necessitates considering an alternative interconnect technology to replace the traditional electrical interconnects. Among such technologies, photonic technology has demonstrated promising potentials to address the aforementioned issues with the metallic interconnects in MPSoCs. In this context, high-performance silicon photonic devices, which are CMOS compatible, are necessary to construct photonic interconnect networks. Furthermore, it is required to explore the feasibility and performance of photonic interconnects as well as the guidelines and design requirements to realize such interconnects.

OPTICS aims at discussing the most recent advances in photonic interconnects for computing systems, covering topics from the device fabrication all the way up to the system-level design. The workshop is of interest to researchers working on silicon photonics and high-performance computing systems. It is comprised of invited talks of the highest caliber in addition to refereed paper presentations. Industry's and academia's views on the feasibility and recent progresses of optical interconnects will be discussed during the workshop.

Topics to be discussed in the workshop include (but are not limited to) the following:

- Design Methodology, Modelling and Tools: design space exploration, optimization, thermal-aware design, floor-planning, system level modelling and simulation.
- Architecture/Micro-Architecture: hybrid optical-electronic interconnects, passive/active-based optical switches networks, communication protocols.
- Applications: high-performance computing, photonics interconnect for memory.
- Silicon Photonics Devices: circuit demonstrator, on-chip lasers, photodetectors, electro-optic modulators, optical switches, athermal devices.
- Silicon Photonics Circuits: Optical switches and routers, high-bandwidth I/O.

0830 INTRODUCTION
Chair: Gabriela Nicolescu, Ecole Polytechnique de Montreal, CA

0830 INTRODUCTION TO OPTICS WORKSHOP
Speakers: Gabriela Nicolescu[1] and Mahdi Nikdast[2]
[1]Ecole Polytechnique de Montreal, CA; [2]Ecole Polytechnique de Montréal, CA

0840 MORNING SESSION ON SYSTEM DESIGN, ARCHITECTURE, MODELLING, AND APPLICATIONS
Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR, Contact Sébastien Le Beux

0840 SCALABLE OPTICAL INTERCONNECTS FOR COMPUTING SYSTEMS AND THE NEED FOR ELECTRO-OPTICAL INTEGRATION
Speaker: Antonio La Porta, IBM, Zurich Research Laboratory, CH

0915 TOWARDS A VERTICALLY INTEGRATED SYNTHESIS FLOW FOR PREDICTABLE DESIGN OF WAVELENGTH-ROUTED OPTICAL NOCS
Speaker: Davide Bertozzi, University of Ferrara, IT

0935 INTER/INTRA-CHIP OPTICAL NETWORKS: OPPORTUNITIES AND CHALLENGES
Speaker: Jiang Xu, Hong Kong University of Science and Technology, CN

0955 A FORCE-DIRECTED PLACEMENT ALGORITHM FOR 3D OPTICAL NETWORKS-ON-CHIP
Authors: Anja von Beuningen and Ulf Schlichtmann, Technische Universität München, DE

1015 SYSTEM-LEVEL DESIGN SPACE EXPLORATION FOR SOCS INTEGRATING OPTICAL NETWORKS ON CHIP
Speaker: Fabiano Hessel, Pontifícia Universidade Católica do Rio Grande do Sul, BR

1035 COFFEE BREAK

1100 MEET IN THE MIDDLE: LEVERAGING OPTICAL INTERCONNECTION OPPORTUNITIES IN CHIP MULTI PROCESSORS
Speaker: Sandro Bartolini, Università di Siena, IT

1120 ELECTRONIC VS PHOTONIC NOCS: SHOULD THEY COMPETE OR COLLABORATE?
Speaker: Josè Flich, Universidad Politecnica de Valencia, ES

1140 BANDWIDTH REQUIREMENTS IN MANYCORE ARCHITECTURES: WHAT CAN 3D BRING?
Speaker: Olivier Sentieys, INRIA - University of Rennes 1, FR

1200 LUNCH

1300 AFTERNOON SESSION ON SILICON PHOTONICS DEVICES, CIRCUITS, AND CHALLENGES
Chair: Jiang Xu, Hong Kong University of Science and Technology, CN, jia

1300 BUILDING A SCALABLE DESIGN ENVIRONMENT FOR SILICON PHOTONICS THROUGH PDKS
Speaker: John Ferguson, Mentor Graphics Corp, US

1335 RECENT DEVELOPMENT OF SI-PHOTONICS IN 300MM FAB
Speaker: Sebastien Cremer, STMicroelectronics, FR

1355 SILICON PHOTONICS FOR INTERPOSER
Speaker: Yvain Thonnart, CEA, LETI, MINATEC, FR

1415 THERMAL MANAGEMENT OF OPTICAL INTERCONNECTS
Speaker: Yaoyao Ye, Huawei Technologies Co. Ltd., CN

1435 COFFEE BREAK

1500 PARAMETRIC EXPLORATION OF VERTICAL TAPERED COUPLER FOR 3D OPTICAL INTERCONNECTION
Authors: Romain Schuster[1], Alberto Parini[2] and Gaetano Bellanca[2]
[1]Telecom Bretagne, Campus Brest, FR; [2]University of Ferrara, IT

1520 THE LAST MILE? REMAINING CHALLENGES IN OPTICAL INTERCONNECT
Speaker: Ian O'Connor, Lyon Institute of Nanotechnology, FR

1530 **PANEL**
Moderator: Ian O'Connor, Lyon Institute of Nanotechnology, FR

1530 **PANEL DISCUSSION**
Panelists: John Ferguson[1], Antonio La Porta[2], Gabriela Nicolescu[3], Olivier Sentieys[4], Davide Bertozzi[5] and Jiang Xu[6]
[1]Mentor Graphics Corp, US; [2]IBM, Zurich Research Laboratory, CH; [3]Ecole Polytechnique de Montreal, CA; [4]INRIA - University of Rennes [1], FR; [5]University of Ferrara, IT; [6]Hong Kong University of Science and Technology, CN

1620 **CONCLUDING REMARKS AND CLOSING SESSION**
Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

1620 **CONCLUDING REMARKS**
Speaker: Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

1630 **CLOSING**

FRIDAY 13 MARCH, 2015

DATE15
March 9 – 13, 2015, Grenoble, France
FRI

W10 TRUDEVICE 2015: Workshop on Trustworthy Manufacturing and Utilization of Secure Devices

Les Bans 0830 – 1700

General Chair **Giorgio Di Natale,** LIRMM, FR

General Vice-Chair
Ilia Polian, University of Passau, DE

Programme Committee Chair
Bossuet Lilian, University of St. Etienne, FR

Programme Committee Vice-Chair
Nicolas Sklavos, Technological Educational Institute of Patras, GR

Hardware security is becoming increasingly important for many embedded systems ranging from small RFID tag to satellites orbiting the earth. While secure applications such as public services, communication, control or healthcare keep growing, hardware devices that implement these applications become the Achille's heel of such systems.

The TRUDEVICE Workshop will provide an environment for researchers from academic and industrial domains who want to discuss recent findings, theories and on-going work on all aspects of hardware security including design, manufacturing, testing, reliability, validation and utilization. Program will include invited talks, contributed talks and work in progress. Topics of the workshop include but are not limited to:

- Manufacturing test of secure devices
- Trustworthy manufacturing of secure devices
- PUFs and TRNGs
- Hardware Trojans in IPs and ICs
- Reconfigurable devices for secure functions
- Fault attack injection, detection and protection
- Validation, Evaluation

The workshop will be organized in the framework of the COST Action IC1204 (TRUDEVICE). So far, we organized 2 workshops in the same context, the first in Avignon in conjunction with ETS'13 on May 30, 2013; the second as stand-alone event in Freiburg on December 12-13, 2013.

0830 **TRUDEVICE: TRUSTWORTHY MANUFACTURING AND UTILIZATION OF SECURE DEVICES**
Speakers: Giorgio Di Natale[1], Ilia Polian[2], Bossuet Lilian[3] and Nicolas Sklavos[4]
[1]LIRMM, FR; [2]University of Passau, DE; [3]University of St. Etienne, FR; [4]KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR

0845 **KEYNOTE TALK 1**
Chair: Giorgio Di Natale, LIRMM, FR, Contact Giorgio Di Natale

0845 **THE PROS AND CONS OF TECHNOLOGICAL DISPERSION FOR SECURITY: PUF, TRNG AND SIDE-CHANNEL COUNTERMEASURES**
Author: Jean-Luc Danger, Télécom ParisTech, FR

0930 **SESSION 1**
Chair: Bossuet Lilian, University of St. Etienne, FR, Contact Bossuet Lilian

0930 **ANALYSIS AND UTILIZATION OF DEVIATIONS IN RO-PUFS UNDER ALTERED FPGA DESIGNS**
Authors: Linus Feiten, Tobias Martin and Bernd Becker, University of Freiburg, DE

0945 **RING OSCILLATORS ANALYSIS FOR FPGA SECURITY PURPOSES**
Authors: Mario Barbareschi[1], Lionel Torres[2] and Giorgio Di Natale[3]
[1]University of Naples Federico II, IT; [2]LIRMM - University Montpellier [2], FR; [3]LIRMM, FR

1000 **ENHANCED TERO-PUF DESIGN AND CHARACTERIZATION WITH FPGA**
Authors: Cedric Marchand, Abdelkarim Cherkaoui and Bossuet Lilian, University of St. Etienne, FR

1015 **IMPLEMENTING RELIABLE MECHANISMS FOR IP PROTECTION ON LOW-END FPGA DEVICES**
Authors: Mario Barbareschi, Antonio Mazzea and Pierpaolo Bagnasco, University of Naples Federico II, IT

1030 **POSTER SESSION 1**
Chair: Ilia Polian, University of Passau, DE, Contact Ilia Polian

1030 **FUNCTIONAL LOCKING MODULES FOR DESIGN PROTECTION OF INTELLECTUAL PROPERTY CORES**
Authors: Brice Colombier and Bossuet Lilian, University of St. Etienne, FR

1030 **3D-NOC PROTECTION CAPABILITIES AND THREATS: THE TSV RISK**
Authors: Martha Johanna Sepulveda[1], Guy Gogniat[2] and Marius Strum[1]
[1]University of São Paulo, BR; [2]Universite de Bretagne-Sud / Lab-STICC, FR

1030 **HARDWARE TROJANS IN TRNGS**
Authors: Honorio Martin[1], Pedro Paris-Lopez[1], Enrique San Millan[1], Juan E. Tapidor[1] and Nicolas Sklavos[2]
[1]University Carlos III of Madrid, ES; [2]KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR

1030 **DEVELOPMENT OF A LAYOUT-LEVEL HARDWARE OBFUSCATION TOOL**
Authors: Shweta Malik[1], Georg T. Becker[2], Christof Paar[2] and Wayne P. Burleson[1]
[1]University of Massachusetts, US; [2]Horst Görtz Institute for IT-Security, Ruhr-University Bochum, DE

1030 **GET - PROGRAM FOR THE GENERATION AND ANALYSIS ON NONLINEAR ELEMENTS**
Authors: Stjepan Picek[1] and Lejla Batina[2]
[1]Faculty of Electrical Engineering and Computing, HR; [2]Radboud University Nijmegen, NL

1030 **WHY YOU SHOULD CARE ABOUT LEADING-EDGE SOFTWARE ENGINEERING?**
Author: Tiziana Margaria, University of Limerick (Ireland) and Lero - The Irish Software Research Center, IE

1030 **ERROR DETECTION AND CORRECTION FOR LIGHTWEIGHT CRYPTOGRAPHIC ALGORITHMS**
Authors: Francesco Regazzoni[1], Andrey Bogdanov[2], Luca Breveglieri[3] and Israel Koren[4]
[1]Université catholique de Louvain and ALaRI, CH; [2]Technical University of Denmark, DK; [3]Polimi, IT; [4]University of Massachusetts, US

1030 **FINE GRAIN PARTIAL RECONFIGURATION FOR FAULT EMULATION AND PRECISE LUT MODIFICATION**
Authors: L.A. Cardona[1], Bibiana Lorente[2] and C. Ferrer[3]
[1]IEEC-UAB, ES; [2]CNM-CSIC, ES; [3]EEC-UAB, ES

1130 **SESSION 2**
Chair: Nicolas Sklavos, KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR

1130 **HIERARCHICAL SECURE DFT**
Authors: Mafalda Cortez[1], Said Hamdioui[2], Giorgio Di Natale[3], Marie-Lise Flottes[3] and Bruno Rouzeyre [3]
[1]TU Delft, NL; [2]Delft University of Technology, NL; [3]LIRMM, FR

1200 **INTEGRATED SENSORS: A BACKDOOR FOR HARDWARE TROJAN ACTIVATION**
Authors: Xuan-Thuy Ngo, Zakaria Najm, Shivam Bhasin, Sylvain Guilley and Jean-Luc Danger, Télécom ParisTech, FR

1300 **KEYNOTE TALK 2**
Chair: Ilia Polian, University of Passau, DE

1300 **PROTECTING CRYPTOGRAPHIC IMPLEMENTATIONS ON RECONFIGURABLE DEVICES**
Author: Tim Güneysu, Ruhr University Bochum, DE

1345 **SESSION 3**
Chair: Bossuet Lilian, University of St. Etienne, FR, Contact Bossuet Lilian

1345 **TOWARDS GENERIC COUNTERMEASURES AGAINST FAULT INJECTION ATTACKS**
Authors: Pablo Rauzy and Sylvian Guilley, Télécom ParisTech, FR

1400 **ANALYSIS OF LASER-INDUCED ERRORS: RTL FAULT MODEL VERSUS LAYOUT LOCALITY CHARACTERISTICS**
Authors: Athanasios Papdimitriou[1], David Hely[2], Vincent Beroulle[2], Paolo Maistri[3] and Regis Leveugle[3]
[1]Univ. Grenoble Alpes, LCIS Laboratory, FR; [2]Univ. Grenoble Alpes, FR; [3]TIMA Laboratory, FR

1415 **SENSITIVITY TO FAULT LASER INJECTION: A COMPARISON BETWEEN 28NM BULK AND FD-SOI TECHNOLOGY**
Authors: Stephan De Castro and Giorgio Di Natale, LIRMM, FR

1430 **DYNAMIC FAULT MODEL FOR LONG DURATION LASER-INDUCED FAULT SIMULATION**
Authors: Feng Lu, Giorgio Di Natale, Marie-Lise Flottes and Bruno Rouzeyre , LIRMM, FR

1430 **POSTER SESSION 2**
Chair: Nicolas Sklavos, KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR

1430 **A NOVEL SCHEDULING POLICY FOR THWARTING DIFFERENTIAL POWER ANALYSIS ATTACKS**
Author: Ke Jiang, Linköping University, SE

1430 **EXPLORING RNS IN THE DESIGN OF IMPROVED RSA IMPLEMENTATIONS**
Authors: Juvenal Araujo, Pedro Matutino, Leonel Sousa and Ricardo Chaves, INESC-ID, IST, Universidade de Lisboa, PT

1430 **CAESAR AND NORX – DEVELOPING THE FUTURE OF AUTHENTICATED ENCRYPTION**
Authors: Jean-Philippe Aumasson[1], Philipp Jovanovic[2] and Samuel Neves[3]
[1]Kudelski Security, CH; [2]University of Passau, DE; [3]University of Coimbra, GR

1430 **POWER AND ELECTROMAGNETIC ANALYSIS FOR ONLINE TEMPLATE ATTACKS**
Authors: Margaux Dugardin[1], Louiza Papachristodoulou[2], Zakaria Najm[1], Lejla Batina[3], Jean-Luc Danger[1], Sylvain Guilley[1], Jean-Christophe Courrege[4], Anne-Sophie Rivemale[4] and Carine Therond[4]
[1]Télécom ParisTech, FR; [2]Radboud University Nijmegen,, NL; [3]Radboud University Nijmegen, NL; [4]Thales Communications & Security, FR

1430 **SEARCH STRATEGY FOR FAULT INJECTION USING MEMETIC ALGORITHMS**
Authors: Stjepan Picek[1], Pieter Buzing[2] and Lejla Batina[3]
[1]Faculty of Electrical Engineering and Computing, HR; [2]Riscure BV, NL; [3]Radboud University Nijmegen, NL

1430 **INSIGHTS INTO THE CORRELATION BETWEEN THE PROCESSED DATA AND ITS POWER TRACES**
Authors: Miryam Haber, Binyamin Frankel, Moshe Avital, Itamar Levi, Osnat Keren and Alexander Fish, Bar-Ilan University, IL

1430 **TUNING OF RANDOMIZED WINDOWS AGAINST SIMPLE POWER ANALYSIS FOR SCALAR MULTIPLICATION ON ELLIPTIC CURVES**
Authors: Simon Pontie[1], Paolo Maistri[2] and Regis Leveugle[2]
[1]University Grenoble Alpes, FR; [2]TIMA Laboratory, FR

1500 **SESSION 4**
Chair: Giorgio Di Natale, LIRMM, FR

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1500 PUBLIC KEY CRYPTOGRAPHIC PRIMITIVE DESIGN AND PROTECTION AGAINST FAULT AND POWER ANALYSIS ATTACKS
Authors: Apostolos P. Fournaris and Nicolas Sklavos, KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR

1515 ON THE USE OF ERROR DETECTING AND CORRECTING CODES TO BOOST SECURITY IN CACHES AGAINST SIDE CHANNEL ATTACKS.
Authors: Madalin Neagu[1], Salvador Manich[2] and Liniu Miclea[1]
[1]Technical University of Cluj-Napoca, RO; [2]Universitat Politecnica de Catalunya, ES

1530 A SIDE-CHANNEL ATTACK AGAINST SECRET PERMUTATION ON AN EMBEDDED MCELIECE CRYPTOSYSTEM
Authors: Tania Richmond[1], Martin Petrvalsky[2] and Milos Drutarovsky[2]
[1]Univ. St. Etienne, FR; [2]Technical University of Kosic, SK

1545 SESSION 5
Chair: Nicolas Sklavos, KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR

1545 INVESTIGATING TERO FOR HARDWARE TROJAN HORSE DETECTION
Authors: Paris Kitsos[1] and Artemios G. Voyiatzis[2]
[1]Technological Educational Institute of Western Greece, GR; [2]ISI, GR

1600 INSERTION AND EVALUATION OF HARDWARE TROJANS IN PROCESSORS
Authors: Ioannis Voyiatzis, Costas Efstathiou and Thanos Milidonis, Technological Educational Institute of Athens, GR

1615 SECURITY OF ICS FROM HARDWARE TROJANS
Authors: Georgina Kalogeridou[1], Andrew W. Moore[1], Nicolas Sklavos[2] and Odysseas Koufopavlou[3]
[1]Computer Laboratory, University of Cambridge, GB; [2]KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR; [3]University of Patras, GR

1630 HINT: HOLISTIC APPROACHES FOR INTEGRITY OF ICT-SYSTEMS
Authors: Ingrid Verbauwhede and Dave Singelee, KU Leuven and UCLA, BE

1645 CLOSING SESSION

1645 CONCLUSIONS & OUTLOOK: ROUND TABLE
Speakers: Giorgio Di Natale[1], Ilia Polian[2], Bossuet Lilian[3] and Nicolas Sklavos[4]
[1]LIRMM, FR; [2]University of Passau, DE; [3]University of St. Etienne, FR; [4]KNOSSOSnet Research Group / Technological Educational Institute of Western Greece, GR"

EXHIBITION THEATRE PROGRAMME

Organiser: **Jürgen Haase,** edacentrum GmbH, DE

In addition to the conference programme during DATE 2015, there will be a presentation theatre as part of the exhibition from Tuesday 10 March to Thursday 12 March 2015. Attendees will benefit from having an industry forum in the midst of Europe's leading electronic systems design event. The theatre is located in Room Lesdiguières, which is within the exhibition hall and affords easy access for exhibition visitors as well as for conference delegates.

Like in previous years, open Special Conference Sessions from Track 8 (full details are contained in the main conference programme pages) will take place in the Exhibition Theatre. This includes an executive panel session (6.6: The Future of Electronics, Semiconductor, and Design in Europe) and three hot topic sessions (3.8 - Design Methodologies for a Cyber-Physical Systems Approach to Personalized Medicine-on-a-Chip; 5.8 - The next generation of virtual prototyping: Ultra-fast yet accurate simulation of HW/SW systems; 9.8 - Monolithic 3D: A Path to Real 3D Integrated Chips).

In seven special Exhibition Theatre sessions DATE15 exhibition will highlight an Exhibition Keynote from MathWorks (11.8), three Exhibition Panels on FDSIO Technology (2.8, presented by STMicroelectronics and partners), IP Management (7.8, presented by Design&Reuse) and on Systems for the Connected Autonomous Future (11.8, presented by MathWorks), two Best Practice sessions (4.8 on Interdisciplinary Research, presented by Cadence Academic Network; 8.8 on Multi Project Wafers, presented by CMP and IMEC) and a Tutorial on FPGA/ARM System Development (12.8, presented by MathWorks).

The sessions of DATE 2015 Exhibition Theatre are open to conference delegates as well as to exhibition visitors. Please review below information on the Exhibition Theatre sessions. The full programme with all the details of the exhibition sessions is available on the DATE web portal.

Exhibition Theatre

2.8	Facilities for Design and Fabrication for FDSOI IC	TUE 1130-1300
3.8	Hot Topic – Design Methodologies for a Cyber-Physical Systems Approach to Personalized Medicine-on-a-Chip: Challenges and Opportunities	TUE 1430-1600
4.8	Strength by Interdisciplinary Research: The Cadence Academic Network	TUE 1700-1830
5.8	Hot Topic – The Next Generation of Virtual Prototyping: Ultra-fast yet Accurate Simulation of HW/SW Systems	WED 0830-1000
6.6	Panel – The Future of Electronics, Semiconductor, and Design in Europe **Different room: Bayard**	WED 1100-1230
7.8	Critical Research Areas Driven by Industry Transformations	WED 1430-1600
8.8	Share a Fab – Multi Project Wafers Enable Your Innovations	WED 1700-1830
9.8	Hot Topic – Monolithic 3D: A Path to Real 3D Integrated Chips	THU 0830-1000
10.8	From IP to EDA Tools Enterprise Management: What is so special?	THU 1100-1230
11.8	Exhibition Keynote: Designing Systems for the Connected Autonomous Future	THU 1400-1500
12.8	Tutorial: An Industry Approach to FPGA/ARM System Development and Verification	THU 1500-1730

2.8 Facilities for Design and Fabrication for FDSOI IC

Salle Lesdiguières 1130 - 1300

Organiser: **Ahmed Jerraya,** CEA Leti, FR
Moderator: **Carlos Mazure,** Soitec, FR
Panelists: **Giorgio Cesana,** STMicroelectronics, FR
Gerd Teepe, GLOBALFOUNDRIES, DE
Patrick Blouet, STMicroelectronics, FR
Olivier Thomas, CEA-Leti, Minatec, FR

FDSOI enable dramatically improved ICs performances at a much lower cost and power consumption than new leading-edge CMOS technology below 28 nm transistor fabrication. The success of these new ICs depends on the availability of new tools, flows, platforms, methodologies and skills that are required to achieve acceptable design quality and productivity. This introduces the FDSOI ecosystem and show current facilities for design and fabrication for FDSOI IC.

3.8 Hot Topic - Design Methodologies for a Cyber-Physical Systems Approach to Personalized Medicine-on-a-Chip: Challenges and Opportunities

Salle Lesdiguières 1430 - 1600

Organiser: **Krishnendu Chakrabarty,** Duke University, US
Chair: **Paul Pop,** Technical University of Denmark, DK
Co-Chair: **Mohammad Abdullah Al Faruque,** University of California Irvine, US

Modern stressful and sedentary lifestyles coupled with inadequate, irregular and inappropriate sleep patterns and diet have contributed not only to increased prevalence of chronic diseases but also to increased healthcare costs. To address these emerging clinical and healthcare challenges, in this special session, we advocate for a cross-disciplinary approach to cyber-physical systems design (CPS) aiming at seamlessly and safely integrate sensing, computation, communication, control and actuation for developing new technology for personalized and precise medicine.

4.8 Strength by Interdisciplinary Research: The Cadence Academic Network

Salle Lesdiguières 1700 - 1830

Organiser: **Patrick Haspel,** Cadence Academic Network, US
Chair: **Jürgen Haase,** edacentrum GmbH, DE

The Academic Network was launched by Cadence in 2007. The aim was to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence was established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems.

Specific examples of research directions in the cadence academic network will be given in three talks.

5.8 Hot Topic - The Next Generation of Virtual Prototyping: Ultra-fast yet Accurate Simulation of HW/SW Systems

Salle Lesdiguières 0830 - 1000

Organisers: **Oliver Bringmann,** University of Tübingen, DE
Daniel Müller-Gritschneder, Technische Universitaet München, DE
Chair: **Andy D. Pimentel,** University of Amsterdam, NL
Co-Chair: **Christian Haubelt,** University of Rostock, DE

This session addresses leading-edge solutions in the field of virtual prototyping. Employing techniques such as source-level software simulation, host-compiled firmware, OS and processor modeling, as well as abstract communication and peripheral models, it is possible to reach very high simulation speeds. With intelligent new out-of-order modeling, synchronization and temporal decoupling techniques, such ultra-fast simulation can be achieved while also maintaining a very high accuracy.

7.8 Critical Research Areas Driven by Industry Transformations

Salle Lesdiguières 1430 - 1600

Organiser: **John Zhao,** MathWorks, US

Increasing demands of electrification arise from connected vehicles, medical devices, smart-grid and microgrid technologies, and the IoT evolution of devices into smart, interconnected systems. Those systems must meet market requirements for not only more sophisticated functionality, but also improved performance and robustness. As a result, companies need to transform how they design, analyze, implement, and verify their systems. At the same time, embedded-system platforms have become increasingly diverse combinations of digital/analog electronics and software, ranging from FPGA/ARM platforms (e.g,. Xilinx Zynq and Altera SoC) to a diverse range of heterogeneous manycore systems.

To help companies leverage these trends in their product and system development, EDA and embedded-system researchers are called upon to focus their research on new kinds of issues that arise. This panel will explore the key research needs and opportunities that come from the transformations that industries must embrace.

8.8 Share a Fab - Multi Project Wafers Enable Your Innovations

Salle Lesdiguières 1700 - 1830

Moderator: **Jürgen Haase,** edacentrum GmbH, DE

Today most innovations in the major industries include the use of dedicated chips. However, extremely high IC fabrication costs and foundries accepting only orders with high quantities are substantial obstacles for innovations developed from SMEs, start-ups, universities and research organisations.

The solution is that many of these innovators team up and share a fab run by using the opportunities offered by Multi Project Wavers (MPWs). European service providers like Europractice and CMP provide the access to MPW runs as well as the required know-how and tooling.

In the tutorial part of this session first-time users as well as experienced users will be provided with comprehensive information about the available semiconductor technologies, new design methodologies and possible applications. In the best practice part of the session users of such services will share their experience with the MPW concept with the audience and present projects and products realized by utilizing MPW opportunities.

9.8 Hot Topic - Monolithic 3D: A Path to Real 3D Integrated Chips

Salle Lesdiguières 0830 - 1000

Organisers: **Pierre-Emmanuel Gaillardon,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH
Chair: **Giovanni De Micheli,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Co-Chair: **Ian O'Connor,** Institut des Nanotechnologies de Lyon, FR

As compared to standard 3D technologies, 3D Monolithic Integration (3DMI) overcomes the vertical connectivity challenge through the use of nano-scale inter-layer vias, which are orders-of-magnitude smaller than TSVs. In this hot topic session, we cover 3DMI for actual (FDSOI) and emerging (CNFETs and RRAM) technologies, and identify its promises from a design perspective.

10.8 From IP to EDA Tools Enterprise Management: What is so special?

Salle Lesdiguières 1100 - 1230

Moderator: **Gabrièle Saucier,** Design and Reuse, FR
Panelists: **Huy-Nam Nguyen,** Bull S.A.S., FR
Philippe Quinio, STMicroelectronics International, CH

IPs are today part of any Electronic Systems and it is more and more urgent to trace, monitor and more generally "manage" IPs in systems or products. The key feature of such a management is its multidisciplinary facet implying multiple management views and actors (IP Engineering, IP Sourcing, IP Procurement..).

EXHIBITION SESSIONS

Today an IP management platform needs to be a next generation web application hosted on an intranet server and receiving data from multiple sources (Design DB, IP Delivery DB, Product Shipment DB, Legal and Financial reports..). It aims at providing a reliable follow up to all of these departments such as IP Entry, IP Delivery, IP tracing in products… It delivers results (fee and royalty calculation for instance) as well as expertise for decision making (planning the future in terms of IP expenses, cost per product..).

The introductory talk will show how such a portal can be configured to fulfill the needs of an enterprise and what are the required "special" technical features missing in management tools presently available on the market.

Specific views namely Engineering view and Legal aspects will be commented by 2 speakers from companies veteran in IP management.

It will also be demonstrated that an amazing and straightforward extension concerns EDA Tool license management and optimization including integrated license monitoring. Such an extension aims at optimizing the tool cost for large enterprises using extensively and at a large scale a variety of development tools and gives an unique corporate global view on IP and Tools.

11.8 Exhibition Keynote: Designing Systems for the Connected Autonomous Future: An Industry Perspective

Salle Lesdiguières 1400 - 1500

Organiser: **John Zhao,** MathWorks, US
Chair: **Jürgen Haase,** edacentrum GmbH, DE

Speaker to be announced in the online programme.

Will I ever travel in an autonomous vehicle? Will my refrigerator really order food automatically from my grocery store? Can the watch I wear in the future warn me about an impending heart attack? Innovations at the SoC and board level are poised to provide the necessary computational power with low cost and high flexibility to make these products. However, designing the systems of the future -- whether an automobile, connected industrial machinery, medical device, consumer electronics, or an aerospace guidance system -- requires advances not only in embedded systems and software, but how they are designed and verified.

In this keynote, an expert from industry will discuss trends and innovations in systems that are incorporating more electronic content than ever before, and describe model-based development approaches that companies are using to create the system functionality that will power our connected autonomous future.

12.8 Tutorial: An Industry Approach to FPGA/ARM System Development and Verification

Salle Lesdiguières 1500 - 1730

Organiser: **John Zhao,** MathWorks, US

MATLAB and Simulink provide a rich environment for embedded-system development, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as MPSoC. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows. Functional verification throughout the design process improves coverage and test-case generation while reducing the time and resources required.

In this set of tutorial sessions, you will learn

- How to implement an application that leverages the FPGA and ARM core of a Zynq SOC
- The flexibility and diversity of the approach through examples that include prototyping a motor control algorithm and a video-processing algorithm.
- A HW/SW co-design workflow that combines system level design and simulation with automatic code generation
- Successful use of the HW/SW co-design workflow in commercial development
- Functional verification using MATLAB and Simulink in a SystemVerilog workflow illustrated by a detailed example

UNIVERSITY BOOTH

The University Booth is organised during DATE and will be located in booth 4 of the exhibition area. All demonstrations will take place from Tuesday, March 10 to Thursday, March 12, 2015 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 39 demonstrations from 14 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover four major topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Designing Electronics for the Internet of Things
- Designing Electronics for Medical Applications

The University Booth at DATE 2015 invites you to booth 4 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information can be found online at www.date-conference.com/group/exhibition/u-booth. A University Booth programme flyer will be included in the conference bags. The following demonstrators will be presented at the University Booth.

3D-COSTAR: USING 3D-COSTAR FOR 2.5D-/3D-SIC COST ANALYSIS

Mottaqiallah Taouil[1], Mottaqiallah Taouil[1], Said Hamdioui[1] and Erik Jan Marinissen[2]
[1]TU Delft, NL; [2]IMEC, BE

4-LOOP: 4-CORE LEON 3 WITH LINUX OPERATING SYSTEM, OPENMP LIBRARY AND HARDWARE PROFILING SYSTEM

Giacomo Valente, Vittoriano Muttillo and Fabio Federici, University of L'Aquila, IT

A FRAMEWORK FOR THE EMULATION AND PROTOTYPING OF NANO-PHOTONIC OPTICAL ACCELERATORS

Alberto Garcia-Ortiz[1], Wolfgang Büter[2], A. Ali[3], S Mahmood[3], S. Arefin[3], V. V. Parsi Sreenivas[3], M. Mike Bülters[4] and R.-B. Bergmann[4]
[1]University of Bremen, DE; [2]Institute for Electrodynamics and Microelectronics Systems (ITEM), DE; [3]University of Bremen, Physics/Electrical Engineering, DE; [4]Bremer Institut für angewandte Strahltechnik GmbH, DE

AIDASOFT: ANALOG IC DESIGN AUTOMATION

Nuno Horta[1], Nuno Lourenço[1], Ricardo Martins[1], Ricardo Póvoa[1], António Canelas[1], Ricardo Lourenço[2] and Pedro Ventura[2]
[1]Instituto de Telecomunicações/Instituto Superior Técnico, PT; [2]Instituto de Telecomunicações, PT

AN FPGA LAB-ON-CHIP: AN ANALYSIS TOOL AND FRAMEWORK FOR ADVANCED MEASUREMENTS AND RELIABILITY ASSESSMENTS ON MODERN NANOSCALE FPGAS

Petr Pfeifer, Technical University of Liberec, CZ

BONDCALC: THE BOND CALCULATOR

Carl Christoph Jung[1], Christian Silber[2] and Juergen Scheible[1]
[1]Reutlingen University, DE; [2]Robert Bosch GmbH, DE

UNIVERSITY BOOTH

COMBINATION OF WSN AND 1ST ORDER KINETIC MODEL FOR REAL-TIME SHELF-LIFE PREDICTION OF PERISHABLE GOODS
Valerio Francesco Annese and Daniela De Venuto, Politecnico di Bari, IT

CRYPTOCHIP: DEMONSTRATION OF CRYPTOGRAPHIC ASIC PROTOTYPE
Xuan Thuy Ngo, Xuan Thuy Ngo, Jean-Luc Danger, Sylvain Guilley, Tarik Graba, Yves Mathieu and Zakaria Najm, Télécom ParisTech, FR

DESIGNING AND EVALUATING RESOURCE MANAGEMENT POLICIES FOR HETEROGENEOUS SYSTEM ARCHITECTURES
Gianluca Durelli, Cristiana Bolchini, Antonio Miele, Gabriele Pallotta, Marcello Pogliani and Marco Santambrogio, Politecnico di Milano, IT

FLARE: A RECONFIGURATION AWARE FLOORPLANNER
Riccardo Cattaneo, Marco Rabozzi and Marco Santambrogio, Politecnico di Milano, IT

FUNCTIONAL ECO: AN EFFICIENT REWIRING ENHANCED FUNCTIONAL ECO
Tak Kei Lam[1], Xing Wei[2], Yi Diao[2], Tak Kei Lam[1] and Yu-Liang Wu[2]
[1]The Chinese University of Hong Kong, HK; [2]Easy-Logic Technology Limited, HK

GESTURE RECOGNITION BASED ROBOTIC EMBEDDED SYSTEM
Seetal Potluri[1], Ravindran Balaraman[1], Pradyot K. V. N.[1], Manimaran S. S. [1], Praharasan Raja[1], Anshul Bansal[2] and Abhishek Mehta[2]
[1]IIT Madras, IN; [2]Punjab Engineering College, IN

HIPER-NIRGAM: A TOOL CHAIN BASED FRAMEWORK FOR MODELING THERMAL-AWARE RELIABILITY ESTIMATION IN 2D MESH NOCS
Ashish Sharma[1], Manoj Singh Gaur[1], Lava Bhargava[1], Vijay Laxmi[1] and Mark Zwolinski[2]
[1]Malaviya National Institute of Technology, Jaipur, IN; [2]University of Southampton, GB

ID.FIX: AN EDA TOOL FOR FIXED-POINT REFINEMENT OF EMBEDDED SYSTEMS
Olivier Sentieys[1], Daniel Menard[2] and Nicolas Simon[1]
[1]INRIA, FR; [2]INSA Rennes, FR

IMPLEMENTATIONS OF THE SEMI-GLOBAL MATCHING 3D VISION ALGORITHM FOR AUTOMOTIVE APPLICATIONS
Affaq Qamar and Luciano Lavagno, Politecnico di Torino, IT

INTERACTIVE VISUALIZATION OF ESL DESIGNS
Jannis Stoppe[1], Robert Wille[2] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen/DFKI GmbH, DE

ISIS: CUSTOMIZABLE RUNTIME VERIFICATION OF HARDWARE/SOFTWARE VIRTUAL PLATFORMS
Laurence PIERRE and Martial Chabot, TIMA, FR

ISP RAS VERIFICATION TOOLS: INTEGRATED APPROACH TO HARDWARE VERIFICATION AT UNIT AND SYSTEM LEVELS BASED ON STATIC AND DYNAMIC METHODS
Andrei Tatarnikov, Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak and Sergey Smolov, Institute for System Programming of the Russian Academy of Sciences (ISP RAS), RU

LINUX ON TSAR: PORTING THE LINUX KERNEL TO THE TSAR MANYCORE ARCHITECTURE
César Fuguet Tortolero, Joël Porquet and Alain Greiner, UPMC-LIP6, FR

MAMMA: SPEECH ENHANCEMENT DEMO EXPLOITING MEMS MICROPHONE ARRAY FOR PEOPLE WITH DISABILITIES
Luca Fanucci[1], Alessandro Palla[1], Luca Fanucci[1] and Roberto Sannino[2]
[1]University of Pisa, IT; [2]STMicroelectronics, IT

UNIVERSITY BOOTH

NETFPGA SUME: NETFPGA SUME: MAKING 100GBPS A COMMODITY
Noa Zilberman, Yury Audzevich, Georgina Kalogeridou and Andrew W. Moore, University of Cambridge, GB

NUMERICAL METHODS FOR EFFICIENT SIMULATIONS OF CIRCUITS WITH SEPARATED TIME SCALES
Genie Hsieh, Sandia National Laboratories, US

ODEN: ASSERTION MINING FOR BEHAVIORAL DESCRIPTIONS
Alessandro Danese, Alessandro Danese, Tara Ghasempouri and Graziano Pravadelli, University of Verona, IT

ORIENTOMA: A WEARABLE ORIENTATION SYSTEM FOR BLIND AND VISUALLY IMPAIRED PEOPLE
Giuseppe AiroFarulla, Marco Indaco and Ludovico Russo, Politecnico di Torino, IT

OSTC: COMBINING HIFSUITE AND SCNSL FOR SMART DEVICE INTEGRATION AND SIMULATION
Graziano Pravadelli, Alessandro Danese, Franco Fummi, Valerio Guarnieri, Michele Lora, Graziano Pravadelli and Francesco Stefanni, University of Verona, IT

PARLOMA: A REMOTE COMMUNICATION SYSTEM FOR DEAFBLIND PEOPLE
Ludovico Orlando Russo[1], Giuseppe Airò Farulla[1], Marco Indaco[1], Calogero Maria Oddo[2], Daniele Pianu[3], Paolo Prinetto[1], Stefano Rosa[1] and Ludovico Orlando Russo[1]
[1]Politecnico di Torino, IT; [2]Scuola Superiore Sant'Anna, The Biorobotics Institute, IT; [3]CNR, IEIIT, IT

REAL-TIME MULTIPROCESSOR COMPILER DEMO: COMPILER FOR REAL-TIME MULTIPROCESSOR SYSTEMS WITH SHARED ACCELERATORS
Bekooij Marco, Guus Kuiper, Stefan Geuns, Philip Wilmanns, Joost Hausmans and Marco Bekooij, University of Twente, NL

REAL-TIME PATTERN DETECTION OF MOVEMENT RELATED POTENTIALS BY SYNCHRONIZED EEG AND EMG
Valerio Francesco Annese and Daniela De Venuto, Politecnico di Bari, IT

RECONFIGURABLE FPGA-BASED NON-INTRUSIVE BERT FOR PRODUCTION TEST
Sergei Odintsov and Artjom Jasnetski, Tallinn University of Technology, EE

RSOC FRAMEWORK: FRAMEWORK FOR RAPID PROTOTYPING OF APPLICATIONS ON RECONFIGURABLE SOCS
Korcek Pavol, Jan Viktorin, Vlastimil Kosar and Jan Korenek, Brno University of Technology, CZ

SMART CELL DEVELOPMENT PLATFORM FOR EMBEDDED BATTERY MANAGEMENT
Swaminathan Narayanaswamy[1], Matthias Kauer[1], Sebastian Steinhorst[1], Martin Lukasiewycz[1] and Samarjit Chakraborty[2]
[1]TUM CREATE, SG; [2]TU Munich, DE

STRNG: A SELF-TIMED RING BASED TRUE RANDOM NUMBER GENERATOR WITH MONITORING AND ENTROPY ASSESSMENT
Abdelkarim Cherkaoui[1], Laurent Fesquet[2], Viktor Fischer[3] and Alain Aubert[3]
[1]TIMA, FR; [2]TIMA, FR; [3]LaHC, FR

SYSTEM-LEVEL FPGA PROTOTYPING OF ANALOG/MIXED-SIGNAL SYSTEMS
Georg Gläser[1], Eckhard Hennig [1] and Vojtech Dvorak[2]
[1]Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE; [2]Brno University of Technology, CZ

UNIVERSITY BOOTH

THE Ψ-CHART DESIGN APPROACH IN TTOOL/DIPLODOCUS: A FRAMEWORK FOR HW/SW CO-DESIGN OF DATA-DOMINATED SYSTEMS-ON-CHIP

Andrea Enrici, Ludovic Apvrille, Daniel Camara and Renaud Pacalet, Télécom ParisTech, FR

VDA-ADMF: AN AGILE MIGRATION FRAMEWORK FOR ANALOG LAYOUT DESIGN

Po-Cheng Pan[1], Ching-Yu Chin[1], Hung-Ming Chen[1], Tung-Chieh Chen[2], Jou-Chun Lin[2] and Yi-Peng Weng[3]
[1]National Chiao Tung University, TW; [2]Synopsys Co., Ltd., TW; [3]Taiwan Semiconductor Manufacturing Company, TW

VHDL TO SYSTEMC TRANSLATION AND ABSTRACTION: SYSTEMC MANIPULATION FRAMEWORK: FROM RTL VHDL TO OPTIMIZED TLM SYSTEMC

Syed Saif Abrar, Syed Saif Abrar, Valentin Tihhomirov, Maksim Jenihhin and Jaan Raik, Tallinn University of Technology, EE

WHERE IS IT? FIND THE CODE YOU ARE INTERESTED IN!

Jan Malburg[1] and Görschwin Fey[2]
[1]University of Bremen, DE; [2]University of Bremen / German Aerospace Center, DE

WORKCRAFT: WORKCRAFT: FRAMEWORK FOR INTERPRETED GRAPHS

Danil Sokolov, Newcastle University, GB

XTSI: THE 3-D ELECTRO-THERMAL SIMULATOR

Jürgen Scheible and Carl Christoph Jung, Reutlingen University, DE

See you at the University Booth!

University Booth Co-Chairs	**Laurent Fesquet,** TIMA and CIME Nanotech, FR **Andreas Vörg,** edacentrum GmbH, DE
Contacts:	**Laurent Fesquet,** TIMA and CIME Nanotech, FR **Andreas Vörg,** edacentrum GmbH, DE university-booth@date-conference.com

FRINGE TECHNICAL MEETINGS

A number of specialist interest groups will be holding their meetings at DATE 2015. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage **www.date-conference.com**

Day+Time	Meeting & Contact	Room
MON 1400-1700	**ENI² meeting** Patrick Cogez, STMicroelectronics, FR patrick.cogez@st.com	Bayard
MON 1900-2100	**ACM SIGDA/EDAA PhD Forum** Rolf Drechsler, University of Bremen/DFKI, DE drechsle@informatik.uni-bremen.de	Salle de Reception
TUE 1300-1430	**eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)** Giorgio Di Natale, LIRMM, FR giorgio.dinatale@lirmm.fr	Berlioz
TUE 1830-1930	**EDAA General Assembly** Georges Gielen, Katholieke Universiteit Leuven, BE Georges.Gielen@kuleuven.be	Bayard
TUE 1830-2030	**IFIP Working Group 10.5** Dominique Borrione, IMAG, Fr Dominique.Borrione@imag.fr	Les Bans
THU 0900-1600	**MOS-AK Workshop** Wladek Grabinski, Modeling of Systems and Parameter Extraction Working Group, CH wladek@grabinski.ch	Berlioz

ACM SIGDA/EDAA PHD FORUM

Monday, March 9, 2015, 1900-2100, Room – Salle de Reception
Organiser: **Rolf Drechsler,** University of Bremen/DFKI, DE

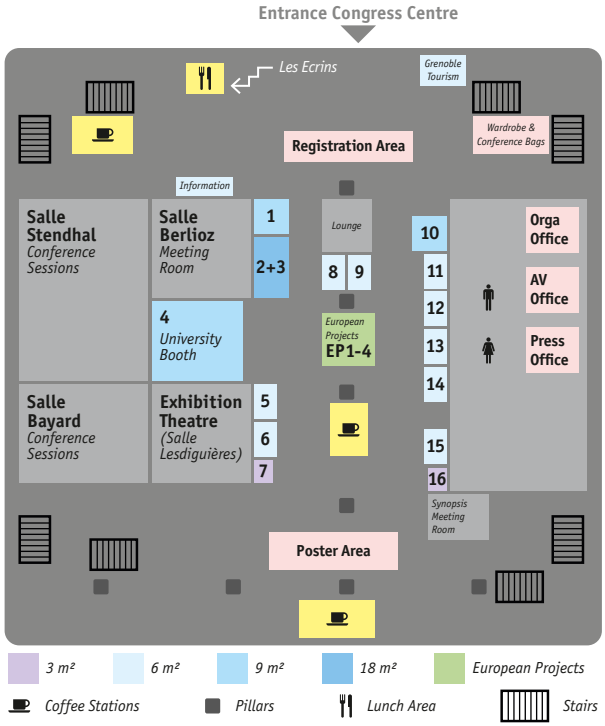
The ACM SIGDA/EDAA PhD Forum at the Design, Automation and Test in Europe (DATE) Conference is a poster session and a buffet dinner organized and sponsored by ACM SIGDA and the European Design and Automation Association (EDAA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.
More information is available on the web **www.date-conference.com**

EXHIBITION GUIDE

On behalf of the whole Organising Committee, we thank you very much for visiting DATE 2015 and are happy to welcoming you in the beautiful city of Grenoble, France!

All commercial sponsors and participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

EXHIBITION FLOOR PLAN



EXHIBITORS & COMMERCIAL SPONSORS

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CEA-Leti	8
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Keysight Technologies	6
MathWorks	
Mentor Graphics	
Methodics	13
MINALOGIC	
MunEDA GmbH	5
PRiME Research Programme – Power-efficient, Reliable, Manycore Embedded systems	EP 1
PRO DESIGN Electronic GmbH	15
Silexica	12
SPRINGER	2+3
STMicroelectronics	9
Synopsys	
TRESCCA	EP 3
University Booth	4

COMPANY PROFILES

Advantest Europe GmbH

★ Booth: 7

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Cloud Testing Service, Inc., a wholly owned Advantest subsidiary, was founded in 2012, with the mission of creating a new paradigm for semiconductor test. Benefitting from decades of experience and our trusted leadership role in the semiconductor test industry, CloudTesting™ Service (CTS) is positioned to offer an alternative to standard test hardware. CTS addresses the challenges facing major chipmakers, R&D engineers, design labs, universities and research institutes to get access to large ATE testers to debug and test their devices.

We leverage the recent advances in cloud computing that have transformed the concept of ownership from physical possession of an asset to a licensing agreement. With the asset itself residing in the cloud, the semiconductor test business model expands customer access to testers by delivering test IP directly to their personal computers. This revolutionary concept of a tester in every lab defines our mission to transform the accessibility of test. Driven by our passion to solve customer issues with innovative products and services, we contribute to the further development of the semiconductor industry.

The main benefits of using CTS include:
- Small and portable personal test solution
- One box for all signals, features and performance
- Multiple IPs to customize testing needs
- Easy testing through GUI interfaces
- No capital investment in tester hardware
- Easy implementation of EDA data and straightforward migration to production

For detailed product information and user registration visit: www.cts-advantest.com/en/.

Test:
- Design for Test
- Design for Manufacture and Yield
- Logic Analysis
- Test Automation (ATPG, BIST)
- Boundary Scan
- Silicon Validation

AUTOMICS

★ Booth: EP 4

Contact: Dr. Ramy Iskander

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Website: www.automics.eu

Smart Power ICs integrating on the same substrate power stages and low power circuits are extensively used today in the field of automotive applications. Performance challenges (such as high integration, integration of functions of different natures, speed, low power consumption, ...) trigger numerous reliability problems especially the ones related to signal integrity inside such smart power ICs. The objective of AUTOMICS is to develop a novel computer-aided design methodology for fast modeling and simulation of destructive substrate coupling effects in integrated mixed-signal, High Voltage (HV) and High Temperature (HT) smart power ICs for automotive applications.

ASIC and SOC Design:
- Physical Analysis (Timing, Themal, Signal)
- Analogue and Mixed-Signal Design
- System-Level Design:
- Physical Analysis

Test:
- Design for Manufacture and Yield
- Mixed-Signal Test

Avnet ASIC Israel Ltd

★ Booth: 16

Contact: Karni Tohar

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Israel

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Website: www.avnet-asic.com

AAI is a leading provider of complete ASIC and COT design and Turnkey Manufacturing Services for companies that develop advanced SoC (system-on-chip) devices. AAI offers a broad spectrum of ASIC services, among them Logic architecture and Design, IP selection and Integration, ASIC implementation (RTL to GDSII), Analog design; Productization and Production services (Silicon, Package, Test) and others. AAI is experienced in both digital and analog mixed-signal technologies and can offer SoC solutions based on the most advanced process nodes from 180nm down to 28nm. AAI is a subsidiary of Avnet Israel, branch of Avnet, Inc. – the world's largest distributor of electronic parts, enterprise computing and storage products and embedded subsystems. AAI has been serving the international SoC market since 1986 and has completed more than 300 successful tape-outs.

Cadence Academic Network

Contact: Patrick Haspel

Cadence Academic Network
Germany

E-Mail: phaspel@cadence.com
Website: www.cadence.com

The Academic Network was launched by Cadence in 2007. The aim was to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence was established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems

CEA-Leti ★ Booth: 8

Contact: Caroline Arnaud

CEA-Leti
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Leti is an institute of CEA, a French research-and-technology organization with activities in energy, IT, healthcare, defense and security. Leti is focused on creating value and innovation through technology transfer to its industrial partners. It specializes in nanotechnologies and their applications, from wireless devices and systems, to biology, healthcare and photonics. In addition to Leti's 1,800 employees, there are more than 250 students involved in research activities, which makes Leti a mainspring of innovation expertise. Leti's portfolio of 1,880 families of patents helps strengthen the competitiveness of its industrial partners. In parallel to these activities, Leti has built strong partnerships with main EDA actors as ATRENTA or DOCEA. Leti proposes also a Silicon Product Enablement Center to enable industrials partners to develop and launch best in class products by providing them with access to advanced technology, design know-how and expert resources.

Circuits Multi-Projects (CMP) ★ Booth: 1

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Website: http://cmp.imag.fr

Circuits Multi-Projects (CMP) is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 1000 Institutions from 70 countries have been served, more than 6700 projects have been prototyped through 800 manufacturing runs, and 60 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and ams down to 28 nm FDSOI, 3D-IC from TEZZARON/GLOBALFOUNDRIES. MEMS are available on various processes: specific MEMS technologies (PolyMUMPS, SOIMUMPS, PiezoMUMPS, MetalMUMPS from MEMSCAP), MIDIS from TELEDYNE DALSA and bulk micromachining from ams. Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ceramic packages.

ASIC and SOC Design:
- MEMS Design
- Services:
- Prototyping
- Foundry & Manufacturing

CLERECO FP7 ★ Booth: EP 2

Contact: Maha Kooli

CNRS - LIRMM
161, rue Ada, 34095 Montpellier
France

Website: www.clereco.eu

Advanced multifunctional computing systems realized in forthcoming technologies hold the promise of a significant increase of the computational capability that will offer end-users ever improving services and functionalities. However, the same path that is leading technologies toward these remarkable achievements is also making electronic devices increasingly unreliable. Reliability of electronic systems is therefore a key challenge for the whole information and communication technology and must be guaranteed without penalizing or slowing down the characteristics of the final products.
CLERECO research project (http://www.clereco.eu), a FP7 Collaboration Project involving Politecnico di Torino (Italy), National and Kapodistrian University of Athens (Greece), LIRMM (France), Intel Corporation Iberia S.A. (Spain), Thales SA (France), Yogitech spa (Italy) and ABB AS (Norway), recognizes early accurate reliability evaluation as one of the most important and challenging tasks toward this goal. Being able to precisely and early evaluate the reliability of a system means being able to carefully plan for specific countermeasures rather than resorting to worst-case approaches. The proposed CLERECO framework for efficient reliability evaluation and therefore efficient exploitation of reliability oriented design approaches starting from early phases of the design process will enable circuit integration to continue at exponential rates and enable the design and manufacture of future systems for the computing continuum at a minimum cost contrary to existing worst-case-design solutions for reliability. The applications of such chips will play a major role in several fields ranging from avionics, automobile, smartphones, mobile systems, and future servers utilized in the settings of several types of HPC systems.

Concept Engineering GmbH ★ Booth: 11

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Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers, SoC and IC/FPGA designers.

Nlview Widgets™ – a family of schematic generation and visualization engines that can be easily integrated into EDA tools.

S-Engine™ - automatic system-level schematic generation capabilities combined with IP editing and SoC assembly features.

T-Engine™ - a visualization engine for transistor-level EDA tools.

StarVision® PRO - a mixed-signal and mixed-language debugger with extensive support for post-layout debugging and customizable netlist pruning.

RTLVision® PRO – a graphical debugger for SystemVerilog, Verilog and VHDL based designs.

SpiceVision® PRO – a customizable debugger for SPICE based designs.

GateVision® PRO – a customizable debugger for Verilog, LEF/DEF and EDIF based designs.

ASIC and SOC Design:
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design

Test:
- Design for Test

Design & Reuse ★ Booth: 14

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Design & Reuse (D&R) was founded in 1997, the same year it launched its unique and renowned IP web portal, www.design-reuse.com. D&R has extended its scope with its new site, www.dr-embedded.com for connecting system designers with vendors of subsystems, platforms, middleware...
D&R continues to maintain its focus on streamlining IP-based design with its Enterprise IP Management System (IPMS) offering, a next generation configurable Enterprise Java based platform offering the most innovative solution for internal and external IP management from design to reuse, to IP tracing in delivery and products etc.
It includes unique powerful procurement features for external IPs (Finance reporting, Fee and royalty calculation). Recently, the platform has been extended to software license management. It incorporates a license monitoring Front End aiming at reducing License cost and offers powerful corporate financial reporting capabilities.

EUROPRACTICE Booth: 10

Contact: Carl Das

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The EUROPRACTICE Service offers CAD tools for education, low cost and easy access to ASIC prototype and small volume fabrication. The service is offered by IMEC (B), STFC (UK) and Fraunhofer IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW runs whereby many designs are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemi, austiamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up

to more than 5000 wafers per year per ASIC.

Test:
- Design for Test
- Design for Manufacture and Yield
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Prototyping

Semiconductor IP:
- Analogue & Mixed Signal IP
- Physical Libraries

EuroTraining – Training in Nanoelectronics

Contact: Annette Locher

FSRM - Swiss Foundation for Research in Microtechnology
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Website: www.eurotraining.net

EuroTraining develops and runs the website www.eurotraining.net offering access to hundreds of courses, summer schools, lecturing material and on-line tutorials in the field of nanoelectronics and micro-nano systems.

The service addresses industry and universities which are also encouraged to share the basic development of courses, text books and training material on the EuroTraining website.

Course providers, universities or European projects can announce their training offer on www.eurotraining.net for free. Upon request, the events can also be included in the monthly newsletter to over 16'000 addresses.

The EuroTraining project is funded by the European Union.

H-INCEPTION

★ Booth: EP 4

Contact: Dr Olivier Guillaume

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New types of emerging applications require microelectronics which closely interact with the surrounding environment in different physical domains (optical, mechanical, acoustical, biological, etc.). The main challenge is to correctly specify, dimension and verify these multi-domain microelectronics assisted systems, to avoid unnecessary errors and redesigns which hamper product quality and thus time to market. Heterogeneous INCEPTION ("H-INCEPTION") aims at developing and deploying a novel unified design methodology and tools to address the system-level design and verification need for these systems. This will be deployed inside the European Industry with an ecosystem, delivering all design technology ingredients, from design and verification methodology to the essential modeling languages and simulation engines.
H-INCEPTION will enable the industrial partners to create multi-domain virtual prototypes by introducing abstract modeling techniques and fast system simulation concepts. A rich consortium from 5 countries composed of semiconductor and fabless companies, equipment suppliers, EDA vendors, research institutes and universities cover different fields and applications domains such as automotive, wireless, avionics and biomedical will all contribute to the creation and validation of this unified design methodology and ecosystem.

ASIC and SOC Design:
- Behavioural Modelling & Simulation
- Analogue and Mixed-Signal Design
- MEMS Design

System-Level Design:
- Behavioural Modelling & Analysis

Keysight Technologies

★ Booth: 6

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Keysight Technologies Inc. (NYSE: KEYS) is the world's leading electronic measurement company, transforming today's measurement experience through innovation in wireless, modular, and software solutions. With its HP and Agilent legacy, Keysight delivers solutions in wireless communications, aerospace and defense and semiconductor markets with world-class platforms, software and consistent measurement science. The company's 9,500 employees serve customers in more than 100 countries.

MathWorks

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MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development.
MATLAB®, the language of technical computing, is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink® is a graphical environment for simulation and Model-Based Design of multidomain dynamic and embedded systems. The company produces nearly 100 additional products for specialized tasks such as data analysis and image processing.
MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields, such as financial services and computational biology. MATLAB and Simulink enable the design and development of a wide range of advanced products, including automotive systems, aerospace flight control and avionics, telecommunications and other electronics equipment, industrial machinery, and medical devices. More than 5000 colleges and universities around the world use MATLAB and Simulink for teaching and research in a broad range of technical disciplines.

ASIC and SOC Design:
- Behavioural Modelling & Simulation
- Verification
- Analogue and Mixed-Signal Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Hardware/Software Co-Design

Test:
- System Test

Services:
- Design Consultancy
- Training

Mentor Graphics

Contact: Jean-Marie Saint-Paul

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Website: www.mentor.com

Mentor Graphics is a technology leader in electronic design automation, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months in excess of $1.15 billion. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com/. We offer the broadest industry portfolio of best-in-class hardware and software design solutions focused on IC design and physical verification, functional verification, FPGA/PLD, design-for-test, PCB design and emerging technologies. Mentor Graphics innovative tools help our customers solve current and future design challenges, including scalable solutions for functional verification, cutting-edge technology for design-for-manufacturability and mixed-level IC design verification, award-winning test compression technology, embedded software development systems, and market-leading integrated system design solutions.

ASIC and SOC Design:
- Design Entry
- Verification
- Analogue and Mixed-Signal Design

System-Level Design:
- Acceleration & Emulation
- PCB & MCM Design

Test:
- Design for Test
- Embedded Software Development:
- Compilers
- Real Time Operating Systems

Methodics

★ Booth: 13

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Methodics delivers state-of-the-art semiconductor data management (DM) for analog, digital, and SoC design teams.
Integration of IP Lifecycle Management with powerful analytics and industry-standard DM enables Methodic's solutions to significantly reduce design cost; making design more efficient, predictable and with higher quality. Advanced IP distribution infrastructure, cataloging, and workspace management ensure that no matter where designers are located they have full visibility into the IP available to them and can easily access that data regardless of its location.
Methodic's clients for analog and digital designers integrate natively with existing design environments making DM seamless to the users. Building our solutions on top of standard Subversion and Perforce infrastructure ensures data is safe, always available, and that the tools can take advantage

of the latest advancements from the software development community.
Our highly scalable and industry proven solutions are ideal for small specialized IP design teams, as well as large multinational, multisite, SoC design teams. For further information, visit www.methodics.com.

ASIC and SOC Design:
– Design Entry
– Analogue and Mixed-Signal Design

Services:
– Data Management and Collaboration
– IP e-commerce & Exchange

MINALOGIC

MINALOGIC
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France

Tel: +33 4 38 78 19 47

Website: www.minalogic.com

Created in 2005, the Minalogic global competitive cluster in Grenoble is a public/private partnership with 240 members dedicated to smart systems integration and digital solutions. Minalogic's collaborative projects are focused on developing products and services that capitalize on the potential of better combinations of micro- and nanoelectronics, optics-photonics and software. The cluster encourages and supports industry research-training collaborations with companies in Europe, Asia and the U.S., while responding to the global high-tech community's need to identify new value-added services that can be integrated into existing products in health care, the environment, mobility, the media, the textile industry and other areas.

MunEDA GmbH ★ Booth: 5

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Website: http://www.muneda.com

MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA´s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA´s solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

PRiME Research Programme – Power-efficient, Reliable, Many-core Embedded systems ★ Booth: EP 1

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E-Mail: info@prime-project.org
Website: www.prime-project.org

PRiME is a five year collaborative research programme aimed at improving the reliability and power efficiency of many-core embedded systems. With funding of £5.6m from the UK's Engineering and Physical Sciences Research Council, PRiME brings together four leading UK universities with expertise in advanced electronics and computer systems. Working in collaboration with five companies, PRiME will tackle the challenge of developing the theory and practice of future high-performance embedded systems utilising many-core processors.

PRiME's objectives are to develop understanding of how to manage power consumption and improve the reliability of embedded many-core systems and to develop theory, methods and tools to address these issues.

PRiME seeks to exploit the vast potential of heterogeneous many-core processors; the objective is to enable processor core scaling with sustainable energy consumption and reliability.

PRiME has four inter-related research themes. Each theme focuses on the theory, algorithms, architecture and engineering challenges which need to be overcome to deliver PRiME's objectives:

1. Cross-layer theories and model
2. Run-time management and optimisation
3. Many-core architectures and re-configuration
4. Platforms, applications and demonstrators

An integrated, cross-system layers (hardware and software) approach is being followed.

ASIC and SOC Design:
– Power & Optimisation

System-Level Design:
– Hardware/Software Co-Design

Embedded Software Development:
– Software/Modelling

Semiconductor IP:
– Embedded Software IP

COMPANY PROFILES

DATE15 March 9 – 13, 2015, Grenoble, France

PRO DESIGN Electronic GmbH ★ Booth: 15

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E-Mail: patrick.lemeledo @prodesign-europe.com
Website: www.prodesign-europe.com

The privately held company was founded in 1982 and has around 80 employees, with various facilities in Germany and France. PRO DESIGN has more than 30 years of experience in the EDA market and as provider in the E²MS market. It has built extensive knowledge in the areas of FPGA Board development, electronic engineering, FPGA design, high performance PCB design, construction, production, assembly and testing.

PRO DESIGN is the vendor of the successful proFPGA product line. The proFPGA product family is a complete, scalable, and modular multi FPGA Prototyping solution, which fulfills highest needs in the area of ASIC and IP Prototyping and pre-silicon software development. The proFPGA product series consists of different kind of motherboards, various Xilinx Virtex 7 and Virtex UltraScale based FPGA Modules, a set of interconnection boards/cables, and a range of daughter boards (e.g. DDR3 memory boards, high speed interface boards (like PCIe, USB 3.0, Gigabit Ethernet, etc.). It addresses customers who need a scalable and most flexible high performance FPGA based Prototyping solution for early software development and IP and ASIC verification. The innovative system concept and technologies offers best in class reusability for several projects, which guarantees the best return on invest. For more information about PRO DESIGN please visit: www.proFPGA.com

ASIC and SOC Design:
– Verification

System-Level Design:
– Acceleration & Emulation
– Hardware/Software Co-Design

Test:
– System Test

Services:
– Prototyping

Hardware:
– FPGA & Reconfigurable Platforms
– Development Boards

Silexica ★ Booth: 12

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E-Mail: sheng@silexica.com
Website: www.silexica.com

Silexica provides programming tools for embedded multicore architectures. The product spectrum addresses software developers and hardware platform architects, as well as semiconductor vendors and fabless multicore IP providers. Silexica´s unique source-to-source compilation approach frees the users from tedious manual software partitioning and distribution on multicores while delivering robust parallel code optimized for performance and power consumption.

System-Level Design:
– Behavioural Modelling & Analysis
– Hardware/Software Co-Design

Services:
– Prototyping
– Training

Embedded Software Development:
– Compilers
– Software/Modelling

Semiconductor IP:
– Embedded Software IP

Application-Specific IP:
– Digital Signal Processing
– Telecommunication
– Wireless Communication

SPRINGER ★ Booth: 2+3

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You can also browse key titles in your field and buy (e)books at discount prices. With Springer you are in good company.

STMicroelectronics

★ Booth: 9

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STMicroelectronics is one of the world's largest semiconductor companies. Offering one of the industry's broadest product portfolios, ST serves customers across the spectrum of electronics applications with innovative semiconductor solutions by leveraging its vast array of technologies, design expertise and combination of intellectual property portfolio, strategic partnerships and manufacturing strength. ST focuses its product strategy on sense and power technologies, automotive products, and embedded-processing solutions. The Sense and Power segment encompasses MEMS and sensors, power discrete, and advanced analog products. The Automotive portfolio covers all key application areas from powertrain and safety to car body and infotainment. The Embedded Processing Solutions include microcontrollers, digital consumer and imaging products, and digital ASICs.
ST products are found everywhere microelectronics make a positive and innovative contribution to people's lives. From energy management and savings to trust and data security, from healthcare and wellness to smart consumer devices, in the home, car and office, at work and at play. By getting more from technology to get more from life, ST stands for life.augmented. Since its creation, ST has maintained an unwavering commitment to R&D. Almost one fifth of its employees work in R&D and product design. Among the industry's most innovative companies, ST owns almost 15,000 patents and pending applications corresponding to over 9,000 patent families. The Company draws on a rich pool of chip fabrication technologies, including advanced FD-SOI (Fully Depleted Silicon-on-Insulator) CMOS (Complementary Metal Oxide Semiconductor), mixed-signal, analog and power processes. From its inception, ST has established a strong culture of partnership and through the years has created a worldwide network of strategic alliances with key customers, suppliers, competitors, and leading universities and research institutes around the world.

Synopsys

Website: www.synopsys.com

Synopsys, Inc. provides products and services that accelerate innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor intellectual property (IP), Synopsys' comprehensive, integrated portfolio of system level, IP, implementation, verification, manufacturing, optical and field-programmable gate array (FPGA)solutions help address the key challenges designers face such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in quickly bringing the best products to market while reducing costs and schedule risk. For more than 25 years, Synopsys has been at the heart of accelerating electronics innovation with engineers around the world having used Synopsys technology to successfully design and create billions of chips and systems. The company is headquartered in Mountain View, California, and has approximately 90 offices located throughout North America, Europe, Japan, Asia and India.

University Booth

★ Booth: 4

Contact: Andreas Vörg and Laurent Fesquet

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CIME Nanotech
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E-Mail: university-booth@date-conference.com
Website: www.date-conference.com/group/exhibition/u-booth

The University Booth fosters the transfer of academic work to industry. The University Booth is part of the DATE 2015 exhibition and is free of charge for presenters and their visitors. The University Booth is sponsored by the DATE Sponsor's Committee. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are presenting innovative hardware and software demonstrations. All demonstrations will take place during the exhibition within a dedicated time slot.

The detailed University Booth Programme is available in your conference bag and online at www.date-conference.com/exhibition/ub-programme

The University Booth is organized by University Booth Co-Chairs Laurent Fesquet, TIMA and CIME Nanotech, FR
university-booth@date-conference.com

Andreas Vörg, edacentrum GmbH, DE
university-booth@date-conference.com.

ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Synthesis
- Power & Optimisation
- Physical Analysis (Timing, Themal, Signal)
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Physical Analysis
- Acceleration & Emulation
- Hardware/Software Co-Design
- Package Design
- PCB & MCM Design

Test:
- Design for Test
- Design for Manufacture and Yield
- Logic Analysis
- Test Automation (ATPG, BIST)
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Design Consultancy
- Prototyping
- Data Management and Collaboration
- IP e-commerce & Exchange
- Foundry & Manufacturing
- Training
- Embedded Software Development:
- Compilers
- Real Time Operating Systems
- Debuggers
- Software/Modelling

Hardware:
- FPGA & Reconfigurable Platforms
- Development Boards
- Workstations & IT Infrastructure
- Semiconductor IP:
- Analogue & Mixed Signal IP
- Configurable Logic IP
- CPUs & Controllers
- Embedded FPGA
- Embedded Software IP
- Encryption IP
- Memory IP
- On-Chip Bus Interconnect
- On-Chip Debug
- Physical Libraries
- Processor Platforms
- Synthesizable Libraries
- Test IP
- Verification IO

Application-Specific IP:
- Analogue & Mixed Signal IP
- Data Communication
- Digital Signal Processing
- Multimedia Graphics
- Networking
- Security
- Telecommunication
- Wireless Communication

DATE EXECUTIVE COMMITTEE

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DETAILED INDEX

NOTES

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NOTES

Scope of the Event

The 19th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical, Healthcare and Assistive Technology Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles; Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by Sunday September 13, 2015 via:
www.date-conference.com

Papers can be submitted either for standard oral presentation or for interactive presentation.
The Programme Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.

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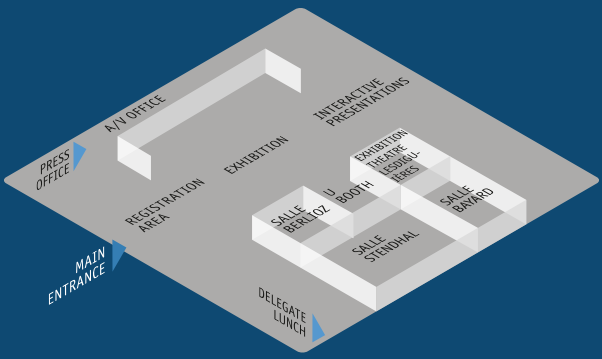
VENUE PLAN



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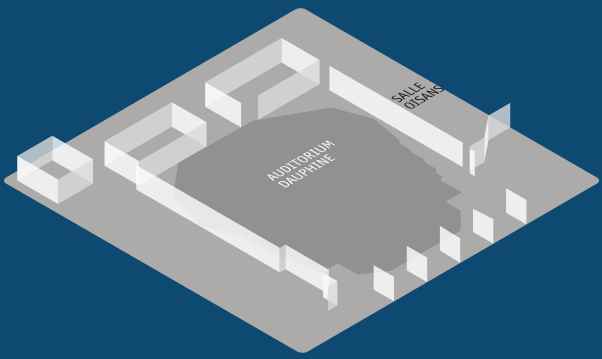
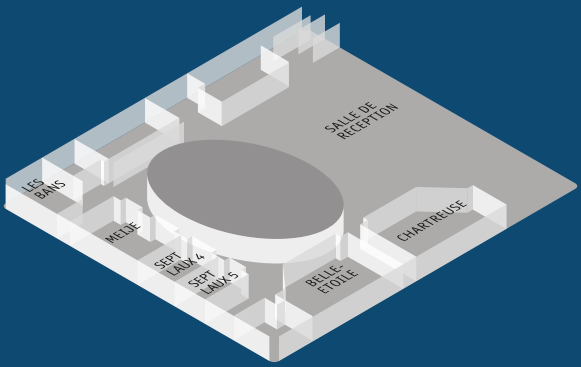


FIRST FLOOR



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