Leveraging dynamic reconfiguration to increase fault-tolerance in FPGA-based satellite systems

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Performance requirements for on-board processing of satellite instrument data are steadily increasing. This demonstrator shows how today's SoCs for satellite payload processing can be extended with high-speed interfaces and computing power utilizing commercial dynamically reconfigurable FPGAs. Reconfigurable hardware further allows for changing or adapting payload processing during the flight mission, even if not foreseen at design time. Moreover, dynamic partial reconfiguration allows for implementing time-sharing of the reconfigurable resources between different applications, thus increasing the area and energy efficiency. The use of commercial SRAM-based FPGAs will experience single event effects (SEE) due to radiation in configuration memory, logic resources and block rams. Therefore, a unit for detection (readback scrubbing), and correction on the processing FPGAs has been developed to increase the reliability of the system.

To prove the effectiveness of the system a scalable prototyping environment has been developed [1] combining dynamically reconfigurable Xilinx FPGAs, a rad-hard SoC (SpaceWire Remote Terminal Controller, based on a LEON2-FT), and emerging avionic interfaces (e.g., SpaceFibre) additionally to established ones (e.g., SpaceWire, MIL or CAN).

The modular RAPTOR FPGA prototyping platform has been used to create a highly scalable platform, where the amount of reconfigurable resources (e.g., number of FPGAs or FPGA type) can be easily modified. The RAPTOR-based demonstrator is depicted in Fig.1. Further details on the architecture of the system are presented in [2].
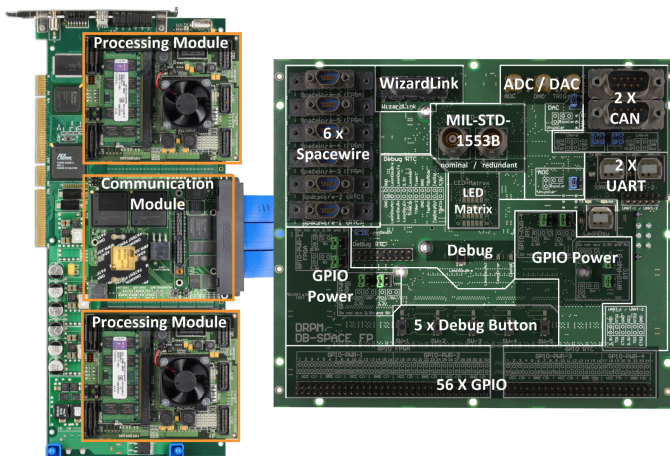

Fig. 1. Modular RAPTOR-based demonstrator for satellite payload processing

The key component on each data processing FPGA is a dedicated unit, called self-hosting reconfiguration controller (SHRC), which offers the maximum possible scrubbing and reconfiguration bandwidth of 400 MByte/s. The SHRC includes a small, self-contained readback scrubbing unit (RSU) which continuously monitors the internal configuration of the SRAM-based FPGA. Thereby, the RSU can adapt the scrub rate for different parts of the FPGA individually, giving the user the ability to scrub some parts of the design, e.g., sensitive parts, more often. The RSU is triplicated using triple modular redundancy to mitigate faults caused by SEE.
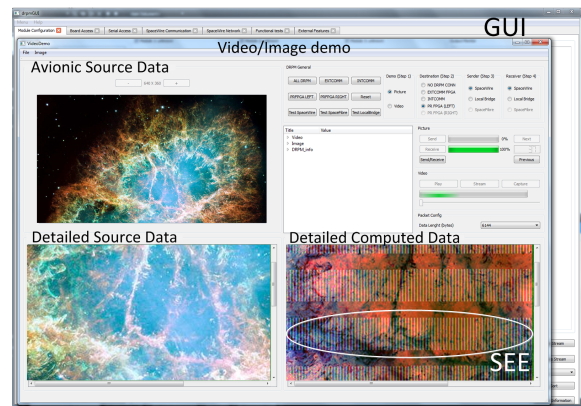

Fig. 2. GUI of the demonstrator (showing a bit flip during image processing)

The overall system is started, monitored, and controlled by a rad-hard LEON2-FT CPU at run-time. In case of detected persistent errors, the CPU triggers a full reconfiguration of the affected FPGA. A GUI (Fig.2) allows to modify the system setup and visualize the data (e.g., partial or full bitstreams, images or videos) from/to the avionic source/sink interfaces.

To evaluate the fault tolerance of the system, a fault is injected into the configuration of the FPGA by the SHRC using partial reconfiguration. The artefacts in the bottom right picture (Fig.2) shows the effect of a SEE during image processing. A detected SEE is corrected by the RSU in 1.92 μs.

References

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