A Visualization and Design Environment for Topological Quantum Circuits

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Quantum circuits use quantum-mechanical properties of certain physical systems, such as superposition and entanglement, to perform massively parallel calculations. They provide polynomial algorithms for problems for which only inefficient algorithms with asymptotically-exponential running time are known in conventional models of computation. Building a scalable quantum computer that can process a large number of quantum bits (qubits) is one of the grand challenges of modern science. While first small quantum computers have been experimentally demonstrated and a number of implementation technologies have been suggested, all of them encounter difficulties when it comes to scaling. The central difficulty is the high susceptibility of such circuits to noise and decoherence, which necessitates the use of special quantum error correction.

Topological quantum computing (TQC) [1] [2] is a paradigm that offers a path to scalability. It strikes a balance between systematic, intuitive methods to design large computations, and relatively loose requirements on the vulnerability of individual qubits to errors. The availability of a platform for implementing large quantum algorithm constitutes the need for methods to manage design complexity, including automatic synthesis, optimization, compaction, verification and visualization of TQC circuits. Topological quantum circuits are based on a three-dimensional cluster of qubits which supports highly efficient topological quantum error-correcting codes. In this way, the circuits can operate even though its individual qubits are subject to relatively high error rates.

We will present the first environment for design of TQC circuits. The environment allows the user to graphically enter the structure of a circuit, add, delete and re-shape individual qubits, and perform optimization and compaction (both manually and by global replacement). The circuits are represented on an intermediate technology-independent level, where “logical qubits” that consist of a large number of physical qubits perform error-corrected operations. For example, the circuit in Fig. 1 shows an error-corrected CNOT gate implemented by four logical qubits represented by colored structures. The optimized representation can be translated into instruction sequences for a classical computer that operates the actual quantum hardware.

[1] S. Devitt et al, Architectural design for a topological cluster state quantum computer, *New J. Phys.* 11, 2009.
[2] A. Paler et al., Synthesis of topological quantum circuits, *IEEE/ACM NANOARCH Symp.*, 2012.

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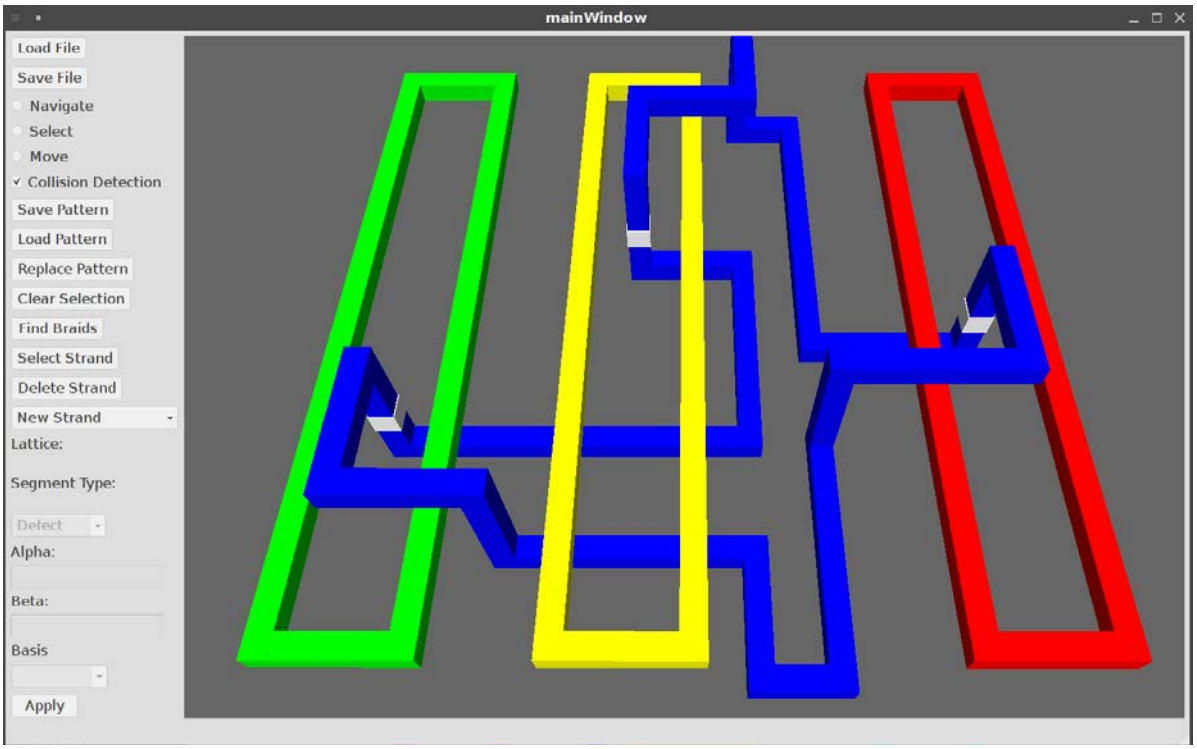

Figure 1: Main working window of the design environment.