advance programme

DATE 14

Design, Automation & Test in Europe

Dresden, Germany
March 24 – 28, 2014

www.date-conference.com

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PROGRAMME GUIDE programme guide

Dear Colleague,

We proudly present to you the Advance Programme of DATE 14. DATE combines an electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

DATE 14 received 1090 paper submissions; an all-time high for DATE and an 8% increase over DATE 13. 890 of those submissions were eligible for review. Besides the large share (46%) of submissions coming from Europe, 23% of submissions are from North- America, 27% from Asia, and 4% from the rest of the world. This clearly demonstrates DATE's global reach and impact. The most attractive topics this year were: "Architectural and Microarchitectural Design" in the Design Methods and Tools Track, "Secure Systems" in the Application Design Track, "On-Line Test, Fault Tolerance and Reliable System Design" in the Test and Reliability Track and "Real-time, Networked, and Dependable Systems" in the Embedded Systems Software Track.

For the 17th successive year DATE has prepared an exciting technical program, with the help of more than 300 members of the Technical Program Committee who dedicated their time to perform 3620 reviews (more than four per submission).

The plenary keynote speakers on Tuesday are David Fuller, Vice President of Application and Embedded Software for National Instruments, to talk about "System Design Challenges for Next Generation Wireless and Embedded Systems" and Gerd Teepe, Director Design Engineering at GLOBALFOUNDRIES in Dresden, to talk about "The Growing Importance of Microelectronics from a Foundry Perspective". On the same day, the Executive Track offers a series of business panels discussing hot topics. Executive speakers from Synopsys, Cadence, IBM, IMEC, TSMC Europe, Mentor Graphics and many other companies leading the design and automation industry will address some of the complexity issues in electronics design and discuss about the advanced technology challenges and opportunities. To emphasize that DATE is the major event for designers, DATE 14 features invited sessions where Europe's famous consumer industry presents its best designs and design practices.

Gerhard Fettweis

Luca Fanucci

The main conference program from Tuesday to Thursday includes 77 technical sessions organized in parallel tracks from four areas:

D – Design Methods, Tools, Algorithms and Languages

A – Application Design

T – Test and Reliability

E – Embedded Software

Extra tracks are dedicated to the Executive Day on Tuesday and the two special days: "System Level Design" Day on Wednesday and "Advancing Electronics Beyond CMOS" Day on Thursday. There is a lunch-time keynote on Wednesday by Michael Bolle (Robert Bosch GmbH, DE), who will talk on "The connected car and its implication to the automotive chip roadmap". A second lunch-time keynote on Thursday by Karl Leo (Technische Universität Dresden, DE) will be on "Organic Electronics – From Lab to Markets". Additionally, there are 107 Interactive Presentations which are organized into five IP sessions.

Finally, DATE offers a comprehensive overview of commercial design and verification tools in its exhibition including vendor seminars and abundant networking possibilities with fringe meetings.

We wish you a productive and exciting DATE 14 and a memorable social party on Wednesday evening.

DATE 14 General Chair
Gerhard Fettweis, TU Dresden, DE

DATE 14 Programme Chair
Luca Fanucci, University of Pisa, IT

plenary session

Tuesday, March 25, 2014, 0830 – 1030

Opening Plenary, DATE Awards Ceremony and Keynote Addresses

first keynote address

Tuesday, March 25, 2014, 0910, Grosser Saal

1.1.1 System design challenges for next generation wireless and embedded Systems

David Fuller, National Instruments, US

Application demands in our embedded world are growing dramatically. Consumer expectations and the industry's forward-looking technology roadmaps paint a picture of a connected world full of intelligent devices once thought to have fixed functionalities. Researchers exploring next generation wireless systems, Internet of Things (IOT), and even machine-to-machine (M2M) communications face many challenges in making this vision a reality. Where once a single, isolated design flow addressed the discrete application, heterogeneous multi-processing architectures must be considered and embraced along with the connections to other devices and systems, and real-world sensor data. As the systems grow in complexity, new design approaches must also be developed and employed to expedite the research, design, and development cycle. David Fuller will outline challenges system designers face in developing cyber-physical systems and explore a graphical system design approach that includes hardware abstraction and comprehends a heterogeneous multiprocessing environment while embracing different models of computation. Through this new approach, system designers can shorten design cycles and the time to prototype ultimately accelerating deployment.

plenary session

Tuesday, March 25, 2014, 0830 – 1030

Opening Plenary, DATE Awards Ceremony and Keynote Addresses

second keynote address

Tuesday, March 25, 2014, 0950, Grosser Saal

1.1.2 The growing importance of microelectronics from a foundry perspective

Gerd Teepe, GLOBALFOUNDRIES, DE

Microelectronics is the dominant industrial technology of today. Its rate of innovation, spelled out by Moore's Law, is exceptional by any commercial metric, especially, as it has been on this trajectory for almost 40 years. It is not surprising, that other industrial sectors are taking advantage of the innovation engine of the semiconductors for its own product innovation: Cars are safer and more economic, medical diagnostics are performing to a significantly higher level, and energy efficiency from the generation to the consumer is a lot more efficient. "The Internet" has become the basis for our communication, organization and planning in our economies with significant impact to our society. However, the Semiconductor industry is under a powerful transformation marked by the following trends: - Design Complexity is facing new challenges, as technological complexity is transferred to the design space at an accelerated pace - The SOC is dominating the design space - Intelligent Things are emerging with unprecedented cognitive and motion capabilities - The supply chain transformation is in full motion, with the foundry model at the forefront With these powerful trends in motion, we will have to rethink our approach towards semiconductors as part of the industrial system. It will not be sufficient any more to "enhance" traditional products like Cars, TVs, machines or phones with semiconductor content to make them perform at a higher level to increase its value to consumers. We need to rethink the connected world around us to truly assess the next generation of intelligent applications, which we are about to enter.

wednesday keynote address

Wednesday, March 26, 2014, 1330 – 1400, Saal 1

7.0

The connected car and its implication to the automotive chip roadmap

Michael Bolle,
Robert Bosch GmbH, DE

The automotive industry is in a radical change process driven by technology. On the one hand side the proliferation of communication technologies into the car leads to internet connected vehicles. The vehicle will become an integral part of the internet – opening new processing paradigms for the car itself. On the other hand the vehicle itself significantly expands its sensor and processing capabilities by the use of radar, video, ultrasound sensors and usage of state of the art CPU and GPU processor architectures. In our talk we will address both developments and outline foreseen future applications as future driving assistant and infotainment systems as well as highly automated driving. We will discuss major requirements for the future electrical architectures and implications for future automotive chips.

thursday keynote address

Thursday, March 27, 2014, 1330 – 1400, Saal 1

11.0

Organic electronics – from lab to markets

Karl Leo,
Technische Universität Dresden, DE

Organic semiconductors with conjugated electron system are currently intensively investigated for optoelectronic applications. This interest is spurred by novel devices such as organic light-emitting diodes (OLED), organic solar cells, and flexible electronics. I this talk, I will discuss some of the recent progress in realizing devices, in particular highly efficient white OLED for lighting and flexible organic solar cells.

general information

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 14.
Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website **www.date-conference.com**

Dates and Venue

The conference will take place from 24 to 28 March, 2014 in the MARITIM Hotel & International Congress Center Dresden (ICCD), Ostra-Ufer 2, Dresden, Germany – www.dresden-congresscenter.de.
The accompanying exhibition is scheduled from 25 to 27 March, 2014 on the Terrace Level of the ICCD.

Interactive Programme Online

A fully interactive DATE 14 programme is available on the web **www.date-conference.com** where you will be able to view the entire details of the programme and plan your attendance in advance.

Internet Access

The conference organisers will again provide free wireless internet access on-site throughout the whole congress center. Every registered delegate will receive an own WLAN login code at the registration desk (Terrace Level).

Proceedings

The conference proceedings are available for download on-site through the DATE-WLAN for every registered conference delegate. Link: www.date-conference.com/proceedings

Coffee & Lunch Breaks

During the conference days (Tuesday to Thursday), the exhibition area on the Terrace Level of the International Congress Centre also hosts the coffee and lunch break area. During the below-mentioned times, coffee and tea will be served during the coffee breaks as well as light snacks during the lunch break (for fully registered conference delegates only). Furthermore, there is a cash bar on the Terrace Level for visitors and exhibitors.

Tuesday, March 25, 2014	Coffee Break	1030 – 1130
	Lunch Break	1300 – 1430
	Coffee Break	1600 – 1700
Wednesday, March 26, 2014	Coffee Break	1000 – 1100
	Lunch Break	1230 – 1400
	Coffee Break	1600 – 1700
Thursday, March 27, 2014	Coffee Break	1000 – 1100
	Lunch Break	1230 – 1400
	Coffee Break	1530 – 1600

Welcome Reception Monday, March 24, 2014

The organisers kindly invited all registered conference delegates to the DATE 14 Welcome Reception which will take place on Monday, March 24, 2014, from 1800 – 1900 in "Saal 1" of the congress centre. Subsequently, the PhD Forum will take place from 1900 – 2100 in the same room, where every interested delegate can attend as well.

Exhibition Reception Tuesday, March 25, 2014

The Exhibition Reception will take place on Tuesday, March 25, 2014, from 1830 – 1930 in the exhibition area (Terrace Level), where free drinks and snacks for all conference delegates and exhibition visitors will be offered.

DATE Party Wednesday, March 26, 2014

The DATE Party is again scheduled on the second conference day, Wednesday, March 26, 2014, starting from 1930. This year, it will take place in one of Dresden's most exciting and modern buildings, the "Gläserne Manufaktur" of the car manufacturer Volkswagen AG (www.glaesernemanufaktur.de/en/). The party will feature a flying buffet style dinner with various catering points and accompanying drinks. Light background music and the possibility of guided visits through the extraordinary premises will round off the evening. It provides a perfect opportunity to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities.
Please kindly note that it is no seated dinner.
All delegates, exhibitors and their guests are encouraged to attend the party. Please be aware that entrance is only possible with a party ticket. Each full conference registration includes a ticket for the DATE Party. Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets).
Ticket price for the full Evening Social Programme: 75 € per person.
DATE Party Shuttle: There will be an organised shuttle by tram to the DATE Party venue and back for all conference delegates having a Party Ticket.
Meeting point: 1845 in front of the main entrance of the International Congress Center Dresden (ICCD). The trams then start at 1900 from the tram station "Kongresszentrum".

The DATE Party is co-sponsored by the City of Dresden.

Interactive Presentations

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.
To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held on the Conference Level of the congress centre in 30-minute time slots on the following days:

IP Session 1, Tuesday, March 25, 2014	Conference Level, Foyer	1600 – 1630
IP Session 2, Wednesday, March 26, 2014	Conference Level, Foyer	1000 – 1030
IP Session 3, Wednesday, March 26, 2014	Conference Level, Foyer	1600 – 1630
IP Session 4, Thursday, March 27, 2014	Conference Level, Foyer	1000 – 1030
IP Session 5, Thursday, March 27, 2014	Conference Level, Foyer	1530 – 1600

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

Organiser: **Yervant Zorian,** Synopsys, US

DATE 2014 will again feature an Executive Track of presentations by leading company executives representing a range of semiconductor manufacturers, EDA vendors, fables houses and IP providers. This one-day program will be held on Tuesday 25 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks.

All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view.

2.1

EXECUTIVE SESSION:

How to Handle Today's Design Complexity

— see page 33

3.1

EXECUTIVE SESSION:

Advanced Technology Challenges & Opportunities

— see page 38

4.1

EXECUTIVE SESSION:

Addressing Challenges of Reliable Chips

— see page 46

special day – wednesday

Organisers and Co-Chairs: **Jürgen Teich,** University of Erlangen-Nuremberg, DE
Johannes Stahl, Synopsys, US

System-Level Design

The special day **System-Level Design** will reflect current industrial practices as well as present recent advances in this research area. A particular emphasis will be on ultra-low power design and modeling at multiple abstraction levels, virtual platforms for software development and architecture design of MPSoCs. We will also take a look at high-level synthesis from different input languages as well as software code generation techniques. Important topics also include multicore enablement for safety-critical and real-time embedded systems as well as accelerator-rich design for the fight against dark silicon.

5.1 SPECIAL DAY Hot Topic: Predictable Multi-Core Computing – see page 51

6.1 SPECIAL DAY Hot Topic: The fight against Dark Silicon – see page 58

7.0 Special Day Keynote – see page 63

7.1 SPECIAL DAY Panel: HW/SW Co-Development - The Industrial Workflow – see page 64

8.1 SPECIAL DAY System Simulation and Virtual Prototyping – see page 70

special day – thursday

Organisers and Co-Chairs: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Thomas Mikolajick, Namlab (cfAED), DE

Advancing Electronics beyond CMOS

As the issues associated with CMOS scaling become harder and more costly to solve, the special day **Advancing Electronics beyond CMOS** will cover the latest trends towards alternative devices and paradigms for computing and data acquisition, storage and transport. Important topics include nanoscale switching devices and computing nanofabrics, trends in memory technologies in hybrid 3D integration, flexible and organic electronics, new state variable vectors (spintronics, photonics) and interfaces to the natural world (sensor networks, data analysis, displays, MEMS).

9.1 SPECIAL DAY Hot Topic: CMOS scaling - from evolutionary to revolutionary computing – see page 76

10.1 SPECIAL DAY Hot Topic: Memories today and tomorrow – see page 83

11.0 Special Day Keynote – see page 89

11.1 SPECIAL DAY Embedded Tutorial: Alternatives to CMOS – see page 89

12.1 SPECIAL DAY Hot Topic: The future of interfacing to the natural world – see page 97

Special Session Chairs: **Omar Hammami,** ENSTA ParisTech, FR
Wolfgang Mueller, University of Paderborn, DE

The following 16 Special Sessions have been organized, which should prove to be of great general interest. Panel Sessions provide forums in which motivated opinions on unsettled issues are discussed. The 'trend setters' are given a time-slot to present their views, which are then subjected to critical appraisal and rich exchanges from the audience. Hot Topic Sessions give technical information about strongly emerging topics and offer a good overview and technical insight provided by leading experts in the field. Relevant issues and their importance for research and development are exposed as food for thought. Embedded Tutorials give an insight of relevant topics usually starting from an introductory basis.

2.2 **Panel: Emerging vs. Established Technologies: a Two Sphinxes' Riddle at the Crossroads?**
Organiser: Marco Casale-Rossi, Synopsys, IT

2.8 **Hot Topic: Technology Transfer towards Horizon 2020**
Organiser: Rainer Leupers, RWTH Aachen, DE

3.2 **Panel: The World Is Going… Analog & Mixed-Signal! What about EDA?**
Organiser: Marco Casale-Rossi, Synopsys, IT

3.8 **Hot Topic: Mission Profile Aware Design – The Solution for Successful Design of Tomorrow Automotive Electronics**
Organisers: Goeran Jerke, Robert Bosch GmbH, DE
Oliver Bringmann, University of Tuebingen, DE

4.2 **Hot Topic: Multicore Systems in Safety Critical Electronic Control Units for Automotive and Avionics**
Organisers: Jürgen Becker, KIT, DE
Oliver Sander, KIT, DE

5.2 **Hot Topic: Hacking and Protecting Hardware: Threats and Challenges**
Organisers: Said Hamdioui, TU Delft, NL
Giorgio Di Natale, LIRMM, FR

5.8 **Embedded Tutorial: System Integration - The Bridge between More than Moore and More Moore**
Organisers: Manfred Dietrich, Fraunhofer IIS/EAS Dresden, DE
Kai Hahn, University Siegen, DE

6.2 **Embedded Tutorial: Emerging Transistor Technologies: From Devices to Architectures**
Organisers: Michael Niemier, University of Notre Dame, US
X. Sharon Hu, University of Notre Dame, US

7.2 **Embedded Tutorial: Cross Layer Resiliency in Real World**
Organiser: Vikas Chandra, ARM, US

8.2 **Hot Topic: Near Threshold Computing (NTC)**
Organiser: Michael Huebner, Ruhr-University Bochum, DE

8.8 **Hot Topic: Beyond CMOS Ultra-low-power Computing**
Organiser: Saibal Mukhopadhyay, Georgia Institute of Technology, US

9.5 **Hot Topic: Connecting Different Worlds – Technology Abstraction for Reliability-Aware Design and Test**
Organisers: Ulf Schlichtmann, Technische Universität München, DE
Andreas Herkersdorf, Technische Universität München, DE

9.8 **Embedded Tutorial: Memcomputing: the Cape of Good Hope**
Organisers: Yiyu Shi, Missouri University of Science & Technology, US
Hung-Ming Chen, National Chiao Tung University, TW

11.8 **Embedded Tutorial: GPGPUs: how to combine high computational power with high reliability**
Organiser: Matteo Sonza Reorda, Politecnico di Torino, IT

12.2 **Hot Topic: How Secure are PUFs Really? On the Reach and Limits of Recent PUF Attacks**
Organiser: Ulrich Rührmair, TU München, DE

12.8 **Panel: Future SoC verification methodology: UVM evolution or revolution?**
Organiser: Alex Goryachev, IBM Research - Haifa, IL

EVENT OVERVIEW event overview

MONDAY
Educational Tutorials
ACM SIGDA/EDAA PhD Forum
Fringe Meetings
Welcome Reception

TUESDAY
Opening Plenary, DATE Awards Ceremony and Keynote Addresses
Technical Conference
Vendor Exhibition & Exhibition Theatre
Executive Sessions
University Booth
Fringe Meetings
Exhibition Reception

WEDNESDAY
Technical Conference
Vendor Exhibition & Exhibition Theatre
Special Day on "System-Level Design" and Keynote
University Booth
DATE Party

THURSDAY
Technical Conference
Vendor Exhibition & Exhibition Theatre
Special Day on "Advancing Electronics beyond CMOS" and Keynote
University Booth
Fringe Meetings

FRIDAY
Special Interest Workshops

CONTACTS

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MONDAY monday 24 march

0730	**TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS**					
Breaks	**1100 – 1130 MORNING COFFEE BREAK, 1600 – 1630 AFTERNOON COFFEE BREAK**					
	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 6	Konferenz 5
0930 – 1300	M01 Development of mixed-criticality systems based on system partitioning	M02 Software Debug on ARM Processors in Emulation	M03 Automatic fixed-point conversion: a gate way to high-level power optimization	M04 Dynamic Heterogeneous Architectures to Address The Efficiency Crisis!	M05 Wireless NoC as Interconnection Backbone for Multicore Chips: Promises, Challenges, and Recent Developments	M06 Testing of TSV-Based 2.5D- and 3D-Stacked ICs
1300 – 1430	**LUNCH BREAK**					
1330	**CONFERENCE REGISTRATION BEGINS**					
	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 6	Konferenz 5
1430 – 1800	M07 L4/Fiasco.OC - A Microkernel OS Designed for Security, Real-Time and Reliability	M08 Microfluidic Biochips: A Vision for More than Moore and Biochemistry-on-Chip	M09 Energy-Efficient System Design Through Error-Resilient Computing	M10 A Cyber-Physical Approach to Modeling, Simulation and Verification of Smart Systems	M11 Post-Silicon Validation and Debug: Best Practices and Disruptive Innovation	M12 All You Need to Know About Hardware Trojans and Counterfeit ICs
1800 – 1900	**WELCOME RECEPTION, Saal 1**					

tuesday 25 march

TUESDAY

tuesday 25 march

0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2			
0830–1030	1.1 OPENING PLENARY, DATE AWARDS CEREMONY AND KEYNOTE ADDRESSES, Grosser Saal			
1030–1130	EXHIBITION AND COFFEE BREAK			
	EXECUTIVE SESSIONS	**SPECIAL SESSIONS**	**A-TRACK**	**D-TRACK**
1130–1300	Saal 1 2.1 EXECUTIVE SESSION: How to Handle Today's Design Complexity	Konferenz 6 2.2 Panel: Emerging vs. Established Technologies: a Two Sphinxes' Riddle at the Crossroads?	Konferenz 1 2.3 Making automotive systems safer and more energy efficient	Konferenz 2 2.4 Modern Challenges in Analog and Mixed-Signal Design
1300–1430	LUNCH BREAK			
1430–1600	Saal 1 3.1 EXECUTIVE SESSION: Advanced Technology Challenges & Opportunities	Konferenz 6 3.2 Panel: The World Is Going... Analog & Mixed-Signal! What about EDA?	Konferenz 1 3.3 Secure Hardware Primitives and Implementations	Konferenz 2 3.4 Modeling and Optimization of Power Distribution Networks
1600–1700	COFFEE BREAK *co-sponsored by ELSEVIER*			
1600–1630	IP1 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer			
1700–1830	Saal 1 4.1 EXECUTIVE SESSION: Addressing Challenges of Reliable Chips	Konferenz 6 4.2 Hot Topic: Multicore Systems in Safety Critical Electronic Control Units for Automotive and Avionics	Konferenz 1 4.3 Secure Device Identification	Konferenz 2 4.4 "Almost there" emerging technologies
1830–1930	EXHIBITION RECEPTION			

Plenary Session
Executive Session
Special Session
IP Session
Exhibition Theatre Session

0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2			
0830–1030	1.1 OPENING PLENARY, DATE AWARDS CEREMONY AND KEYNOTE ADDRESSES, Grosser Saal			
1030–1130	EXHIBITION AND COFFEE BREAK			
	D-TRACK	**E-TRACK**	**T-TRACK**	**EXHIBITION THEATRE**
1130–1300	Konferenz 3 2.5 Low-Power and Efficient Architectures	Konferenz 4 2.6 Real-Time memory hierarchies	Konferenz 5 2.7 Yield and Reliability for Robust Systems	Exhibition Theatre 2.8 Hot Topic: Technology Transfer towards Horizon 2020
1300–1430	LUNCH BREAK			
1430–1600	Konferenz 3 3.5 Robust Architectures	Konferenz 4 3.6 Cyber Physical Systems: Security and Co-design	Konferenz 5 3.7 On line Strategies for Reliability	Exhibition Theatre 3.8 Hot Topic: Mission Profile Aware Design – The Solution for Successful Design of Tomorrows Automotive Electronics
1600–1700	COFFEE BREAK *co-sponsored by ELSEVIER*			
1600–1630	IP1 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer			
1700–1830	Konferenz 3 4.5 Memory System Architectures	Konferenz 4 4.6 Code Generation and Optimization for Embedded Platforms	Konferenz 5 4.7 Dependable System Design	Exhibition Theatre 4.8 State-of-the-art in Verification: European Tertulia IC Design - Enabling AMS Structured Verification / Verification in FPGA & IP design flows
1830–1930	EXHIBITION RECEPTION			

D-Track
A-Track
T-Track
E-Track

wednesday 26 march

	SPECIAL DAY	SPECIAL SESSIONS	A-TRACK	D-TRACK
0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
0830 – 1000	5.1 SPECIAL DAY Hot Topic: Predictable Multi-Core Computing	5.2 Hot Topic: Hacking and Protecting Hardware: Threats and Challenges	5.3 Reliable Systems in the Age of Variability	5.4 Prediction and optimization of timing variations
1000 – 1100	EXHIBITION AND COFFEE BREAK			
1000 – 1030	IP2 INTERACTIVE PRESENTATIONS, Conference Level, Foyer			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
1100 – 1230	6.1 SPECIAL DAY Hot Topic: The fight against Dark Silicon	6.2 Embedded Tutorial: Emerging Transistor Technologies: From Devices to Architectures	6.3 Management of Micro/Macro Renewable Energy Storage Systems	6.4 Power delivery and distribution
1230 – 1400	LUNCH BREAK			
1330 – 1400	7.0 SPECIAL DAY KEYNOTE, Saal 1			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
1430 – 1600	7.1 SPECIAL DAY Panel: HW/SW Co-Development - The Industrial Workflow	7.2 Embedded Tutorial: Cross Layer Resiliency in Real World	7.3 Low power methods and multicore architectures for mobile health applications	7.4 Runtime memory optimization and GPU/manycore architectures
1600 – 1700	COFFEE BREAK			
1600 – 1630	IP3 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
1700 – 1830	8.1 SPECIAL DAY: System Simulation and Virtual Prototyping	8.2 Hot Topic: Near Threshold Computing (NTC)	8.3 Physical Attacks and counter-measures	8.4 Efficient Designs for Telecom and Financial Applications
1930 – 2300	DATE PARTY *co-sponsored by the City of Dresden*			

Special Day 1 | Special Session | IP Session | Exhibition Theatre Session

WEDNESDAY

wednesday 26 march

	D-TRACK	E-TRACK	T-TRACK	EXHIBITION THEATRE
0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
0830 – 1000	5.5 Boosting the Scalability of Formal Verification Technologies	5.6 Emerging logic technologies	5.7 Test generation and optimization	5.8 Embedded Tutorial: System Integration – The Bridge between More than Moore and More Moore
1000 – 1100	EXHIBITION AND COFFEE BREAK			
1000 – 1030	IP2 INTERACTIVE PRESENTATIONS, Conference Level, Foyer			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1100 – 1230	6.5 Beyond EDA: Extending the Application Domain of Formal Methods	6.6 Model-Based Design and Hardware/ Software Interfaces	6.7 Hardening Approaches at Different Design Levels	6.8 First Time Right in Analog Design Enabling New Business Cases
1230 – 1400	LUNCH BREAK			
1330 – 1400	7.0 SPECIAL DAY KEYNOTE, Saal 1			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1430 – 1600	7.5 Emerging memory technologies	7.6 Performance and timing analysis	7.7 Design-for-Test and Test Access	7.8 FD-SOI – the Enabling European Technology for Energy Efficient Solutions – Creating a Solution Hive & Design Hub as Eco-System for Future Success
1600 – 1700	COFFEE BREAK			
1600 – 1630	IP3 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1700 – 1830	8.5 Modeling & Specification	8.6 Mapping and Scheduling for Many-Core Embedded Systems	8.7 Performance Modeling and Delay Test	8.8 Hot Topic: Beyond CMOS Ultra-low-power Computing
1930 – 2300	DATE PARTY *co-sponsored by the City of Dresden*			

D-Track | A-Track | T-Track | E-Track

thursday 27 march

	SPECIAL DAY	D-TRACK	A-TRACK	D-TRACK
0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
0830–1000	9.1 SPECIAL DAY Hot Topic: CMOS scaling - from evolutionary to revolutionary computing	9.2 Low-Cost, High-Performance NoCs	9.3 Hardware Implementations for Data Security	9.4 Timing challenges in validation
1000 – 1100	EXHIBITION AND COFFEE BREAK			
1000 – 1030	IP4 INTERACTIVE PRESENTATIONS, Conference Level, Foyer			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
1100 – 1230	10.1 SPECIAL DAY Hot Topic: Memories today and tomorrow	10.2 Wireless NoCs	10.3 Green Computing Systems	10.4 System-level evaluation
1230 – 1400	LUNCH BREAK			
1330 – 1400	11.0 SPECIAL DAY KEYNOTE, Saal 1			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
1400 – 1530	11.1 SPECIAL DAY Embedded Tutorial: Alternatives to CMOS	11.2 Transitioning NoC Design Techniques to Future Challenges	11.3 Industry relevant research and practice for system design	11.4 Enabling validation on fast platforms
1530 – 1600	COFFEE BREAK			
1530 – 1600	IP5 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer			
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2
1600 – 1730	12.1 SPECIAL DAY Hot Topic: The future of interfacing to the natural world	12.2 Hot topic: How Secure are PUFs Really? On the Reach and Limits of Recent PUF Attacks	12.3 Multimedia Systems	12.4 Physical Aspects

Special Day 2 | Special Session | IP Session | Exhibition Theatre Session

thursday 27 march

	D-TRACK	E-TRACK	D-TRACK	EXHIBITION THEATRE
0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
0830–1000	9.5 Hot Topic: Connecting Different Worlds – Technology Abstraction for Reliability-Aware Design and Test	9.6 Schedulability analysis	9.7 Timing Analysis and Cell Design	9.8 Embedded Tutorial: Memcomputing: the Cape of Good Hope
1000 – 1100	EXHIBITION AND COFFEE BREAK			
1000 – 1030	IP4 INTERACTIVE PRESENTATIONS, Conference Level, Foyer			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1100 – 1230	10.5 Analysis of Components and Systems	10.6 Multi-processor and distributed systems	10.7 Advances in Synthesis	10.8 EDA+3D+ MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics
1230 – 1400	LUNCH BREAK			
1330 – 1400	11.0 SPECIAL DAY KEYNOTE, Saal 1			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1400 – 1530	11.5 Memory Resource Allocation and Scheduling in MPSoC	11.6 System-Level Thermal Estimation and Management	11.7 Power and Emerging Technologies in Reconfigurable Computing	11.8 Embedded Tutorial: GPGPUs: how to combine high computational power with high reliability
1530 – 1600	COFFEE BREAK			
1530 – 1600	IP5 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer			
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1600 – 1730	12.5 System-level Design Space Exploration	12.6 Error Resilience and Power Management	12.7 Built-in self-test solutions for mixed-signal and RF ICs	12.8 Panel: Future SoC verification methodology: UVM evolution or revolution?

D-Track | A-Track | T-Track | E-Track

0730	**WORKSHOP REGISTRATION AND WELCOME REFRESHMENTS**
Breaks	**PLEASE SEE INDIVIDUAL WORKSHOP PROGRAMMES FOR LUNCH AND BREAK TIMES**

0830-1700 Konferenz 1	0830-1700 Konferenz 2	0830-1700 Konferenz 3	0830-1700 Konferenz 4
W1 International Workshop on Dependable GPU Computing	W2 ES4CPS - Engineering Simulations for Cyber-Physical Systems	W3 Electronic System-Level Design towards Heterogeneous Computing	W4 Workshop on Design Automation for Understanding Hardware Designs
0815-1630 Konferenz 5	**0830-1630 Konferenz 6**	**0830-1700 Seminar 5+6**	**0830-1700 Seminar 3+4**
W5 3D Integration: Applications, Technology, Architecture, Design, Automation, and Test	W6 MEDIAN - Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale	W7 Memristor Science & Technology	W8 3PMCES – Performance, Power and Predictability of Many-Core Embedded Systems

MONDAY 24 MARCH 2014

0730-0930		**Tutorial Registration and Welcome Refreshments**
0930-1100		**Tutorials** (1100-1130 Coffee Break)
M01	Konferenz 1	**Development of mixed-criticality systems based on system partitioning**
M02	Konferenz 2	**Software Debug on ARM Processors in Emulation**
M03	Konferenz 3	**Automatic fixed-point conversion: a gate way to high-level power optimization**
M04	Konferenz 4	**Dynamic Heterogeneous Architectures to Address The Efficiency Crisis!**
M05	Konferenz 6	**Wireless NoC as Interconnection Backbone for Multicore Chips: Promises, Challenges, and Recent Developments**
M06	Konferenz 5	**Testing of TSV-Based 2.5D- and 3D-Stacked ICs**
1300-1430		**Lunch**
1330		**CONFERENCE REGISTRATION BEGINS**
1430-1800		**Tutorials** (1600-1630 Coffee Break)
M07	Konferenz 1	**L4/Fiasco.OC - A Microkernel OS Designed for Security, Real-Time and Reliability**
M08	Konferenz 2	**Microfluidic Biochips: A Vision for More than Moore and Biochemistry-on-Chip**
M09	Konferenz 3	**Energy-Efficient System Design Through Error-Resilient Computing**
M10	Konferenz 4	**A Cyber-Physical Approach to Modeling, Simulation and Verification of Smart Systems**
M11	Konferenz 6	**Post-Silicon Validation and Debug: Best Practices and Disruptive Innovation**
M12	Konferenz 5	**All You Need to Know About Hardware Trojans and Counterfeit Ics**
1800-1900		**Welcome Reception**
1900-2100		**ACM SIGDA/EDAA PhD Forum**

TUTORIALS tutorials

Tutorials Chair: **Franco Fummi,** Universita' di Verona, IT

Twelve pre-conference tutorials will be given on Monday. All tutorials are half-day tutorials, six to be given in the morning (M01-M06) and six in the afternoon (M07-M12). A participant should enroll for one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only).

The titles, organisers, speakers, and abstracts of the tutorials are given hereafter:

M01

Konferenz 1

0930 **DEVELOPMENT OF MIXED-CRITICALITY SYSTEMS BASED ON SYSTEM PARTITIONING**

Speakers: **Alfons Crespo,** Universidad Politécnica de Valencia, ES
Alejandro Alonso, Universidad Politécnica de Madrid, ES
Jon Pérez, IK4-IKERLAN, ES

Modern embedded applications typically integrate a multitude of functionalities with potentially different criticality levels into a single system. In addition, the increasing power of mono-core and multi-core processors make it possible to integrate them in a single platform. However, this implies a number of challenges, being the integration of mixed-criticality applications one of them. System partitioning emerges as a powerful alternative for dealing with these challenges. An hypervisor allows creating several virtual machines, that run with spatial and temporal isolation. Applications are assigned to partitions, according to several criteria, such as its criticality. Resources are assigned to virtual machines, to guarantee the fulfilment of applications time requirements. This approach is also valid for multi-cores. This tutorial will introduce the attendee the basic techniques in the development of partitioned high integrity embedded systems, which will be illustrated with an industrial case study. This development relies on the XtratuM hypervisor and supporting tools for validation, partitioning, and code and configuration files generation. This tutorial will benefit attendees from the industry, as it will show in a practical manner the basics in the development of partitioned embedded systems. They could have an idea on how to integrate this approach on their current practices. Attendees from the academia will get acquainted with advance development techniques and open research topics. In addition, the availability of the development framework can be the base of laboratory assignments on advanced courses.

M02

Konferenz 2

0930 **SOFTWARE DEBUG ON ARM PROCESSORS IN EMULATION**

Speaker: **Russ Klein,** Mentor, US

Emulation systems can execute designs fast enough to run significant amounts of software. For example, one can execute the software boot process, run diagnostics, boot an OS, load and exercise drivers. This allows earlier access to the design for the software team. It also allows software to be used to drive activity; exercising realistic use cases as part of the hardware verification. This software will need to be debugged. The emulated design will likely contain all the debug facilities, such as JTAG and ETM, as the final device. These can be used in emulation just as they would on the final silicon. Emulators will allow access to signals around the core, not accessible in the final device, which can used to debug and trace the processor. This gives the developer a number of options for debugging. This session explores the different debug approaches available, trade-offs involved in each approach, and how and when they can be most effectively applied during the design cycle. Russ Klein is a Technical Director in Mentor's emulation division. He has been developing verification and debug solutions which span the boundaries between hardware and software for over 20 year.

M03

Konferenz 3

0930 **AUTOMATIC FIXED-POINT CONVERSION: A GATE WAY TO HIGH-LEVEL POWER OPTIMIZATION**

Speakers: **Daniel Ménard,** INSA Rennes, FR
David Novo, EPFL, CH
Karthick Parashar, Imperial College London, GB
Olivier Sentieys, Inria and University of Rennes, FR

Given that Moore's law scaling has hit the power-wall, reducing power consumption of high-performance embedded systems becomes very crucial. It is also well admitted that system-level techniques offer the greatest potential for optimizing power. In this tutorial, we demonstrate how the careful tuning of the fixed-point arithmetic used to implement numerous functionalities in embedded system applications, can lead to significant savings in power consumption. Interestingly, proper dimensioning of the bit widths used to represent signals or variables can reduce the power consumption in both hardware and software implementations. Even in software implementation, the pervasive use of Single Instruction Multiple Data (SIMD) datapaths in modern processors is pushing designers to meddle with bit allocation. Often, a reduction in bit widths can enable the use of more SIMD slots, which increases the parallelism boosting the speed and energy efficiency of the software implementation. Although quantization effects in digital signal processing systems have been studied since the 70's, significant progress has been made in the recent years. This tutorial packs nearly a decade of research in designing systems with fixed-point arithmetic. We expose the deficiency in the support offered by existing EDA tools and motivate the need for new solutions. Accordingly, we put into perspective several recent techniques that have been developed to facilitate a quick analysis of the impact of a selected fixed-point format on the system performance and cost. We analyze the fixed-point refinement in a comprehensive way from a tools perspective, dividing the problem into various design steps (e.g., range and precision analysis). For each step, we present concrete solutions amenable to design automation that are illustrated with multiple relevant design examples from the wireless communication, multi-media and other signal processing domains.

M04

Konferenz 4

0930 DYNAMIC HETEROGENEOUS ARCHITECTURES TO ADDRESS THE EFFICIENCY CRISIS!

Speakers: **Houman Houmayoun,** George Mason University, US
Farhang Yazdani, BroadPak Corporation, US
Ayse Coskun, Boston University, US
Hank Hoffmann, University of Chicago, US

The microprocessor industry is at a crossroads. While it continues to scale performance with each generation, we continue to drive this critically important technology domain. When performance scaling stops, microprocessors become a generic commodity and no longer a technology driver or enabler. Because modern processors are most heavily constrained by power, and sometimes energy, constraints, performance scaling no longer falls naturally from increased transistor counts. Instead, total performance is maximized by maximizing performance/Watt. Future computing platforms will need to be flexible, scalable, conservative on power, while saving size, weight, energy, etc. In addressing these challenges, microprocessor industry is moving towards heterogeneous architecture design. Heterogeneous designs promise to push the envelope of power efficiency further by enabling general purpose processors to achieve the efficiency of customized cores. By enabling more diverse designs, and designs that are customized dynamically, we can push the efficiency envelope even further. This tutorial first reviews the major challenges facing semiconductor industry; in general performance, power, temperature and reliability, and in specific dark and unreliable silicon. The tutorial then introduces the concept of heterogeneous architecture to address the efficiency crisis and briefly reviews the state of the art in static and dynamic heterogeneous architectures in industry and academia. The tutorial then presents 3D design concept and argue how it can eliminate the fundamental barrier to dynamic heterogeneity. Finally it reviews the state of the art in simulators and modeling tools and how they can be integrated to accurately model performance, power, area, and temperature in 3D heterogeneous architectures. About the Team: The team consists of experts in interdisciplinary areas including heterogeneous architecture and 3D design (Houman Homayoun), temperature-aware design, DRAM and 3D integration (Ayse Coskun), 3D fabrication and packaging (Farhang Yazdani), and system architecture design (Hank Hoffman). The team consists of three faculties and one industry expert in the field. Houman Homayoun is an Assistant Professor of the Department of Electrical and Computer Engineering at George Mason University.

M05

Konferenz 6

0930 WIRELESS NOC AS INTERCONNECTION BACKBONE FOR MULTICORE CHIPS: PROMISES, CHALLENGES, AND RECENT DEVELOPMENTS

Speakers: **Radu Marculescu,** Carnegie Mellon University, US
Partha Pratim Pande, Washington State University, US
Deukhyoun Heo, Washington State University, US
Hiroki Matsutani, Keio University, JP

Continuing progress and integration levels in silicon technologies make possible complete end-user systems consisting of extremely high number of cores on a single chip targeting either embedded or high-performance computing. However, without new approaches for energy- and thermally-efficient design, as well as scalable, low power and high bandwidth on-chip communication architectures, this vision may remain a pipe dream. Towards this end, wireless Network-on-Chip (WiNoC) represents an emerging paradigm for designing low power, high bandwidth interconnect infrastructure for multicore chips. This tutorial will provide a timely and insightful journey into various challenges and emerging solutions of designing WiNoC architectures from a variety of different perspectives, ranging from very high levels of abstraction (e.g., system architecture) to very low levels (e.g., on-chip antenna and transceiver design). The tutorial will start by discussing the fundamentals of network-based communication for 2D and 3D multicore systems and advanced design techniques for multi-domain clock and power management for embedded and high-performance processors, using real examples of multicore platforms. The second part of the tutorial will focus on the design of high bandwidth and low power WiNoC architectures incorporating the small-world effects. We will present detailed performance evaluation and necessary design trade-offs for the small-world WiNoCs with respect to their conventional wireline counterparts. We will conclude this part of the tutorial by presenting design of on-chip millimeter (mm)-wave wireless link as the suitable physical layer for the WiNoCs. In the last part, we will complement the above discussions regarding planar WiNoCs by introducing the wireless 3D NoCs that use inductive coupling though-chip interfaces (TCIs) to connect stacked chips by square coils as data transmitters. We will present design and implementation of wireless 3D NoC systems, real-chip experimental results, and their interconnection techniques. By scope and contents, this tutorial targets students and researchers belonging to both academia and industry.

M06

Konferenz 5

0930 TESTING OF TSV-BASED 2.5D- AND 3D-STACKED ICS

Speakers: **Erik Jan Marinissen,** IMEC - Leuven, BE
Krishnendu Chakrabarty, Duke University - Durham, NC, US

Stacked ICs with vertical interconnect containing fine-pitch microbumps and through-silicon vias (TSVs) are a hot-topic in design and manufacturing communities. These 2.5D- and 3D-SICs hold the promise of heterogeneous integration, inter-die connections with increased performance at lower power dissipation, and increased yield and hence decreased product cost. However, testing for manufacturing defects remains an obstacle and potential showstopper before stacked-die products can become a reality. There are concerns about the cost or, even worse, feasibility of testing such TSV-based 3D chips. In this tutorial, we present key concepts in 3D technology, terminology, and benefits. We discuss design and test challenges and emerging solutions for 2.5D- and 3D-SICs. Topics to be covered include an overview of 3D integration and trendsetting products such as a 2.5D-FPGA and 3D-stacked memory chips, test flows and test content for 3D chips, advances in wafer probing, 3D design-for-test architectures and ongoing IEEE P1838 standardization efforts for test access, and 3D test cost modeling and test-flow selection.

M07

Konferenz 1

1430 L4/FIASCO.OC - A MICROKERNEL OS DESIGNED FOR SECURITY, REAL-TIME AND RELIABILITY

Speakers: **Hermann Härtig,** TU Dresden, DE
Adam Lackorzynski, Kernkonzept GmbH, DE
Carsten Weinhold, TU Dresden, DE
Björn Döbel, TU Dresden, DE

Modern embedded systems contain an increasing amount of software components with differing requirements in terms of real-time guarantees, security isolation, and reliability. In order to reduce production cost it is desirable to consolidate many such applications into a single hardware platform. Such consolidation requires an operating system that suits these differing application requirements. L4/Fiasco.OC is a microkernel operating system developed as a research project at TU Dresden and now commercially supported by Kernkonzept GmbH. The operating system has been constantly evolved for the past 15 years to accomodate real-time, security, and reliability use cases. Commercially, the microkernel is the foundation of Deutsche Telekom's SIMKo3 high-security smartphone, which was certified for German Government use in September 2013. This tutorial will give an insight into Fiasco.OC's features. Talks by Fiasco.OC developers and researchers will explore usage enarios. A hands-on session lets participants get first-hand experience in Fiasco.OC system setup and application development.

M08

Konferenz 2

1430 MICROFLUIDIC BIOCHIPS: A VISION FOR MORE THAN MOORE AND BIOCHEMISTRY-ON-CHIP

Speakers: **Tsung-Yi Ho,** National Cheng Kung University, TW
Krishnendu Chakrabarty, Duke University, US

The tutorial offers attendees an opportunity to bridge the semiconductor ICs/system industry with the biomedical and pharmaceutical industries. The tutorial will first describe emerging applications in biology and biochemistry that can benefit from advances in electronic "biochips". The presenters will next describe technology platforms for accomplishing "biochemistry on a chip", and introduce the audience to both the droplet-based "digital" microfluidics based on electrowetting actuation and flow-based "continuous" microfluidics based on microvalve technology. Next, the presenters will describe system-level synthesis includes operation scheduling and resource binding algorithms, and physical-level synthesis includes placement and routing optimizations. In this way, the audience will see how a "biochip compiler" can translate protocol descriptions provided by an end user (e.g., a chemist or a nurse at a doctor's clinic) to a set of optimized and executable fluidic instructions that will run on the underlying microfluidic platform. Testing techniques will be described to detect faults after manufacture and during field operation. A classification of defects will be presented based on data for fabricated chips. Appropriately fault models will be developed and presented to the audience. On-line and off-line reconfiguration techniques will be presented to bypass faults once they are detected. The problem of mapping a small number of chip pins to a large number of array electrodes will also be covered. Finally, sensor feedback-based cyberphysical adaptation will be covered. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial.

MONDAY

M09

Konferenz 3

1430 ENERGY-EFFICIENT SYSTEM DESIGN THROUGH ERROR-RESILIENT COMPUTING

Speakers: **Saibal Mukhopaddhyay,** University of Georgia Tech., US
Shidhartha Das, ARM Ltd., GB
Anand Raghunathan, Purdue University, US
Srimat Chakradhar, NEC Labs, US

This is a half-day tutorial that covers a broad range of technologies for error-resilient computing, and highlights the significant role of resiliency technologies in achieving high energy-efficiency across different levels of abstractions (circuit, hardware architecture and software) in modern computing systems. Safety-margins added to address the impact of rising variations at nanometer geometries incur unacceptable power and performance overheads. Traditional adaptive techniques compensate for some manifestations of these variations, however, they require margins to account for localized and fast-changing variations. The adverse impact of margins has led to a recent research focus on so-called "error-resilient" techniques, both in academia and industry. Resilient techniques permit computational errors to occur at run-time, either by operating without the full setup margin or by deliberately designing for inexact outputs. In lieu of the "always-correct" output as mandated in the traditional model of computing, computing with errors enables significant improvements in energy-efficiency as long as the error-rate and/or the magnitude of errors are sufficiently low. Resilient techniques have wide-ranging applications that span high-performance general-purpose computing to digital signal processing (DSP) algorithms. In this tutorial, we provide an in-depth overview of error-resilient techniques encompassing circuits, micro-architectural, algorithmic and system-architecture aspects. We organize the material into two segments. In the first, we discuss error-resilient techniques for bit-exact applications where perfect recovery from errors is a key requirement. We briefly review the existing design space for traditional adaptive techniques and motivate the case for error-resiliency by analyzing the additional margins eliminated through explicit error-detection and correction. We then discuss error-detection and recovery approaches for microprocessor pipelines highlighting "Razor" as a specific example. We present measurement results from academia and industry on resilient techniques similar to Razor. The second segment of the tutorial focuses on "approximate" computing; an approach to computing that defines correctness as producing outputs of acceptable "quality". Many applications (such as web search, data analytics, sensor data processing, recognition, mining, and synthesis) have a high degree of intrinsic resilience to their underlying computations being executed incorrectly. We review software, hardware architecture and circuit design techniques to build approximate computing systems. These new techniques significantly improve performance or energy efficiency while ensuring that the results produced are acceptable. We will conclude with a discussion of the key challenges that need to be addressed in order to facilitate a broader adoption of approximate computing.

M10

Konferenz 4

1430 A CYBER-PHYSICAL APPROACH TO MODELING, SIMULATION AND VERIFICATION OF SMART SYSTEMS

Speakers: **Davide Quaglia,** EDALab s.r.l., IT
Dimitris Drogoudis, Agilent, BE
Davide Bresolin, University of Bologna, IT

The design of future smart embedded systems should jointly take into account aspects from different domains, such as digital (hardware, software, network) and analog (electronic, electromechanical, etc., as for instance RF, MEMS, power sources, thermal issues, sensors and actuators) so that they can be considered ever more cyber-physical systems. To increase energy efficiency, to fully exploit the potential of current nanoelectronics technologies, as well as to enable the integration of existing/new IPs and "More than Moore" devices, new methodologies and tools for multi-disciplinary and multi-scale modeling, simulation and verification are needed. In engineering practice, the analysis of a complex system is usually carried on through simulation, which allows the engineer to explore one of the possible system executions at a time. Formal verification instead aims at exploring all possible executions, in order to be certain that a property of interest holds in all cases, or conversely acquire information about potential fault cases. Because of their heterogeneous nature, cyber-physical systems have a mixed discrete and continuous behavior, which makes them quite challenging for verification. In this tutorial, we survey state-of-the-art modeling, simulation and verification techniques for cyber-physical systems. The presentations will be accompanied by concrete tool introductions and demonstrations, showing how the presented concepts support improvement of today's state-of-the-art system-level design flow of smart systems. Most of this tutorial is based of the results of the SMAC European project on smart systems design. By scope and contents, this tutorial targets students and researchers belonging to both academia and industry.

M11

Konferenz 6

1430 POST-SILICON VALIDATION AND DEBUG: BEST PRACTICES AND DISRUPTIVE INNOVATION

Speakers: **Nagib Hakim,** Intel Corporation Santa Clara, US
Subhasish Mitra, Stanford University, US
Amir Nahir, IBM Research Labs Haifa, IL
Alan Hu, University of British Columbia, CA

Hardware failures are a growing concern as electronic systems become more complex, interconnected, and pervasive. The complexity challenge is further exacerbated by new ways of improving energy efficiency of electronic systems with the slowdown of CMOS (Dennard) scaling: increasing amounts of cores, uncore components, and accelerators; increasing degrees of adaptivity; and, increasing levels of heterogeneous integration. All these features and their complex interactions make future systems highly vulnerable to design flaws (bugs) that can jeopardize correct system operation and/or introduce security vulnerabilities. Existing validation methods barely cope with today's complexity. Traditional pre-silicon verification alone is no longer adequate. Post-silicon validation involves operating manufactured ICs in actual application environments to detect and fix bugs. Existing post-silicon practices are ad-hoc, and their costs are rising faster than design cost. Effective post-silicon validation requires a radical departure from today's ad-hoc practices to structured techniques. A wide range of topics will be covered in this tutorial, from best practices at leading companies to recent research results that are immediately applicable. Examples include: 1. overview of validation product life cycle; 2. trade-offs in pre- vs. post-silicon validation; 3. validation test content generation using the concept of exercisers; 4. validation infrastructure including triggers, observability structures, and performance monitors; 5. structured and systematic techniques such as QED (Quick Error Detection); 6. coverage metrics; 7. logic and electrical bug validation and debug techniques; 8. formal techniques for post-silicon validation and debug; 9. post-silicon repair, survivability, and resiliency; 10. bug benchmarks and industrial case studies.

MONDAY

M12

Konferenz 5

1430 ALL YOU NEED TO KNOW ABOUT HARDWARE TROJANS AND COUNTERFEIT ICS

Speakers: **Mark (Mohammad) Tehranipoor,** University of Connecticut, US
Domenic Forte, University of Connecticut, US

The migration from a vertical to horizontal business model has made it easier to introduce hardware Trojans and counterfeit electronic parts into the electronic component supply chain. Hardware Trojans are malicious modifications made to original IC designs that reduce system integrity (change functionality, leak private data, etc.). Counterfeit parts are often below specification and/or of substandard quality. The existence of Trojans and counterfeit parts creates risks for the life-critical systems and infrastructures that incorporate them including automotive, aerospace, military, and medical systems. In this tutorial, we will cover (i) Background and motivation for hardware Trojan and counterfeit prevention/detection; (ii) Taxonomies related to both topics; (iii) Existing solutions; (iv) Open challenges; (v) New and unified solutions to address these challenges.

TUESDAY 25 MARCH, 2014

1.1 Opening Plenary, DATE Awards Ceremony and Keynote Addresses

Grosser Saal 0830 – 1030

0830 **WELCOME ADDRESSES**

Gerhard Fettweis, DATE 2014 General Chair,
TU Dresden, DE
Luca Fanucci, DATE 2014 Programme Chair
University of Pisa, IT

0850 **PRESENTATION OF DISTINGUISHED AWARDS**

DATE 2014 BEST PAPER AWARDS

EDAA LIFETIME ACHIEVEMENT AWARD 2014
Rolf Ernst, TU Braunschweig, DE

EDAA OUTSTANDING DISSERTATION AWARDS 2013

ACM SIGDA DISTINGUISHED SERVICE AWARD
Peter Marwedel, TU Dortmund, DE

DATE FELLOW AWARD
Enrico Macii, Politecnico di Torino, IT

IEEE/CEDA OUTSTANDING SERVICE CONTRIBUTION AWARD 2013
Enrico Macii, Politecnico di Torino, IT

IEEE CS TTTC OUTSTANDING CONTRIBUTION AWARD
Enrico Macii, Politecnico di Torino, IT

IEEE FELLOW AWARD
Cecilia Metra, University of Bologna, IT

0910 **KEYNOTE ADDRESSESS**

0910 **SYSTEM DESIGN CHALLENGES FOR NEXT GENERATION WIRELESS AND EMBEDDED SYSTEMS**

David Fuller, National Instruments, US

0950 **THE GROWING IMPORTANCE OF MICROELECTRONICS FROM A FOUNDRY PERSPECTIVE**

Gerd Teepe, GLOBALFOUNDRIES, DE

1030 **EXHIBITION AND COFFEE BREAK** in Exhibition Area

2.1 EXECUTIVE SESSION: How to Handle Today's Design Complexity

Saal 1 1130 – 1300

Organiser: **Yervant Zorian,** Fellow & Chief Architect, Synopsys, US
Executives: **Sanjive Agarwala,** Fellow & Silicon Director, Texas Instruments, US
Paul Lo, Senior Vice President, Synopsys, US
Rainer Kress, Head Design Methodology, Infineon, DE
Leon Stock, Vice President, IBM, US
Sanjiv Taneja, Vice President, Cadence, US

The widening gap between growing SOC complexity and designer productivity limits traditional chip design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of complex SOC design. Executives in this session will discuss the impact of complexity and the new opportunities it may bring in designing today's SOC.

1300 **LUNCH BREAK** in Exhibition Area

2.2 Panel: Emerging vs. Established Technologies: a Two Sphinxes' Riddle at the Crossroads?

Konferenz 6 1130 – 1300

Organiser: **Marco Casale-Rossi,** Synopsys Inc., US
Chair: **Giovanni De Micheli,** EPFL, CH

Crossroads have always been challenging: they require a decision; in Egyptian and Greek mythology they were often guarded by two sphinxes trying to cheat the traveler with their riddles. The two sphinxes, the knight and the knave, the lady and the tiger, are just few instances of difficult puzzles that have kept logicians and mathematicians busy for the last 5,000 years. Today, you are walking down Moore's Law road when you come to a crossroads: one road brings you into the land of emerging technologies: 14, 10 and 7 nanometer, FD-SOI, FinFET, 3D-IC,... beyond and below; the other road holds you into the land of established technologies: 28, 40, 65, and 90 nanometers, possibly even above, A&M/S, MEMS,... Choosing the right road is critical to lead your project and your company to success, but making the right decision is increasingly difficult, as it encompasses complex technical and economic considerations. However, unlike the mythological traveler, you won't run into the sphinxes but, rather, into some of our industry best experts; unlike the sphinxes, they will strive to provide you with honest advice about the "road conditions", and you are allowed to ask multiple questions to them to figure out which road is the best for you.

Panelists: **Rob Aitken,** ARM Ltd., US
Antun Domic, Synopsys Inc., US
Manfred Horstmann, GLOBALFOUNDRIES, DE
Robert Hum, Mentor Graphics Corp., US
Philippe Magarshack, STMicroelectronics, FR

1300 **LUNCH BREAK** in Exhibition Area

2.3 Making automotive systems safer and more energy efficient

Konferenz 1 1130 – 1300

Chair: **Bart Vermeulen,** NXP, NL
Co-Chair: **Sebastian Steinhorst,** TUM-CREATE, SG

With the transition from hydraulic and mechanical automotive systems to electronic systems, the requirements on safety and energy efficiency are becoming increasingly important. The papers in this session address these issues by presenting robustness improvements at component and system level, advanced energy management at network level, and multi-variant design space exploration.

1130 **EMULATION-BASED ROBUSTNESS ASSESSMENT FOR AUTOMOTIVE SMART-POWER ICS**

Manuel Harrant[1], Thomas Nirmaier[1], Jerome Kirscher[1], Christoph Grimm[2] and Georg Pelz[1]
[1]Infineon Technologies AG, DE; [2]TU Kaiserslautern, DE

1200 **STARTUP ERROR DETECTION AND CONTAINMENT TO IMPROVE THE ROBUSTNESS OF HYBRID FLEXRAY NETWORKS**

Alexander Kordes[1], Bart Vermeulen[2], Abhijit Deb[2] and Michael Wahl[1]
[1]University of Siegen, DE; [2]NXP Semiconductors, NL

1230 **A SELF-PROPAGATING WAKEUP MECHANISM FOR POINT-TO-POINT NETWORKS WITH PARTIAL NETWORK SUPPORT**

Jan Reinke Seyler[1], Thilo Streichert[1], Juri Warkentin[1], Matthias Spägele[1], Michael Glaß[2] and Jürgen Teich[2]
[1]Daimler AG, DE; [2]University of Erlangen-Nuremberg, DE

1245 **MULTI-VARIANT-BASED DESIGN SPACE EXPLORATION FOR AUTOMOTIVE EMBEDDED SYSTEMS**

Sebastian Graf[1], Michael Glaß[1], Jürgen Teich[1] and Christoph Lauer[2]
[1]University of Erlangen-Nuremberg, DE; [2]AUDI AG Ingolstadt, DE

IPS **IP1-1, IP1-2**

1300 **LUNCH BREAK** in Exhibition Area

2.4 Modern Challenges in Analog and Mixed-Signal Design

Konferenz 2 1130 – 1300

Chair: **Georges Gielen,** KU Leuven, BE
Co-Chair: **Günhan Dündar,** Bogazici University, TR

The session addresses complex challenges in analogue and mixed-signal modeling and design. The regular papers present a novel, zonotope based approach to non-linear macromodeling and a new layout technique in analogue IC design that avoids failures due to IR-drop and electromigration. The two short papers discuss new mechanisms to select solutions from multi-dimensional Pareto-optimal fronts and efficient recording of activities in CMOS neural networks.

1130 **ELECTROMIGRATION-AWARE AND IR-DROP AVOIDANCE ROUTING IN ANALOG MULTIPORT TERMINAL STRUCTURES**

Ricardo Martins, Nuno Lourenco, António Canelas and Nuno Horta, Instituto de Telecomunicações, Instituto Superior Técnico – TU Lisbon, PT

1200 **ZONOTOPE-BASED NONLINEAR MODEL ORDER REDUCTION FOR FAST PERFORMANCE BOUND ANALYSIS OF ANALOG CIRCUITS WITH MULTIPLE-INTERVAL-VALUED PARAMETER VARIATIONS**

Yang Song, Sai Manoj PD and Hao Yu, Nanyang Technological University, SG

1230 **IMPLEMENTATION ISSUES IN THE HIERARCHICAL COMPOSITION OF PERFORMANCE MODELS OF ANALOG CIRCUITS**

Manuel Velasco-Jiménez, Rafael Castro-López, Elisenda Roca and Francisco Fernández, IMSE-CNM, CSIC and Universidad de Sevilla, ES

1245 **MODELING OF AN ANALOG RECORDING SYSTEM DESIGN FOR ECOG AND AP SIGNALS**

Nils Heidmann, Nico Hellwege, Tim Hoehlein, Thomas Westphal, Dagmar Peters-Drolshagen and Steffen Paul
University of Bremen, DE

IPS **IP1-3, IP1-4, IP1-5, IP1-6, IP1-7**

1300 **LUNCH BREAK** in Exhibition Area

2.5 Low-Power and Efficient Architectures

Konferenz 3 1130 – 1300

Chair: **Cristina Silvano,** Politecnico di Milano, IT
Co-Chair: **Todd Austin,** University of Michigan, US

This session presents three papers on energy efficiency in memory-intensive systems. The first paper aims at energy-efficient scheduling of cooperative-thread arrays on GPGPUs for memory intensive workloads through throttling of warps on different cores. The second paper leverages the application-specific knowledge of the next-generation parallelized high-efficiency video encoder to design a distributed scratchpad memory system with adaptive SPM data allocation and power management. The third paper explores the feasibility of non-volatile memories for instruction caches to improve energy efficiency. To handle the write delay and energy issues of NVMs, an analysis and extensions to the miss status handling registers are proposed.

1130 **ENERGY-EFFICIENT SCHEDULING FOR MEMORY-INTENSIVE GPGPU WORKLOADS**

Seokwoo Song[1], Minseok Lee[1], John Kim[1], Woong Seo[2], Yeongon Cho[2] and Soojung Ryu[2]
[1]KAIST, KR; [2]Samsung, KR

1200 **DSVM: ENERGY-EFFICIENT DISTRIBUTED SCRATCHPAD VIDEO MEMORY ARCHITECTURE FOR THE NEXT-GENERATION HIGH EFFICIENCY VIDEO CODING**

Felipe Sampaio[1], Muhammad Shafique[2], Bruno Zatt[3], Sergio Bampi[4] and Jörg Henkel[2]
[1]Federal University of Rio Grande do Sul, BR; [2]Karlsruhe Institute of Technology (KIT), DE; [3]Federal University of Pelotas, BR; [4]Federal University of Rio Grande do Sul, BR

1230 **FEASIBILITY EXPLORATION OF NVM BASED I-CACHE THROUGH MSHR ENHANCEMENTS**

Manu Komalan[1], José Ignacio Gómez Pérez[2], Christian Tenllado[2], Praveen Raghavan[3], Matthias Hartmann[3] and Francky Catthoor[3]
[1]IMEC, UCM(Universidad Complutense de Madrid), ES; [2]Universidad Complutense de Madrid, ES; [3]IMEC, BE

IPS **IP1-8, IP1-9, IP1-10, IP1-11**

1300 **LUNCH BREAK** in Exhibition Area

2.6 Real-Time memory hierarchies

Konferenz 4 1130 – 1300

Chair: **Benny Akesson,** CTU Prague, CZ
Co-Chair: **Marco Di Natale,** Scuola Superiore Sant'Anna, IT

The papers in this session deal with analysis and management of memory hierarchies for complex real-time systems, both from the deterministic and the probabilistic point of view.

1130 **ON THE CORRECTNESS, OPTIMALITY AND PRECISION OF STATIC PROBABILISTIC TIMING ANALYSIS**

Sebastian Altmeyer[1] and Robert Davis[2]
[1]University of Amsterdam, NL; [2]University of York, GB

1200 **WCET-CENTRIC DYNAMIC INSTRUCTION CACHE LOCKING**

Huping Ding[1], Yun Liang[2] and Tulika Mitra[1]
[1]School of Computing, National University of Singapore, SG; [2]Center for Energy-efficient Computing and Applications, School of EECS, Peking University, CN

1230 **MINIMIZING STACK MEMORY FOR HARD REAL-TIME APPLICATIONS ON MULTICORE PLATFORMS**

Chuansheng Dong and Haibo Zeng, McGill University, CA

1245 **TIME-PREDICTABLE EXECUTION OF MULTITHREADED APPLICATIONS ON MULTICORE SYSTEMS**

Ahmed Alhammad and Rodolfo Pellizzoni, University of Waterloo, CA

1300 **LUNCH BREAK** in Exhibition Area

2.7 Yield and Reliability for Robust Systems

Konferenz 5 1130 – 1300

Chair: **Joan Figueras,** UPC, ES
Co-Chair: **Jose Pineda de Gyvez,** NXP, NL

Robustness is increasingly a requirement for SOCs and memories, and effects such as wearout, BTI, and soft errors are important to consider as part of design. Another important component of robust design is tolerance of rare events. Understanding design robustness helps predict and enhance yield.

1130 **COMPREHENSIVE ANALYSIS OF ALPHA AND NEUTRON PARTICLE-INDUCED SOFT ERRORS IN AN EMBEDDED PROCESSOR AT NANOSCALES**

Mojtaba Ebrahimi[1], Adrian Evans[2], Mehdi B. Tahoori[1], Razi Seyyedi[1], Enrico Costenaro[3] and Dan Alexandrescu[3]
[1]Karlsruhe Institute of Technology, DE; [2]iRoC Technologies, DE; [3]iRoC Technologies, France, FR

1200 **BIAS TEMPERATURE INSTABILITY ANALYSIS OF FINFET BASED SRAM CELLS**

SEYAB KHAN[1], Innocent Agbo[2], Said Hamdioui[3], Halil Kukner[4], Ben Kaczer[4], Praveen Raghavan[5] and Francky Catthoor[4]
[1]Technical University Delft, NL; [2]TU Delft, NL; [3]Delft University of Technology, NL; [4]IMEC, BE; [5]IMEC, BE

1230 **SSFB: A HIGHLY-EFFICIENT AND SCALABLE SIMULATION REDUCTION TECHNIQUE FOR SRAM YIELD ANALYSIS**

Manish Rana and Ramon Canal, Universitat Politecnica de Catalunya, ES

IPS **IP1-12, IP1-13, IP1-14**

1300 **LUNCH BREAK** in Exhibition Area

2.8 Hot Topic: Technology Transfer towards Horizon 2020

Exhibition Theatre 1130 – 1300

Organiser: **Rainer Leupers,** RWTH Aachen, DE
Chair: **Norbert Wehn,** TU Kaiserslautern, DE

European research projects produce many excellent results, and the quality of research papers at DATE and other major European conferences is often outstanding. But how many academic research results in computing technologies and EDA actually make it into industrial practice? In the context of the transition into the Horizon 2020 framework program, the European research community is currently investigating novel ways of stimulating additional academia-industry technology transfer. This special session contributes by discussing concrete transfer experiences and new concepts. Furthermore it will exemplify several success stories from both academic and industrial perspectives.

1130 **THE TETRACOM APPROACH TO TECHNOLOGY TRANSFER**

Rainer Leupers, RWTH Aachen University, DE

1145 **LEVERAGING EUROPEAN RESEARCH TO CREATE VALUE**
Marco Roodzant, ACE Associated Compiler Experts bv, NL

1200 **SUCCESSFUL TECHNOLOGY TRANSFER – SHARING OF EXPERIENCE**
Johannes Stahl, Synopsys Inc., US

1215 **FROM RESEARCH TO MARKET: CASE STUDIES IN THE FIELD OF INNOVATIVE INTEGRATED ARCHITECTURES**
Luca Fanucci, University of Pisa, IT

1230 **OPEN SOURCE TECHNOLOGY TRANSFER: SCENARIOS AND VALUE CREATION**
Albert Cohen, INRIA, FR

1245 **SUPPORTING INTERNATIONAL TECHNOLOGY TRANSFER: OBJECTIVES AND OBSTACLES**
Bernd Janson, Consultant, DE

1300 **LUNCH BREAK** in Exhibition Area

3.1 EXECUTIVE SESSION: Advanced Technology Challenges & Opportunities

Saal 1 1430 – 1600

Organiser: **Yervant Zorian,** Fellow & Chief Architect, Synopsys, US
Executives: **Giorgio Cesana,** Director, STMicroelectronics, FR
Joachim Kunkel, Senior Vice President & GM, Synopsys, US
Rudy Lauwereins, VP, IMEC, BE
Maria Merced, President, TSMC, NL
Gerd Teepe, VP, GLOBALFOUNDRIES, DE

The continuous technology scaling and their new applications are dramatically impacting the semiconductor industry. This may also significantly affect the dependency between eco-system players necessitating smooth interdependency between them. The executives in this session will discuss upcoming innovations in the semiconductor industry and their impact on the solutions offered by the eco system players.

1600 **COFFEE BREAK** in Exhibition Area

3.2 Panel: The World Is Going… Analog & Mixed-Signal! What about EDA?

Konferenz 6 1430 – 1600

Organiser: **Marco Casale-Rossi,** Synopsys Inc., US
Chair: **Pietro Palella,** STMicroelectronics, IT

Contrarily to a common belief, the world is not going digital! Analog and mixed-signal electronics is more and more important and yet pervasive. This is due both to the increasing systems integration, by nature leading to heterogeneity, and to the complex, digital computing functions being complemented by scores of on-chip analog functions, interfacing/interacting with people, environment, and other systems. Specialty silicon foundries are now stable members of top ten revenue rankings. This technology trend demands for more design automation in both implementation and verification domains. Lossless interfaces between digital and analog design environments, multi-technology support, mixed-signal simulation engines – but also debugging aids - are no longer a nice to have. According to IBS, the cost of implementing and verifying the mixed-signal functions is generally over 50% of the design costs even though the mixed-signal transistors can be as low as 3% of the total! What are the critical requirement, moving forward, and what is EDA industry doing to serve the needs of this increasingly important semiconductor industry segment?

Panelists: **Mario Anton,** Micronas, DE
Ori Galzur, TowerJazz, IL
Robert Hum, Mentor Graphics Corp., US
Rainer Kress, Infineon Technologies, DE
Paul Lo, Synopsys Inc., US

1600 **COFFEE BREAK** in Exhibition Area

3.3 Secure Hardware Primitives and Implementations

Konferenz 1 1430 – 1600

Chair: **Paolo Maistri,** TIMA, FR
Co-Chair: **Patrick Schaumont,** Virginia Tech, US

System designers need secure building blocks for robust system protection against physical attacks. This session presents novel hardware designs and analysis on code-based cryptography, random number generators and IP protection mechanisms using watermarking.

1430 **LIGHTWEIGHT CODE-BASED CRYPTOGRAPHY: QC-MDPC MCELIECE ENCRYPTION ON RECONFIGURABLE DEVICES**
Ingo von Maurich and Tim Güneysu, Ruhr-Universität Bochum, DE

1500 **ON THE ASSUMPTION OF MUTUAL INDEPENDENCE OF JITTER REALIZATIONS IN P-TRNG STOCHASTIC MODELS.**
Patrick Haddad[1], Yannick Teglia[1], Florent BERNARD[2] and Viktor Fischer[3]
[1]ST Microelectronics, FR; [2]Laboratory Hubert Curien, University of Lyon, UJM Saint-Etienne, FR; [3]Hubert Curien Laboratory, Jean Monnet University, FR

1530 **CLOCK-MODULATION BASED WATERMARK FOR PROTECTION OF EMBEDDED PROCESSORS**
Jedrzej Kufel[1], Peter Wilson[1], Stephen Hill[2], Bashir Al-Hashimi[1], Paul N. Whatmough[3] and James Myers[3]
[1]University of Southampton, GB
[2]ARM, US
[3]ARM, GB

1600 **COFFEE BREAK** in Exhibition Area

3.4 Modeling and Optimization of Power Distribution Networks

Konferenz 2 1430 – 1600

Chair: **Luca Daniel,** MIT, US
Co-Chair: **Stefano Grivet-Talocia,** Politecnico di Torino, IT

The performance and robustness of 3D power distribution networks is of critical importance for state of the art electronic designs. The papers in this session discuss new modeling and optimization approaches for their efficient characterization and robust design, including order reduction, variability impact, via planning, decoupling capacitor selection, and thermal effects.

1430 **SENSITIVITY-BASED WEIGHTING FOR PASSIVITY ENFORCEMENT OF LINEAR MACROMODELS IN POWER INTEGRITY APPLICATIONS**

Andrea Ubolli[1], Stefano Grivet-Talocia[1], Michelangelo Bandinu[2] and Alessandro Chinea[2]
[1]Politecnico di Torino, IT; [2]IdemWorks s.r.l., IT

1500 **EFFICIENT ANALYSIS OF VARIABILITY IMPACT ON INTERCONNECT LINES AND RESISTOR NETWORKS**

Jorge Fernandez Villena[1] and Luis Miguel Silveira[2]
[1]INESC ID, PT; [2]INESC ID/IST - Lisbon University, PT

1530 **IMPLICIT INDEX-AWARE MODEL ORDER REDUCTION FOR RLC/RC NETWORKS**

Nicodemus Banagaaya[1], Giuseppe Ali'[2], Wil . H. A. Schilders[1] and Caren Tischendorf[3]
[1]Eindhoven University of Technology, NL; [2]University of Calabria and INFN, Gruppo collegato di Cosenza, IT; [3]Institute of Mathematics, Humboldt-Universität zu Berlin, DE

1545 **P/G TSV PLANNING FOR IR-DROP REDUCTION IN 3D-ICS**

Shengcheng Wang, Farshad Firouzi, Fabian Oboril and Mehdi Tahoori
Karlsruhe Institute of Technology, DE

IPS **IP1-15, IP1-16, IP1-17, IP1-18**

1600 **COFFEE BREAK** in Exhibition Area

3.5 Robust Architectures

Konferenz 3 1430 – 1600

Chair: **Todd Austin,** University of Michigan, US
Co-Chair: **Muhammad Shafique,** Karlsruhe Institute of Technology, DE

This session presents the design of novel architectures to support real-time and secure systems. The first paper couples a time-division multiplexed NoC with a real-time memory controller to design a cost-effective real-time system with improved worst-case latency at reduced area and power consumption. The next paper proposes bus designs for multi-cores that are analyzable for probabilistic timing analysis. The final paper in this session designs a lightweight hardware solution using lockstep shadow thread execution to detect and prevent code injection attacks.

1430 **COUPLING TDM NOC AND DRAM CONTROLLER FOR COST AND PERFORMANCE OPTIMIZATION OF REAL-TIME SYSTEMS**

Manil Dev Gomony[1], Benny Akesson[2] and Kees Goossens[3]
[1]Eindhoven University of Technology, NL; [2]Czech Technical University in Prague, CZ; [3]Eindhoven University of Technology, NL

1500 **BUS DESIGNS FOR TIME-PROBABILISTIC MULTICORE PROCESSORS**

Javier Jalle[1], Leonidas Kosmidis[1], Jaume Abella[2], Eduardo Quinones[1] and Francisco Cazorla[3]
[1]Barcelona Supercomputing Center, ES; [2]Barcelona Supercomputing Center (BSC-CNS), ES; [3]Barcelona Supercomputing Center and IIIA-CSIC, ES

1530 **PROGRAMMABLE DECODER AND SHADOW THREADS: TOLERATE REMOTE CODE INJECTION EXPLOITS WITH DIVERSIFIED REDUNDANCY**

Weidong Shi[1], Ziyi Liu[1], Shouhuai Xu[2] and Zhiqiang Lin[3]
[1]University of Houston, US; [2]University of Texas at San Antonio, US; [3]University of Texas at Dallas, US

IPS **IP1-19, IP1-20**

1600 **COFFEE BREAK** in Exhibition Area

3.6 Cyber Physical Systems: Security and Co-design

Konferenz 4 1430 – 1600

Chair: **Rolf Ernst,** Technische Universitaet Braunschweig, DE
Co-Chair: **Anuradha Annaswamy,** MIT, US

This session showcases recent results in cybersecurity and codesign in CPS. The first paper analyzes a stealth cyberattack scenario where a distributed sensor system is disturbed by an attacker who tries to reduce the sensor fusion quality and suggests an algorithmic approach to increase robustness against this attack. The second paper addresses the joint design of a feedback controller and a server-based resource reservation mechanism to guarantee closed-loop stability. The third paper describes a codesign approach formally guaranteeing control robustness for a communication channel with a bounded number of frame losses.

1430 **ATTACK-RESILIENT SENSOR FUSION**

Radoslav Ivanov, Miroslav Pajic and Insup Lee, University of Pennsylvania, US

1500 **BANDWIDTH-EFFICIENT CONTROLLER-SERVER CO-DESIGN WITH STABILITY GUARANTEES**

Amir Aminifar[1], Enrico Bini[2], Petru Eles[1] and Zebo Peng[1]
[1]Linkoping University, SE; [2]Lund University, SE

1530 **FAULT-TOLERANT CONTROL SYNTHESIS AND VERIFICATION OF DISTRIBUTED EMBEDDED SYSTEMS**

Matthias Kauer[1], Damoon Soudbakhsh[2], Dip Goswami[3], Samarjit Chakraborty[4] and Anuradha Annaswamy[5]
[1]TUM CREATE Ltd,, SG; [2]Masschussetts Institute of Technology, US; [3]Eindhoven University of Technology, NL; [4]TU Munich, DE; [5]MIT, US

IPS IP1-21, IP1-22, IP1-23

1600 **COFFEE BREAK** in Exhibition Area

3.7 On line Strategies for Reliability

Konferenz 5 1430 – 1600

Chair: **Fabrizio Lombardi,** Northwestern University, US
Co-Chair: **Jie Han,** University of Alberta, CA

This section presents different approaches to improve reliability of circuits and systems by using on line techniques. It shows different methods that can be applied to caches, processors and multicore architectures.

1430 **SPATIAL PATTERN PREDICTION BASED MANAGEMENT OF FAULTY DATA CACHES**

Georgios Keramidas[1], Michail Mavropoulos[2], Anna Karvouniari[2] and Dimitris Nikolos[2]
[1]Researcher, Univerity of Patras, GR; [2]University of Patras, GR

1500 **COMBINED DVFS AND MAPPING EXPLORATION FOR LIFETIME AND SOFT-ERROR SUSCEPTIBILITY IMPROVEMENT IN MPSOCS**

Anup Das[1], Akash Kumar[1], Bharadwaj Veeravalli[1], Cristiana Bolchini[2] and Antonio Miele[2]
[1]National University of Singapore, SG; [2]Politecnico di Milano, IT

1530 **DARP: DYNAMICALLY ADAPTABLE RESILIENT PIPELINE DESIGN IN MICROPROCESSORS**

Hu Chen, Sanghamitra Roy and Koushik Chakraborty, Utah State University, US

1600 **COFFEE BREAK** in Exhibition Area

3.8 Hot Topic: Mission Profile Aware Design – The Solution for Successful Design of Tomorrows Automotive Electronics

Exhibition Theatre 1430 – 1600

Organisers: **Goeran Jerke,** Robert Bosch GmbH, DE
Oliver Bringmann, University of Tuebingen, DE
Chair: **Goeran Jerke,** Robert Bosch GmbH, DE
Co-Chair: **Oliver Bringmann,** University of Tuebingen, DE

In order to benefit from modern automotive semiconductor technologies, application robustness must now be considered as a design target. This includes the consequent consideration of environmental stress conditions and functional loads, which are formalized in so-called "mission profiles". We introduce the motivation to use mission profiles from an OEM and Tier n perspective. Additionally, we introduce the mission profile aware design flow and present several application scenarios.

1430 **MISSION PROFILES – SOLUTION OR CHALLENGE? THE OEM PERSPECTIVE**

Ulrich Abelein, AUDI AG, DE

1500 **MISSION PROFILE AWARE IC DESIGN - A CASE STUDY**

Goeran Jerke[1] and Andrew Kahng[2]
[1]Robert Bosch GmbH, DE; [2]University of California, San Diego, US

1530 **MISSION PROFILE AWARE ROBUSTNESS ASSESSMENT OF AUTOMOTIVE POWER DEVICES**

Thomas Nirmaier[1], Andreas Burger[2], Manuel Harrant[1], Alexander Viehl[2], Oliver Bringmann[3], Wolfgang Rosenstiel[3] and Georg Pelz[1]
[1]Infineon Technologies AG, DE; [2]FZI Research Center for Information Technology, DE; [3]University of Tuebingen, DE

1545 **APPLICATION OF MISSION PROFILES TO ENABLE CROSS-DOMAIN CONSTRAINT-DRIVEN DESIGN**

Carolin Katzschke[1], Marc-Philipp Sohn[1], Markus Olbrich[1], Volker Meyer zu Bexten[2], Markus Tristl[2] and Erich Barke[1]
[1]Institute of Microelectronic Systems, Leibniz Universität Hannover, DE; [2]Infineon Technologies AG, DE

1600 **COFFEE BREAK** in Exhibition Area

IP1 Interactive Presentations

Conference Level, Foyer 1600 – 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP1-1 **SAFE: SECURITY-AWARE FLEXRAY SCHEDULING ENGINE**

Gang Han[1], Haibo Zeng[2], Yaping Li[3] and Wenhua Dou[1]
[1]National University of Defense Technology, CN; [2]McGill University, CA; [3]The Chinese University of Hong Kong, CN

IP1-2 **TRANSIENT ERRORS RESILIENCY ANALYSIS TECHNIQUE FOR AUTOMOTIVE SAFETY CRITICAL APPLICATIONS**

Sujan Pandey and Bart Vermeulen, NXP Semiconductors, NL

IP1-3 **MODEL BASED HIERARCHICAL OPTIMIZATION STRATEGIES FOR ANALOG DESIGN AUTOMATION**

Engin Afacan[1], Gunhan Dundar[1], Faik Baskaya[1], Simge Ay[1] and Francisco Fernandez[2]
[1]Bogazici University, TR; [2]Universidad de Sevilla, TR

IP1-4 **A NOVEL LOW POWER 11-BIT HYBRID ADC USING FLASH AND DELAY LINE ARCHITECTURES**

Hsun-Cheng Lee and Jacob Abraham,
University of Texas, Austin, US

IP1-5 **SEMI-SYMBOLIC ANALYSIS OF MIXED-SIGNAL SYSTEMS INCLUDING DISCONTINUITIES**

Carna Radojicic, Christoph Grimm, Javier Moreno and Xiao Pan, TU Kaiserslautern, DE

IP1-6 **NOVEL CIRCUIT TOPOLOGY SYNTHESIS METHOD USING CIRCUIT FEATURE MINING AND SYMBOLIC COMPARISON**

Cristian Ferent and Alex Doboli, Stony Brook University, US

IP1-7 **AN EMBEDDED OFFSET AND GAIN INSTRUMENT FOR OPAMP IPS**

Jinbo Wan and Hans KerkHoff, CAES-TDT, CTIT, University of Twente, NL

IP1-8 **EVX: VECTOR EXECUTION ON LOW POWER EDGE CORES**

Milovan Duric[1], Oscar Palomar[1], Aaron Smith[2], Osman Unsal[1], Adrian Cristal[1], Mateo Valero[1] and Doug Burger[2]
[1]Barcelona Supercomputing Center, ES; [2]Microsoft Research, US

IP1-9 **PROGRAM AFFINITY PERFORMANCE MODELS FOR PERFORMANCE AND UTILIZATION**

Ryan Moore and Bruce Childers, University of Pittsburgh, US

IP1-10 **ADVANCED SIMD: EXTENDING THE REACH OF CONTEMPORARY SIMD ARCHITECTURES**

Matthias Boettcher[1], Giacomo Gabrielli[2], Mbou Eyole[2], Alastair Reid[2] and Bashir M. Al-Hashimi[1]
[1]University of Southampton, GB; [2]ARM Ltd., GB

IP1-11 **A TIGHTLY-COUPLED HARDWARE CONTROLLER TO IMPROVE SCALABILITY AND PROGRAMMABILITY OF SHARED-MEMORY HETEROGENEOUS CLUSTERS**

Paolo Burgio[1], Robin Danilo[2], Andrea Marongiu[3], Philippe Coussy[4] and Luca Benini[5]
[1]University of Bologna, Université de Bretagne-Sud, IT; [2]Université de Bretagne-Sud, FR; [3]University of Bologna, IT; [4]Universite de Bretagne-Sud / Lab-STICC, FR; [5]Università di Bologna, IT

IP1-12 **INFORMER: AN INTEGRATED FRAMEWORK FOR EARLY-STAGE MEMORY ROBUSTNESS ANALYSIS**

Shrikanth Ganapathy[1], Ramon Canal[1], Dan Alexandrescu[2], Enrico Costenaro[2], Antonio Gonzalez[3] and Antonio Rubio[1]
[1]Universitat Politecnica de Catalunya, ES; [2]iRoC Technologies, FR; [3]Intel and Universitat Politecnica de Catalunya, ES

IP1-13 **WEAR-OUT ANALYSIS OF ERROR CORRECTION TECHNIQUES IN PHASE-CHANGE MEMORY**

Caio Hoffman, Luiz Ramos, Rodolfo Azevedo and Guido Araújo, University of Campinas, BR

IP1-14 **APPROXIMATING THE AGE OF RF/ANALOG CIRCUITS THROUGH RE-CHARACTERIZATION AND STATISTICAL ESTIMATION**

Doohwang Chang[1], Sule Ozev[1], Ozgur Sinanoglu[2] and Ramesh Karri[3]
[1]Arizona State University, US; [2]New York University Abu Dhabi, AE; [3]Polytechnic Institute of New York University, US

IP1-15 **PACKAGE GEOMETRIC AWARE THERMAL ANALYSIS BY INFRARED-RADIATION THERMAL IMAGES**

jui-hung chien[1], Hao Yu[2], Ruei-Siang Hsu[3], Hsueh-Ju Lin[3] and Shih-Chieh Chang[3]
[1]Industrial Technology Research Institute, TW; [2]None, TW; [3]NTHU, TW

IP1-16 **COST-EFFECTIVE DECAP SELECTION FOR BEYOND DIE POWER INTEGRITY**

Yi-En Chen[1], Tu-Hsung Tsai[1], Shi-Hao Chen[2] and Hung-Ming Chen[1]
[1]Department of Electronics Engineering National Chiao Tung University Hsinchu, Taiwan 300, R.O.C., TW; [2]Global Unichip Corp, Hsinchu, Taiwan, TW

IP1-17 **CHARACTERIZING POWER DELIVERY SYSTEMS WITH ON/OFF-CHIP VOLTAGE REGULATORS FOR MANY-CORE PROCESSORS**

Xuan Wang, Jiang Xu, Zhe Wang, Kevin J. Chen, Xiaowen Wu and Zhehui Wang, HKUST, HK

IP1-18 **MASK-COST-AWARE ECO ROUTING**

Hsi-An Chien[1], Zhen-Yu Peng[1], Yun-Ru Wu[2], Ting-Hsiung Wang[2], Hsin-Chang Lin[2], Chi-Feng Wu[2] and Ting-Chi Wang[1]
[1]National Tsing Hua University, TW; [2]Realtek Semiconductor Corp., TW

IP1-19 **EXPLOITING NARROW-WIDTH VALUES FOR IMPROVING NON-VOLATILE CACHE LIFETIME**

Guangshan Duan and Shuai Wang, Nanjing University, CN

IP1-20 **PARTIAL-SET: WRITE SPEEDUP OF PCM MAIN MEMORY**

Li Bing[1], Shan Shuchang[2], Hu Yu[2] and Li XiaoWei[3]
[1]ICT,UCAS, CN; [2]ICT,CAS, CN; [3]ICT.CAS, CN

IP1-21 **GARBAGE COLLECTION FOR MULTI-VERSION INDEX ON FLASH MEMORY**

Kam-Yiu Lam[1], Jian-Tao Wang[1], Yuan-Hao Chang[2], Jen-Wei Hsieh[3], Po-Chun Huang[4], Chung Keung Poon[5] and ChunJiang Zhu[1]
[1]City University of Hong Kong, HK; [2]Academia Sinica, TW; [3]National Taiwan University of Science and Technology, TW; [4]Acadmia Sinica, TW; [5]City University of Hong Kong, TW

IP1-22 **D2CYBER: A DESIGN AUTOMATION TOOL FOR DEPENDABLE CYBERCARS**

Arslan Munir and Farinaz Koushanfar, Rice University, US

IP1-23 **CONTRACT-BASED DESIGN OF CONTROL PROTOCOLS FOR SAFETY-CRITICAL CYBER-PHYSICAL SYSTEMS**

Pierluigi Nuzzo, John Finn, Antonio Iannopollo and Alberto Sangiovanni-Vincentelli, University of California at Berkeley, US

IP1-24 **A FAULT DETECTION MECHANISM IN A DATA-FLOW SCHEDULED MULTITHREADED PROCESSOR**

Jian Fu[1], Qiang Yang[1], Raphael Poss[1], Chris Jesshope[1] and Chunyuan Zhang[2]
[1]University of Amsterdam, NL; [2]National University of Defense Technology, CN

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

4.1 EXECUTIVE SESSION: Addressing Challenges of Reliable Chips

Saal 1 1700 – 1830

Organiser: **Yervant Zorian,** Fellow & Chief Architect, Synopsys, US
Executives: **Dan Alexandrescu,** President & CEO, iROC Technologies, FR
Robert Aitken, Fellow, ARM, US
Robert Hum, GM & VP, Mentor Graphics, US
Ronald Martino, VP Microcontroller, Freescale, US

While today's SOCs systematically use semiconductor production quality assessment and optimization solutions, meeting end-product requirements for reliability and availability augments the need to prepare the SOC design in advance to address such requirements. The speakers in this executive session will address the current trends and challenges in the semiconductor reliability and discuss the level of readiness needed in a chip to meet today's SOC requirements.

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.2 Hot Topic: Multicore Systems in Safety Critical Electronic Control Units for Automotive and Avionics

Konferenz 6 1700 – 1830

Organisers: **Jürgen Becker,** KIT, DE
Oliver Sander, KIT, DE
Chair: **Jürgen Becker,** KIT, DE
Co-Chair: **Oliver Sander,** KIT, DE

Future applications in automotive and avionics show an ever increasing demand of computational processing power. The use of multicore devices is now emerging in embedded electronics. However these solutions are not directly applicable because of technical requirements that come along with the domain of safety critical and mixed critical applications, such as in automotive or avionics. The major challenge for deployment of multicore devices in safety critical applications such as automotive or avionics, is the lack of determinism and support of segregation due to shared resources. The goal of this session is to present the challenges that arise from the use of multicore devices in embedded safety-critical systems and mixed critical systems.

1700 **AUTOSAR AND MULTICORE**

Stefan Kuntz[1] and Rolf Schneider[2]
[1]Continental Automotive GmbH, DE; [2]AUDI AG, DE

1730 **CONCEPTS TO VALIDATE THE SAFE APPLICATION OF MULTICORE ARCHITECTURES IN THE AVIONICS DOMAIN**

Ottmar Bender[1], Laurent Dieudonné[2]
[1]Cassidian Electronics, DE; [2]Liebherr-Aerospace Lindenbarg GmbH, DE

1800 **MONITORING AND WCET ANALYSIS IN COTS MULTI-CORE-SOC-BASED MIXED-CRITICALITY SYSTEMS**

Jan Nowotsch[1], Michael Paulitsch[2], Arne Henrichsen[3], Werner Pongratz[3] and Andreas Schacht[3]
[1]EADS Innovation Works, DE; [2]EADS Innovation Work, DE; [3]Cassidian, DE

1815 **HARDWARE VIRTUALIZATION SUPPORT FOR SHARED RESOURCES IN MIXED-CRITICALITY MULTICORE SYSTEMS**

Oliver Sander[1], Timo Sandmann[1], Viet Vu Duy[1], Steffen Bähr[1], Falco Bapp[1], Juergen Becker[1], Hans Ulrich Michel[2], Dirk Kaule[2], Daniel Adam[2], Enno Luebbers[3], Jürgen Hairbucher[3], Andre Richter[4], Christian Herber[4] and Andreas Herkersdorf[4]
[1]KIT, DE; [2]BMW F+T, DE; [3]Intel GmbH, DE; [4]Technische Universität München, DE

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.3 Secure Device Identification

Konferenz 1 1700 – 1830

Chair: **Tim Gueneysu,** RUB, DE

Physically Unclonable Functions (PUF) have received much attention for fingerprinting of electronic devices. This session presents novel constructions and threats on Ring-Oscillator-based and Sense-Amplifier-based PUFs.

1700 **ARO-PUF: AN AGING-RESISTANT RING OSCILLATOR PUF DESIGN**

MD. TAUHIDUR RAHMAN[1], Domenic Forte[1], Jim Fahrny[2] and Mohammad Tehranipoor[1]
[1]University of Connecticut, US; [2]Comcast, US

1730 **AN EFFICIENT RELIABLE PUF-BASED CRYPTOGRAPHIC KEY GENERATOR IN 65NM CMOS**

Mudit Bhargava[1] and Ken Mai[2]
[1]ARM, US; [2]Carnegie Mellon University, US

1800 **INCREASING THE EFFICIENCY OF SYNDROME CODING FOR PUFS WITH HELPER DATA COMPRESSION**

Matthias Hiller and Georg Sigl, Institute for Security in Information Technology; Technische Universität München, DE

1815 **KEY-RECOVERY ATTACKS ON VARIOUS RO PUF CONSTRUCTIONS VIA HELPER DATA MANIPULATION**

Jeroen Delvaux[1] and Ingrid Verbauwhede[2]
[1]KU Leuven, BE; [2]KU Leuven - COSIC, BE

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.4 "Almost there" emerging technologies

Konferenz 2 1700 – 1830

Chair: **Ian O'Connor,** University of Lyon, FR
Co-Chair: **Michael Niemier,** University of Notre Dame, US

The three papers in this session all address "nearer-term" emerging technologies. Stochastic computing techniques are becoming increasingly relevant as CMOS becomes more error prone, numerous industrial and academic efforts are targeting 3D integration, and inte-

grated microfluidics promise to have a profound impact on healthcare and other domains.

1700 **IIR FILTERS USING STOCHASTIC ARITHMETIC**

Naman Saraf, Kia Bazargan, David J Lilja and Marc D Riedel, University of Minnesota, Twin Cities, US

1730 **EFFICIENT TRANSIENT THERMAL SIMULATION OF 3D ICS WITH LIQUID-COOLING AND THROUGH SILICON VIAS**

Alain Fourmigue, Giovanni Beltrame and Gabriela Nicolescu, Polytechnique Montreal, CA

1800 **A LOGIC INTEGRATED OPTIMAL PIN-COUNT DESIGN FOR DIGITAL MICROFLUIDIC BIOCHIPS**

Trung Anh Dinh[1], Shigeru Yamashita[1] and Tsung-Yi Ho[2]
[1]Ritsumeikan University, JP; [2]National Cheng Kung University, TW

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.5 Memory System Architectures

Konferenz 3 1700 – 1830

Chair: **Muhammad Shafique,** Karlsruhe Institute of Technology, DE
Co-Chair: **Cristina Silvano,** Politecnico di Milano, IT

The memory sub-system plays an increasingly important role in modern multicore systems. Novel solutions are needed in order to deliver the expected performance improvements with minimal energy overheads. In addition, new solutions should be preferably backward compatible with already existing approaches. In this session we have four papers dealing with different aspects of the memory hierarchy in modern computing systems. ALLARM provides a novel, yet power efficient strategy towards cache coherence to simultaneously improve performance and reduce energy. The next paper in this session presents a novel packet-based interface and compression, which reduces communication overhead. The third paper deals with prefetcher aggressiveness and proposes a sound solution to reduce overall execution time. The last paper of this session proposes a novel extension of the shared L2 cache memory system, providing a very high aggregated bandwidth with a very low impact on L2 cache design complexity or operating frequency.

1700 **ACHIEVING EFFICIENT PACKET-BASED MEMORY SYSTEM BY EXPLOITING CORRELATION OF MEMORY REQUESTS**

Tianyue Lu, Licheng Chen and Mingyu Chen, Institute of Computing Technology, Chinese Academy of Sciences, CN

1730 **ALLARM: OPTIMIZING SPARSE DIRECTORIES FOR THREAD-LOCAL DATA**

Amitabha Roy[1] and Timothy Jones[2]
[1]EPFL, CH; [2]University of Cambridge, GB

1800 **INTRODUCING THREAD CRITICALITY AWARENESS IN PREFETCHER AGGRESSIVENESS CONTROL**

Biswabandan Panda and Shankar Balachandran, IIT Madras, IN

1815 **A MULTI BANKED - MULTI PORTED - NON BLOCKING SHARED L2 CACHE FOR MPSOC PLATFORMS**

Igor Loi and Luca Benini
University of Bologna, IT

IPS **IP2-2, IP2-3, IP2-4**

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.6 Code Generation and Optimization for Embedded Platforms

Konferenz 4 1700 – 1830

Chair: **Heiko Falk,** Ulm University, DE
Co-Chair: **Florence Maraninchi,** Grenoble IMP/VERIMAG, FR

This session covers the broad spectrum of topics in compilers, code optimization, and validation under consideration of today's embedded platforms. The first paper addresses the automated validation of binary translators. The second paper focusses on the on-device optimization of apps and system libraries of mobile platforms. The third paper deals with the code generation of Android image processing applications for heterogeneous GPU-based architectures. The session is rounded off by short presentations of work-in-progress ideas on model transformation, energy and wear-leveling optimization, and scheduling/register allocation.

1700 **EATBIT: EFFECTIVE AUTOMATED TEST FOR BINARY TRANSLATION WITH HIGH CODE COVERAGE**

Hui Guo[1], Zhenjiang Wang[1], Chenggang Wu[1] and Ruining He[2]
[1]Institute of Computing Technology, Chinese Academy of Sciences, CN; [2]University of California, San Diego, US

1730 **ON-DEVICE OBJECTIVE-C APPLICATION OPTIMIZATION FRAMEWORK FOR HIGH-PERFORMANCE MOBILE PROCESSORS**

Garo Bournoutian and Alex Orailoglu, University of California, San Diego, US

1800 **CODE GENERATION FOR EMBEDDED HETEROGENEOUS ARCHITECTURES ON ANDROID**

Richard Membarth, Oliver Reiche, Frank Hannig and Jürgen Teich, University of Erlangen-Nuremberg, DE

IPS **IP2-5, IP2-6, IP2-7, IP2-8**

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.7 Dependable System Design

Konferenz 5 1700 – 1830

Chair: **Yiorgos Makris,** University of Texas at Dallas, US
Co-Chair: **Haralampos Stratigopoulos,** IMAG, FR

This section presents a variety of techniques to improve dependability of digital systems, showing how to improve security and fault tolerance at system level.

1700 **REAL-TIME TRUST EVALUATION IN INTEGRATED CIRCUITS**

Yier Jin and Dean Sullivan, The University of Central Florida, US

1730 **VERIFICATION-GUIDED VOTER MINIMIZATION IN TRIPLE-MODULAR REDUNDANT CIRCUITS**

Dmitry Burlyaev, Pascal Fradet and Alain Girault, INRIA, FR

1800 **TRADE-OFFS IN EXECUTION SIGNATURE COMPRESSION FOR RELIABLE PROCESSOR SYSTEMS**

Jonah Caplan[1], Maria Mera[2], Peter Milder[2] and Brett Meyer[1]
[1]McGill University, CA; [2]SUNY Stonybrook, US

1815 **AN ENERGY-AWARE FAULT TOLERANT SCHEDULING FRAMEWORK FOR SOFT ERROR RESILIENT CLOUD COMPUTING SYSTEMS**

Yue Gao, Sandeep Gupta, Yanzhi Wang and Massoud Pedram, University of Southern California, US

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

4.8 State-of-the-art in Verification: European Tertulia IC Design - Enabling AMS Structured Verification / Verification in FPGA & IP design flows

Exhibition Theatre 1700 – 1830

Organiser: **Andreas Brüning,** Silicon Saxony, DE

1700 **BRING ASIC-ALIKE VERIFICATION TO YOUR FPGA & IP DESIGN FLOW**

Scott Calkins, Blue Pearl Software Inc, US

1720 **ENABLING AMS STRUCTURED VERIFICATION**

1830 **EXHIBITION RECEPTION IN SEVERAL SERVING POINTS INSIDE THE EXHIBITION AREA (TERRACE LEVEL)**

SPECIAL DAY special day

WEDNESDAY 26 MARCH, 2014

5.1 SPECIAL DAY Hot Topic: Predictable Multi-Core Computing

Saal 1 0830 – 1000

Organiser: **Jürgen Teich,** University of Erlangen-Nuremberg, DE
Chair: **Petru Eles,** Linkoping University, SE
Co-Chair: **Jürgen Teich,** University of Erlangen-Nuremberg, DE

The requirement of high performance computing at low power can be met by the parallel execution of an application on a possibly large number of programmable cores. However, the lack of accurate timing properties may prevent parallel execution from being applicable to time-critical applications. This session treats this important problem of time predictability of applications on multi-core platforms by presenting results of the impact of resource sharing on performance, an architecture that has been designed to meet predictability requirements as well as new results on scheduling mixed critical applications on multi-core platforms.

0830 **IMPACT OF RESOURCE SHARING ON PERFORMANCE AND PERFORMANCE PREDICTION**

Jan Reineke and Reinhard Wilhelm, Informatik, Universität des Saarlandes, DE

0900 **TIME-CRITICAL COMPUTING ON A SINGLE CHIP MASSIVELY PARALLEL PROCESSOR**

Benoît Dupont de Dinechin, Kalray, FR

0930 **MAPPING MIXED-CRITICALITY APPLICATIONS ON MULTI-CORE ARCHITECTURES**

Georgia Giannopoulou, Nikolay Stoimenov, Pengcheng Huang and Lothar Thiele
ETH Zurich, CH

1000 **COFFEE BREAK** in Exhibition Area

5.2 Hot Topic: Hacking and Protecting Hardware: Threats and Challenges

Konferenz 6 0830 – 1000

Organisers: **Said Hamdioui,** TU Delft, NL
Giorgio Di Natale, LIRMM, FR
Chair: **Said Hamdioui,** TU Delft, NL
Co-Chair: **Giorgio Di Natale,** LIRMM, FR

For this Hot-Topic Session, we will have four leading researchers and experienced speakers from different companies to address both hacking and protecting ICs for chip data. Two speakers will focus on the weaknesses of IC and systems and the ways they can be hacked to

retrieve secret data, while the other two will cover smart schemes that can be used to protect ICs from such attacks.

0830 **HARDWARE ATTACKS ON SECURE ICS**

Gerard van Battum, Brightsight, NL

0852 **ATTACKING SMART PHONES**

Jean-Luc Danger, Secure IC, FR

0915 **SECURING SYSTEM ON CHIPS**

Fethulah Smailbegovic, ESCRYPT GmbH – Embedded Security, DE

0937 **SILICONAP: A SILICON AUTHENTICATION PLATFORM FOR SECURITY AND ANTI- COUNTERFEITING**

Mohammad Tehranipoor, TrueLogic, US

1000 **COFFEE BREAK** in Exhibition Area

5.3 Reliable Systems in the Age of Variability

Konferenz 1 0830 – 1000

Chair: **Antonio Miele,** Politecnico di Milano, IT
Co-Chair: **José L. Ayala,** Complutense University of Madrid, ES

The evolution of the silicon industry over past decades has been fueled by continued scaling. This has motivated the rapid evolution of integration technologies. In future technology nodes, reliability is expected to become a first-order design constraint. This session tackles this with novel techniques, spanning from memoization to latency-insensitive systems, proposing to tolerate, recover and manage reliability issues in a more variable scenario.

0830 **TEMPORAL MEMOIZATION FOR ENERGY-EFFICIENT TIMING ERROR RECOVERY IN GPGPUS**

Abbas Rahimi[1], Luca Benini[2] and Rajesh Gupta[1]
[1]UC San Diego, US; [2]Università di Bologna, IT

0900 **RELIABILITY-AWARE EXCEPTIONS: TOLERATING INTERMITTENT FAULTS IN MICROPROCESSOR ARRAY STRUCTURES**

waleed dweik, Murali Annavaram and Michel Dubois, University of Southern California, US

0930 **TEMPERATURE AWARE ENERGY-RELIABILITY TRADE-OFFS FOR MAPPING OF THROUGHPUT-CONSTRAINED APPLICATIONS ON MULTIMEDIA MPSOCS**

Anup Das, Akash Kumar and Bharadwaj Veeravalli, National University of Singapore, SG

0945 **RECOVERY-BASED RESILIENT LATENCY-INSENSITIVE SYSTEMS**

Yuankai Chen[1], Xuan Zeng[2] and Hai Zhou[1]
[1]Northwestern University, US; [2]Fudan University, CN

IPS **IP2-10, IP2-11, IP2-12**

1000 **COFFEE BREAK** in Exhibition Area

5.4 Prediction and optimization of timing variations

Konferenz 2 0830 – 1000

Chair: **Antonio Rubio,** UPC Barcelona, ES
Co-Chair: **Marisa López Vallejo,** UPM Madrid, ES

The session addresses yield analysis due to timing variations as well as various flip flop design techniques improving timing margins under variability.

0830 **EFFICIENT HIGH-SIGMA YIELD ANALYSIS FOR HIGH DIMENSIONAL PROBLEMS**

Moning Zhang, Zuochang Ye and Yan Wang, Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, CN

0900 **SUB-THRESHOLD LOGIC CIRCUIT DESIGN USING FEEDBACK EQUALIZATION**

Mahmoud Zangeneh and Ajay Joshi, Boston University, US

0930 **STOCHASTIC ANALYSIS OF BUBBLE RAZOR**

Guowei Zhang[1] and Peter Beerel[2]
[1]Tsinghua University, CN; [2]Univ. of Southern California, US

IPS **IP2-13, IP2-14, IP2-15**

1000 **COFFEE BREAK** in Exhibition Area

5.5 Boosting the Scalability of Formal Verification Technologies

Konferenz 3 0830 – 1000

Chair: **Fahim Rahim,** Atrenta, FR
Co-Chair: **Bernd Becker,** University of Freiburg, DE

While the industrial usage of formal methods has proliferated in the past decade, the capacity limitations of these techniques remains a challenge to their applicability. This session introduces a set of novel advances to boost the scalability of numerous state-of-the-art verification core technologies.

0830 **SCALABLE LIVENESS VERIFICATION FOR COMMUNICATION FABRICS**

Sebastiaan Joosten and Julien Schmaltz, Open University, NL

0900 **PROPERTY DIRECTED INVARIANT REFINEMENT FOR PROGRAM VERIFICATION**

Tobias Welp[1] and Andreas Kuehlmann[2]
[1]UC Berkeley, US; [2]Coverity, Inc., US

0930 **SIMPLE INTERPOLANTS FOR LINEAR ARITHMETIC**

Christoph Scholl[1], Florian Pigorsch[1], Stefan Disch[1] and Ernst Althaus[2]
[1]University Freiburg, DE; [2]University Mainz, DE

0945 **TIGHTENING BDD-BASED APPROXIMATE REACHABILITY WITH SAT-BASED CLAUSE GENERALIZATION**

Gianpiero Cabodi, Paolo Pasini, Stefano Quer and Danilo Vendraminetto, Politecnico di Torino, IT

1000 **COFFEE BREAK** in Exhibition Area

5.6 Emerging logic technologies

Konferenz 4 0830 – 1000

Chair: **Mehdi Tahoori,** KIT, DE
Co-Chair: **Marco Ottavi,** University of Rome "Tor Vergata", IT

The papers in this session consider new ways to realize both Boolean and non-Boolean logic. Potential implementations are based on graphene, spin, and resonance energy transfer.

0830 **RETLAB: A FAST DESIGN-AUTOMATION FRAMEWORK FOR ARBITRARY RET NETWORKS**

Mohammad Mottaghi, Arjun Rallapalli and Chris Dwyer, Duke University, US

0900 **DESIGN OF 3D NANOMAGNETIC LOGIC CIRCUITS: A FULL-ADDER CASE STUDY**

Robert Perricone, X. Sharon Hu, Joe Nahas and Michael Niemier, University of Notre Dame, US

0930 **HIGHLY ACCURATE SPICE-COMPATIBLE MODELING FOR SINGLE- AND DOUBLE-GATE GNRFETS WITH STUDIES ON TECHNOLOGY SCALING**

Morteza Gholipour[1], Ying-Yu Chen[2], Amit Sangai[2] and Deming Chen[2]
[1]University of Tehran, IR; [2]University of Illinois at Urbana-Champaign, US

0945 **REWIRING FOR THRESHOLD LOGIC CIRCUIT MINIMIZATION**

Chia-Chun Lin[1], Chun-Yao Wang[1], Yung-Chih Chen[2] and Ching-Yi Huang[1]
[1]Dept. of Computer Science, National Tsing Hua University, TW; [2]Dept. of Computer Science and Engineering, Yuan Ze University, TW

IPS **IP2-17, IP2-18, IP2-19**

1000 **COFFEE BREAK** in Exhibition Area

5.7 Test Generation and Optimization

Konferenz 5 0830 – 1000

Chair: **Xiaoqing Wen,** Kyushu Institute of Technology, JP
Co-Chair: **Grzegorz Mrugalski,** Mentor Graphics, PL

The session covers generation of tests for different fault models including interconnect opens, interconnect for 3D memories, and small delay faults. Additionally test optimization for SoC designs is presented.

0830 **EFFICIENT SMT-BASED ATPG FOR INTERCONNECT OPEN DEFECTS**

Dominik Erb[1], Karsten Scheibler[1], Matthias Sauer[2] and Bernd Becker[2]
[1]University of Freiburg, Chair of Computer Architecture, DE; [2]University of Freiburg, DE

0900 **INTERCONNECT TEST FOR 3D STACKED MEMORY-ON-LOGIC**

Mottaqiallah Taouil[1], Mahmoud Masadeh[1], Said Hamdioui[1] and Erik Jan Marinissen[2]
[1]Delft University of Technology, NL; [2]IMEC, BE

0930 **AN EFFECTIVE APPROACH TO AUTOMATIC FUNCTIONAL PROCESSOR TEST GENERATION FOR SMALL-DELAY FAULTS**

Andreas Riefert[1], Lyl Ciganda[2], Matthias Sauer[1], Paolo Bernardi[2], Matteo Sonza Reorda[3] and Bernd Becker[1]
[1]University of Freiburg, DE; [2]Politecnico di Torino, IT; [3]Politecnico di Torino - DAUIN, IT

0945 **MULTI-SITE TEST OPTIMIZATION FOR MULTI-VDD SOCS USING SPACE- AND TIME-DIVISION MULTIPLEXING**

FOTIOS VARTZIOTIS[1], Chrysovalantis Kavousianos[2], Krishnendu Chakrabarty[3], Rubin Parekhji[4] and Arvind Jain[4]
[1]University of Ioannina, GR; [2]Department of Computer Science and Engineering, University of Ioannina, GR; [3]Duke University, US; [4]Texas Instruments, IN

IPS **IP2-20, IP2-21, IP2-22**

1000 **COFFEE BREAK** in Exhibition Area

5.8 Hot Topic: System Integration - The Bridge between More than Moore and More Moore

Exhibition Theatre 0830 – 1000

Organisers: **Manfred Dietrich,** Fraunhofer IIS/EAS Dresden, DE
Kai Hahn, University Siegen, DE
Chair: **Manfred Dietrich,** Fraunhofer IIS/EAS Dresden, DE
Co-Chair: **Kai Hahn,** University Siegen, DE

System Integration using 3D technology is a very promising way to cope with current and future requirements for electronic systems. Since the pure shrinking of devices (known as "More Moore") will come to an end due to physical and economic restrictions, the integration of systems (e.g. by stacking dies, or by adding sensor functions) shows a way to maintain the growth in complexity as well as in diversity which is necessary for future applications. This so called "More than Moore" approach complements the conventional SoC product engineering. This session gives insights in System Integration design challenges from different perspectives, ranging from design technology over MEMS product engineering and 3D interconnect to automotive cyber physical systems.

0830 **DESIGN TECHNOLOGY FOR 3-D INTEGRATED SYSTEMS**

Andy Heinig, Fraunhofer IIS/EAS, DE

0845 **SEMICONDUCTOR PACKAGING IS BACK TO EUROPE - ADVANCES IN SYSTEM INTEGRATION IN WAFER LEVEL PACKAGING**

Steffen Kroehnert, NANIUM S.A. - Niederlassung Dresden, DE

0900 **MEMS AND 3D-IC PRODUCT ENGINEERING - TECHNOLOGY DESIGN FOR SYSTEM INTEGRATION**

Kai Hahn, University Siegen, DE

0915 **3D-TSV-HUB: POTENTIALS AND CHALLENGES FOR VERTICAL INTERCONNECTS IN NETWORKS-ON-CHIPS**

Andreas Herkersdorf, TU München, DE

0930 **SENSORS AND POWER DRIVERS, BRIDGE BETWEEN SYSTEM ENVIRONMENT AND COMPUTING**

Jochen Reisinger, Infineon Technologies Austria AG, AT

0945 **CONCLUSIONS AND DISCUSSION**

Manfred Dietrich, Fraunhofer, DE

1000 **COFFEE BREAK** in Exhibition Area

IP2 Interactive Presentations

Conference Level, Foyer 1000 – 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP2-1 **FAST AND ACCURATE COMPUTATION USING STOCHASTIC CIRCUITS**

Armin Alaghi and John P. Hayes, University of Michigan - Ann Arbor, US

IP2-2 **DRAM-BASED COHERENT CACHES AND HOW TO TAKE ADVANTAGE OF THE COHERENCE PROTOCOL TO REDUCE THE REFRESH ENERGY**

Zoran Jaksic and Ramon Canal, Universitat Politecnica de Catalunya, ES

IP2-3 **REDUCING SET-ASSOCIATIVE L1 DATA CACHE ENERGY BY EARLY LOAD DATA DEPENDENCE DETECTION (ELD3)**

Alen Bardizbanyan[1], Magnus Själander[2], David Whalley[2] and Per Larsson-edefors[1]
[1]Chalmers University of Technology, SE; [2]Florida State University, US

IP2-4 **DISTRIBUTED COOPERATIVE SHARED LAST-LEVEL CACHING IN TILED MULTIPROCESSOR SYSTEM ON CHIP**

Preethi Parayil Mana Damodaran[1], Stefan Wallentowitz[2] and Andreas Herkersdorf[3]
[1]LIS, Technical University of Munich, DE; [2]Technische Universität München, Institute for Integrated Systems, DE; [3]TU München, DE

IP2-5 **DESIGN OF SAFETY CRITICAL SYSTEMS BY REFINEMENT**

Alex Iliasov[1], Arseniy Alekseyev[2], Danil Sokolov[3] and Andrey Mokhov[3]
[1]Newcastle University, GB; [2]Newcastle University, ZW; [3]Newcastle University, BB

IP2-6 **ENERGY OPTIMIZATION IN ANDROID APPLICATIONS THROUGH WAKELOCK PLACEMENT**

Faisal Alam[1], Preeti Ranjan Panda[1], Nikhil Tripathi[2], Namita Sharma[3] and Sanjiv Narayan[2]
[1]IIT Delhi, IN; [2]Calypto Design Systems, IN; [3]Indian Institute of Technology Delhi, IN

IP2-7 **A WEAR-LEVELING-AWARE DYNAMIC STACK FOR PCM MEMORY IN EMBEDDED SYSTEMS**

Qingan Li[1], Yanxiang He[2], Yong Chen[2], Chun Xue[3], Nan Jiang[2] and Chao Xu[2]
[1]Wuhan University & City University of Hong Kong, CN; [2]Wuhan University, CN; [3]City University of Hong Kong, CN

IP2-8 **LIFETIME HOLES AWARE REGISTER ALLOCATION FOR CLUSTERED VLIW PROCESSORS**

Xuemeng Zhang[1], Hui Wu[2], Haiyan Sun[1] and Jingling Xue[3]
[1]National University of Defense Technology, CN; [2]The University of New South Wales, AU; [3]UNSW, AU

IP2-9 **A LOW-POWER, HIGH-PERFORMANCE APPROXIMATE MULTIPLIER WITH CONFIGURABLE PARTIAL ERROR RECOVERY**

Cong Liu[1], Jie Han[1] and Fabrizio Lombardi[2]
[1]University of Alberta, CA; [2]Northeastern University, US

IP2-10 **A LINUX-GOVERNOR BASED DYNAMIC REALIABILITY MANAGER FOR ANDROID MOBILE DEVICES**

Pietro Mercati[1], Andrea Bartolini[2], Francesco Paterna[1], Tajana Simunic Rosing[1] and Luca Benini[2]
[1]UCSD, US; [2]University of Bologna, IT

IP2-11 **YIELD AND TIMING CONSTRAINED SPARE TSV ASSIGNMENT FOR THREE-DIMENSIONAL INTEGRATED CIRCUITS**

Yu-Guang Chen[1], Kuan-Yu Lai[1], Ming-Chao Lee[2], Yiyu Shi[3], Wing-Kai Hon[1] and Shih-Chieh Chang[1]
[1]National Tsing Hua University, TW; [2]MediaTek Inc., TW; [3]Missouri University of Science and Technology, US

IP2-12 **COMPILER-DRIVEN DYNAMIC RELIABILITY MANAGEMENT FOR ON-CHIP SYSTEMS UNDER VARIABILITIES**

Semeen Rehman, Florian Kriebel, Muhammad Shafique and Jörg Henkel, Karlsruhe Institute of Technology (KIT), DE

IP2-13 **MINIMIZING STATE-OF-HEALTH DEGRADATION IN HYBRID ELECTRICAL ENERGY STORAGE SYSTEMS WITH ARBITRARY SOURCE AND LOAD PROFILES**

Yanzhi Wang[1], Xue Lin[1], Qing Xie[1], Naehyuck Chang[2] and Massoud Pedram[1]
[1]University of Southern California, US; [2]Seoul National University, KR

IP2-14 **DYNAMIC FLIP-FLOP CONVERSION TO TOLERATE PROCESS VARIATION IN LOW POWER CIRCUITS**

mehrzad nejat, Bijan Alizadeh and Ali Afzali Kusha
School of Electrical and Computer Eng., College of Eng., University of Tehran, IR

IP2-15 **A LOW POWER AND ROBUST CARBON NANOTUBE 6T SRAM DESIGN WITH METALLIC TOLERANCE**

LUO SUN[1], Jimson Mathew[1], Rishad Shafik[2], Dhiraj Pradhan[1] and Zhen Li[1]
[1]University of Bristol, GB; [2]University of Southampton, GB

IP2-16 **MAKE IT REAL: EFFECTIVE FLOATING-POINT REASONING VIA EXACT ARITHMETIC**

Miriam Leeser, Saoni Mukherjee, Jaideep Ramachandran and Thomas Wahl
Northeastern University, US

IP2-17 **WIDTH MINIMIZATION IN THE SINGLE-ELECTRON TRANSISTOR ARRAY SYNTHESIS**

Chian-Wei Liu[1], Chang-En Chiang[1], Ching-Yi Huang[1], Chun-Yao Wang[1], Yung-Chih Chen[2], Suman Datta[3] and Vijaykrishnan Narayanan[4]
[1]Dept. of Computer Science, National Tsing Hua University, TW; [2]Dept. of Computer Science and Engineering, Yuan Ze University, TW; [3]Department of Electrical Engineering, The Pennsylvania State University, US; [4]Department of Computer Science and Engineering, The Pennsylvania State University, US

IP2-18 **AREA MINIMIZATION SYNTHESIS FOR RECONFIGURABLE SINGLE-ELECTRON TRANSISTOR ARRAYS WITH FABRICATION CONSTRAINTS**

Yi-Hang Chen, Jian-Yu Chen and Juinn-Dar Huang, Department of Electronics Engineering, National Chiao Tung University, TW

IP2-19 **SOFTWARE-BASED PAULI TRACKING IN FAULT-TOLERANT QUANTUM CIRCUITS**

Alexandru Paler[1], simon devitt[2], Kae Nemoto[2] and Ilia Polian[1]
[1]University of Passau, DE; [2]National Institute of Informatics, JP

IP2-20 **AN EFFICIENT TEMPERATURE-GRADIENT BASED BURN-IN TECHNIQUE FOR 3D STACKED ICS**

Nima Aghaee, Zebo Peng and Petru Eles, Linkoping University, SE

IP2-21 **TEST AND NON-TEST CUBES FOR DIAGNOSTIC TEST GENERATION BASED ON MERGING OF TEST CUBES**

Irith Pomeranz, Purdue University, US

IP2-22 **NEW IMPLEMENTIONS OF PREDICTIVE ALTERNATE ANALOG/RF TEST WITH AUGMENTED MODEL REDUNDANCY**

Haithem AYARI, Florence AZAIS, Serge BERNARD, Mariane COMTE, Vincent KERZERHO and Michel RENOVELL, LIRMM, CNRS/Univ. Montpellier 2, FR

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

1230 **LUNCH BREAK** in Exhibition Area

6.1 SPECIAL DAY Hot Topic: The fight against Dark Silicon

Saal 1 1100 – 1230

Organiser: **Jörg Henkel,** Karlsruhe Institute of Technology, DE
Chair: **Jörg Henkel,** Karlsruhe Institute of Technology, DE
Co-Chair: **Jürgen Teich,** University of Erlangen-Nuremberg, DE

Dark Silicon is predicted to dominate the chip footage of upcoming many-core systems within a decade since Dennard Scaling fails mainly due to the voltage-scaling problem that results in higher power densities. It would deem upcoming technologies nodes inefficient since a majority of cores would lie fallow. Significant research efforts have started within the last couple of years to investigate and mitigate Dark Silicon effects to ensure an effective use of available chip footage. This special session gives a snapshot of current research activities of this grand challenge. In particular, the three talks present the newest trends and developments starting with the problem of Dennard Scaling and how it mandates new design constraints followed by the problem of power delivery and cooling, and concluding with the newest directions in efficient resource management for many-core systems.

1100 **A LANDSCAPE OF THE NEW DARK SILICON DESIGN REGIME**

Michael Taylor, University of California, San Diego, US

1130 **INTEGRATED MICROFLUIDIC POWER GENERATION AND COOLING FOR BRIGHT SILICON MPSOCS**

Mohamed M. Sabry[1], Arvind Sridhar[1], Patrick Ruch[2], David Atienza[1] and Bruno Michel[2]
[1]EPFL, CH; [2]IBM Research, CH

1200 **EFFECTIVE RESOURCE MANAGEMENT TOWARDS EFFICIENT COMPUTING**

Per Stenström, Chalmers University of Technology, SE

1230 **LUNCH BREAK** in Exhibition Area

6.2 Embedded Tutorial: Emerging Transistor Technologies: From Devices to Architectures

Konferenz 6 1100 – 1230

Organisers: **Michael Niemier,** University of Notre Dame, US
X. Sharon Hu, University of Notre Dame, US
Chair: **Michael Niemier,** University of Notre Dame, US

This "vertically integrated" session is focused on emerging transistor technologies – particularly devices that operate at low voltages and that have steep slopes. It will: (1) introduce desirable (and undesirable) features of new device technologies; (2) highlight how new transistor technologies could impact von Neumann architectures; a particular emphasis will be placed on (a) heterogeneous multi-core architectures and accelerators (where heterogeneity stems from different device technologies) and (b) modeling efforts at all levels of the chip hierarchy (i.e., from the device-level to the architectural-level); (3) illustrate how new device technologies could lead to significant improvements in the performance/efficiency of non-von Neumann architectures. Notably, talks (2) and (3) will identify roles for new device technologies in hybrid analog-digital systems with an end goal of improved application-level performance/efficiency.

1100 **ENERGY EFFICIENT COMPUTING WITH TUNNEL FETS**

Adrian Ionescu, Arnab Biswas, Nilay Dagtekin and Livio Lattanzio, Nanolab, Ecole Polytechnique Fédérale de Lausanne, CH

1130 **MODELING STEEP SLOPE DEVICES: FROM CIRCUITS TO ARCHITECTURES**

Karthik Swaminathan[1], Moon Seok Kim[1], Nandhini Chandramoorthy[1], Behnam Sedighi[2], Robert Perricone[2], Jack Sampson[1] and Vijaykrishnan Narayanan[1]
[1]Pennsylvania State University, US; [2]University of Notre Dame, US

1200 **STEEP SLOPE TRANSISTOR TECHNOLOGIES: IMPACTS ON CNN ARCHITECTURES**

Indranil Palit[1], Behnam Sedighi[1], Xiaobo Sharon Hu[1], Joseph Nahas[1], Michael Niemier[1] and András Hortváth[2]
[1]University of Notre Dame, US; [2]Pázmány Péter Catholic University, HU

1230 **LUNCH BREAK** in Exhibition Area

6.3 Management of Micro/Macro Renewable Energy Storage Systems

Konferenz 1 1100 – 1230

Chair: **Geoff Merrett,** University of Southampton, GB
Co-Chair: **Davide Brunelli,** University of Trento, IT

Modern energy storage systems affect all areas of power electronics, from micro-power energy harvesting systems to mega-watt Smart Grid systems. Papers in this session address novel approaches for on-chip power electronics operating under variable Vdd, and optimisation approaches to efficient design of smart grid energy storage.

1100 **ASYNCHRONOUS DESIGN FOR NEW ON-CHIP WIDE DYNAMIC RANGE POWER ELECTRONICS**

Delong Shang[1], Xuefu Zhang[2], Fei Xia[3] and Alex Yakovlev[2]
[1]School of EEE,Newcastle University, GB; [2]School of EEE, Newcastle University, GB; [3]School of EEE, GB

1130 **REAL-TIME OPTIMIZATION OF THE BATTERY BANKS LIFETIME IN HYBRID RESIDENTIAL ELECTRICAL SYSTEMS**

Maurizio Rossi, Alessandro Toppano and Davide Brunelli, University of Trento, IT

1200 **OPTIMAL DIMENSIONING OF ACTIVE CELL BALANCING ARCHITECTURES**

Swaminathan Narayanaswamy[1], Sebastian Steinhorst[1], Martin Lukasiewycz[2], Matthias Kauer[3] and Samarjit Chakraborty[4]
[1]TUM CREATE, SG; [2]TUM CREATE Singapore, SG; [3]TUM CREATE Ltd,, SG; [4]TU Munich, DE

1215 **OPTIMAL DESIGN AND MANAGEMENT OF A SMART RESIDENTIAL PV AND ENERGY STORAGE SYSTEM**

Di Zhu[1], Yanzhi Wang[1], Naehyuck Chang[2] and Massoud Pedram[1]
[1]Univ. of Southern California, US; [2]Seoul National University, KR

IPS **IP3-1, IP3-2, IP3-3**

1230 **LUNCH BREAK** in Exhibition Area

6.4 Power delivery and distribution

Konferenz 2 1100 – 1230

Chair: **Edith Beigné,** CEA LETI Grenoble, FR
Co-Chair: **Domenik Helms,** OFFIS Oldenburg, DE

This session will present innovative solutions for power delivery in complex SoCs using configurable structures working over large condition range. Configurable DC-DC and LDOs architectures will be considered underlining power efficiency issues of off-chip and on-chip regulators. Fine-grain approaches are also proposed to deal with distributed in-die power generation reducing static and dynamic power in complex SoCs.

1100 **DESIGN AND EVALUATION OF FINE-GRAINED POWER-GATING FOR EMBEDDED MICROPROCESSORS**

Masaaki Kondo[1], Hiroaki Kobyashi[2], Ryuichi Sakamoto[2], Motoki Wada[2], Jun Tsukamoto[2], Mitaro Namiki[2], Weihan Wang[3], Hideharu Amano[3], Kensaku Matsunaga[4], Masaru Kudo[4], Kimiyoshi Usami[4], Toshiya Komoda[5] and Hiroshi Nakamura[5]
[1]The University of Electro-Communications, JP; [2]Tokyo University of Agriculture and Technology, JP; [3]Keio University, JP; [4]Shibaura Institute of Technology, JP; [5]The University of Tokyo, JP

1130 **SUPERRANGE: WIDE OPERATIONAL RANGE POWER DELIVERY DESIGN FOR BOTH STV AND NTV COMPUTING**

Xin He[1], Guihai Yan[2], Yinhe Han[3] and Xiaowei Li[3]
[1]Institue of Computing Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences, CN; [2]Institute of Computing Technology, Chinese Academy of Sciences, CN; [3]Institute of Computing Technology, Chinese Academy of Sciences, CN

1200 **MODELING AND ANALYSIS OF DIGITAL LDOS WITH ADAPTIVE CONTROL FOR HIGH EFFICIENCY UNDER WIDE DYNAMIC RANGE DIGITAL LOADS**

Samantak Gangopadhyay, Youngtak Lee, Saad Bin Nasir and Arijit Raychowdhury, Georgia Institute of Technology, US

1230 **LUNCH BREAK** in Exhibition Area

6.5 Beyond EDA: Extending the Application Domain of Formal Methods

Konferenz 3 1100 – 1230

Chair: **Christoph Scholl,** University of Freiburg, DE
Co-Chair: **Gianpiero Cabodi,** Politecnico di Torino, IT

Formal methods are traditionally used to verify the correctness or hardware, software, or protocols. This session introduces a set of applications which extend the use of formal methods into new domains. The first three papers demonstrate novel ways to bridge formal verification results into the synthesis domain. The fourth leverages formal reasoning to certify the correctness of photonic systems.

1100 **USING MAXBMC FOR PARETO-OPTIMAL CIRCUIT INITIALIZATION**

Sven Reimer, Matthias Sauer, Tobias Schubert and Bernd Becker, University of Freiburg, DE

1130 **PARTIAL WITNESSES FROM PREPROCESSED QUANTIFIED BOOLEAN FORMULAS**

Martina Seidl[1] and Robert Könighofer[2]
[1]JKU Linz, AT; [2]TU Graz, AT

1200 **EQUIVALENCE CHECKING FOR FUNCTION PIPELINING IN BEHAVIORAL SYNTHESIS**

Kecheng Hao[1], Sandip Ray[2] and Fei Xie[3]
[1]Xilinx Inc., US; [2]Strategic CAD Labs, Intel Corporation, US; [3]Portland State University, US

1215 **TOWARDS THE FORMAL ANALYSIS OF MICRORESONATORS BASED PHOTONIC SYSTEMS**

Umair Siddique[1] and Sofiene Tahar[2]
[1]Concordia University, Montreal, CA; [2]Department of Electrical and Computer Engineering, Concordia University, CA

IPS **IP3-4, IP3-5**

1230 **LUNCH BREAK** in Exhibition Area

6.6 Model-Based Design and Hardware/Software Interfaces

Konferenz 4 1100 – 1230

Chair: **Wang Wang Yi,** Uppsala University, SE
Co-Chair: **Wolfgang Nebel,** OFFIS, DE

This sessions covers multiple abstraction in embedded system design. The first paper proposes a scalable approach to refinement checking of component-based systems using contracts and local refinement assertions. The second paper revisits the paradigm of using a set of communicating asynchronous components for implementation of synchronous models. The third paper presents a hardware scheduling support for OpenMP and the fourth paper proposes an object-aware translation layer for flash memories.

1100 **LIBRARY-BASED SCALABLE REFINEMENT CHECKING FOR CONTRACT-BASED DESIGN**

Antonio Iannopollo, Pierluigi Nuzzo, Stavros Tripakis and Alberto Sangiovanni-Vincentelli, University of California, Berkeley, US

1130 **ISOCHRONOUS NETWORKS BY CONSTRUCTION**

Yu Bai and Klaus Schneider, University of Kaiserslautern, DE

1145 **TIGHTLY-COUPLED HARDWARE SUPPORT TO DYNAMIC PARALLELISM ACCELERATION IN EMBEDDED SHARED MEMORY CLUSTERS**

Paolo Burgio[1], Giuseppe Tagliavini[2], Francesco Conti[2], Andrea Marongiu[2] and Luca Benini[3]
[1]University of Bologna, Université de Bretagne-Sud, IT; [2]University of Bologna, IT; [3]Università di Bologna, IT

1200 **P-OFTL: AN OBJECT-BASED SEMANTIC-AWARE PARALLEL FLASH TRANSLATION LAYER**

Wei Wang, Youyou Lu and Jiwu Shu, Tsinghua Univiersity, CN

IPS **IP3-6, IP3-7**

1230 **LUNCH BREAK** in Exhibition Area

6.7 Hardening Approaches at Different Design Levels

Konferenz 5 1100 – 1230

Chair: **Lorena Anghel,** TIMA, FR

New solutions for the design of hardened hardware components, from circuit to processor level.

1100 **NOSTRADAMUS: LOW-COST HARDWARE-ONLY ERROR DETECTION FOR PROCESSOR CORES**

Ralph Nathan and Daniel Sorin, Duke University, US

1130 **WORD-LINE POWER SUPPLY SELECTOR FOR STABILITY IMPROVEMENT OF EMBEDDED SRAMS IN HIGH RELIABILITY APPLICATIONS**

Bartomeu Alorda, Cristian Carmona and Sebastia Bota, Balearic Islands University, ES

1200 **A HIGH PERFORMANCE SEU-TOLERANT LATCH FOR NANOSCALE CMOS TECHNOLOGY**

zhengfeng huang, Hefei University of Technology, CN

1215 **A LOW-COST RADIATION HARDENED FLIP-FLOP**

Yang Lin, Mark Zwolinski and Basel Halak, University of Southampton, GB

IPS **IP3-8, IP3-9**

1230 **LUNCH BREAK** in Exhibition Area

6.8 First Time Right in Analog Design Enabling New Business Cases

Exhibition Theatre 1100 – 1230

1230 **LUNCH BREAK** in Exhibition Area

7.0 Special Day Keynote

Saal 1 1330 – 1400

The automotive industry is in a radical change process driven by technology. On the one hand side the proliferation of communication technologies into the car leads to internet connected vehicles. The vehicle will become an integral part of the internet – opening new processing paradigms for the car itself. On the other hand the vehicle itself significantly expands its sensor and processing capabilities by the use of radar, video, ultrasound sensors and usage of state of the

art CPU and GPU processor architectures. In our talk we will address both developments and outline foreseen future applications as future driving assistant and infotainment systems as well as highly automated driving. We will discuss major requirements for the future electrical architectures and implications for future automotive chips.

1330 **SPECIAL DAY KEYNOTE: THE CONNECTED CAR AND ITS IMPLICATION TO THE AUTOMOTIVE CHIP ROADMAP**
Michael Bolle, Robert Bosch GmbH, DE

7.1 SPECIAL DAY Panel: HW/SW Co-Development - The Industrial Workflow

Saal 1 1430 – 1600

Organiser: **Johannes Stahl,** Synopsys, US
Chair: **Iris Stroh,** Markt & Technik, DE

This panel brings together the entire supply chain for the use of virtual prototyping starting with the end users at an automotive Tier1, a semiconductor supplier, IP providers and the virtual prototyping and software development tool providers. The panelists will discuss what are the benefits and challenges of accelerating software development using virtual prototyping are for deployment in industrial projects.

Panelist
Andreas Schwerin, Siemens, DE
Martin Vaupel, Bosch, DE
Albrecht Mayer, Infineon, DE
Nick Gatherer, ARM, GB
Frank Schirrmeister, Cadence, US
Stephan Lauterbach, Lauterbach, US
Colin Walls, Mentor Graphics, US
Andreas Hoffmann, Synopsys, US

1600 **COFFEE BREAK** in Exhibition Area

7.2 Embedded Tutorial: Cross Layer Resiliency in Real World

Konferenz 6 1430 – 1600

Organiser: **Vikas Chandra,** ARM, US
Chair: **Yanjing Li,** Intel, US
Co-Chair: **Ulf Schlichtmann,** TUM, DE

Resilience at different design hierarchies will be needed in Complex SoCs to handle failures due to variability, reliability and design errors (logical or electrical). The main reasons for the marginal behavior are sheer design complexity, uncertainties in manufacturing processes, temporal variability and operating conditions. In this session, we will cover the basics of cross layer resiliency and explore the reliability challenges in both embedded processors as well as large scale computing resources.

1430 **CROSS-LAYER RESILIENCE EXPLORATION AND OPTIMIZATION**
Subhasish Mitra, Stanford University, US

1500 **RELIABILITY CHALLENGES IN EMBEDDED PROCESSORS**
Vikas Chandra, ARM, US

1530 **BILLION CHIPS OF TRILLION TRANSISTORS: HOW TO MAKE THEM RELIABLE?**
Chen-Yong Cher[1] and Silvia Mueller[2]
[1]IBM Research, US; [2]IBM Boeblingen, DE

1600 **COFFEE BREAK** in Exhibition Area

7.3 Low power methods and multicore architectures for mobile health applications

Konferenz 1 1430 – 1600

Chair: **Giovanni Ansaloni,** EPFL, CH
Co-Chair: **Andrea Bartolini,** University of Bologna, IT

Achieving low power operation is essential for battery operated mobile health applications. In this session, the papers address this important issue. The first two papers present multicore architectural methods for bio-signal processing, dealing with synchronisation and innovative memory architecture design. The last two papers focus on low power design of applications for bio-signal processing: tuning of sensor usage based on applications and methods to selectively drop computations to save power, without affecting the accuracy.

1430 **HARDWARE/SOFTWARE APPROACH FOR CODE SYNCHRONIZATION IN LOW-POWER MULTI-CORE SENSOR NODES**
Rubén Braojos[1], Ahmed Dogan[2], Ivan Beretta[2], Giovanni Ansaloni[2] and David Atienza[2]
[1]École Polytechnique Fédérale de Lausanne, CH; [2]EPFL, CH

1500 **HYBRID MEMORY ARCHITECTURE FOR VOLTAGE SCALING IN ULTRA-LOW POWER MULTI-CORE BIOMEDICAL PROCESSORS**
Daniele Bortolotti[1], Andrea Bartolini[1], Christian Weis[2], Davide Rossi[1] and Luca Benini[1]
[1]University of Bologna, IT; [2]University of Kaiserslautern, DE

1530 **CONTEXT AWARE POWER MANAGEMENT FOR MOTION-SENSING BODY AREA NETWORK NODES**
Filippo Casamassima[1], Elisabetta Farella[2] and Luca Benini[3]
[1]University of Bologna, IT; [2]DEI - University of Bologna, IT; [3]Università di Bologna, IT

1545 **A QUALITY-SCALABLE AND ENERGY-EFFICIENT APPROACH FOR SPECTRAL ANALYSIS OF HEART RATE VARIABILITY**
Georgios Karakonstantis[1], Aviinaash Sankaranarayanan[2], Mohamed Sabry[1], David Atienza[1] and Andreas Burg[1]
[1]EPFL, CH; [2]Debiotech S.A., CH

1600 **COFFEE BREAK** in Exhibition Area

7.4 Runtime memory optimization and GPU/manycore architectures

Konferenz 2 1430 – 1600

Chair: **Alberto Nannarelli,** DTU Copenhagen, DK
Co-Chair: **Alberto Macii,** PoliTo Torino, IT

The session starts with memory design techniques under PVT variation and ageing for DRAMs and SRAM caches. Afterwards, bus, memory and partitioning techniques for 2D and 3D GPUs and manycores are presented.

1430 **EXPLOITING EXPENDABLE PROCESS-MARGINS IN DRAMS FOR RUN-TIME PERFORMANCE OPTIMIZATION**

Karthik Chandrasekar[1], Sven Goossens[2], Christian Weis[3], Martijn Koedam[2], Benny Akesson[4], Norbert Wehn[3] and Kees Goossens[5]
[1]Delft University of Technology, NL; [2]Eindhoven University of Technology, NL; [3]University of Kaiserslautern, DE; [4]Czech Technical University in Prague, CZ; [5]Eindhoven university of technology, NL

1500 **CACHE AGING REDUCTION WITH IMPROVED PERFORMANCE USING DYNAMICALLY RE-SIZABLE CACHE**

Haroon Mahmood, Massimo Poncino and Enrico Macii, Politecnico di Torino, IT

1515 **ON GPU BUS POWER REDUCTION WITH 3D IC TECHNOLOGIES**

Young-joon Lee[1] and Sung Kyu Lim[2]
[1]Intel Corporation, US; [2]Georgia Institute of Technology, US

1545 **PROCESS VARIATION-AWARE WORKLOAD PARTITIONING ALGORITHMS FOR GPUS SUPPORTING SPATIAL MULTITASKING**

Paula Aguilera[1], Jungseob Lee[1], Amin Farmahini Farahani[1], Michael Schulte[2], Katherine Morrow[1] and Nam Sung Kim[1]
[1]University of Wisconsin-Madison, US; [2]AMD, US

IPS **IP3-11, IP3-12, IP3-13**

1600 **COFFEE BREAK** in Exhibition Area

7.5 Emerging memory technologies

Konferenz 3 1430 – 1600

Chair: **Aida Todri,** CNRS, FR
Co-Chair: **Lars Bauer,** KIT, DE

The papers in this sessions consider ways to improve the energy, performance, and reliability of emerging memory technologies. STT-RAM and PCRAM are addressed.

1430 **ASYNCHRONOUS ASYMMETRICAL WRITE TERMINATION (AAWT) FOR A LOW POWER STT-MRAM**

Rajendra Bishnoi, Mojtaba Ebrahimi, Fabian Oboril and Mehdi Tahoori
Karlsruhe Institiute of Technology, DE

1500 **WRITE-ONCE-MEMORY-CODE PHASE CHANGE MEMORY**

Jiayin Li and Kartik Mohanram, University of Pittsburgh, US

1530 **IMPROVING STT-MRAM DENSITY THROUGH MULTI-BIT ERROR CORRECTION**

Brandon Del Bel, Jongyeon Kim, Chris H. Kim and Sachin S. Sapatnekar, University of Minnesota, US

IPS **IP3-14, IP3-15, IP3-16**

1600 **COFFEE BREAK** in Exhibition Area

7.6 Performance and timing analysis

Konferenz 4 1430 – 1600

Chair: **Wang Yi,** Uppsala University, SE
Co-Chair: **Petru Eles,** Linköping University, SE

This session includes three papers. The first uses data mining techniques to detect performance bottlenecks to improve the scalability of multicore platforms for embedded applications. The second proposes to use regular expressions for specifying the patterns of deadline misses and hits to relax schedulability analysis for cyber physical systems. The third presents an approach to the scheduling of streaming applications, considering latency constraints and minimization of the number of processors required.

1430 **SCALABILITY BOTTLENECKS DISCOVERY IN MPSOC PLATFORMS USING DATA MINING ON SIMULATION TRACES**

sofiane lagraa[1], Alexandre Termier[2] and Frédéric Pétrot[1]
[1]Grenoble institute of Technologie, FR; [2]University of Joseph Fourier, FR

1500 **COMPUTING A LANGUAGE-BASED GUARANTEE FOR TIMING PROPERTIES OF CYBER-PHYSICAL SYSTEMS**

Neil Dhruva, Pratyush Kumar, Georgia Giannopoulou and Lothar Thiele, ETH Zurich, CH

1530 **RESOURCE OPTIMIZATION FOR CSDF-MODELED STREAMING APPLICATIONS WITH LATENCY CONSTRAINTS**

Di Liu[1], Jelena Spasic[1], Jiali Teddy Zhai[1], Todor Stefanov[1] and Gang Chen[2]
[1]Leiden University, NL; [2]Technical University Munich, DE

IPS **IP3-17, IP3-18, IP3-19, IP3-20**

1600 **COFFEE BREAK** in Exhibition Area

7.7 Design-for-Test and Test Access

Konferenz 5 1430 – 1600

Chair: **Erik Jan Marinissen,** IMEC, BE
Co-Chair: **Hans-Joachim Wunderlich,** University of Stuttgart, DE

This session covers topics that blend test with fault tolerance, security, and logic placement. As the area of IC test matures the core technology is adapting to the needs of the design and its implementation. As we move forward to advanced nodes in manufacturing the need to tolerate errors could blend with test methods. Test structures provide access to key design IP which is of concern in some situations. Papers in this session address solutions in IC Test for security.

1430 **BIT-FLIPPING SCAN - A UNIFIED ARCHITECTURE FOR FAULT TOLERANCE AND OFFLINE TEST**

Michael Imhof and Hans-Joachim Wunderlich
University of Stuttgart, DE

1500 **TESTING PUF-BASED SECURE KEY STORAGE CIRCUITS**

Mafalda Cortez[1], Gijs Roelofs[1], Said Hamdioui[1] and Giorgio Di Natale[2]
[1]Delft University of Technology, NL; [2]LIRMM, FR

1530 **MAKING IT HARDER TO UNLOCK AN LSIB: HONEYTRAPS AND MISDIRECTION IN A P1687 NETWORK**

Adam Zygmontowicz[1], Jennifer Dworak[1], Al Crouch[2] and John Potter[2]
[1]Southern Methodist University, US; [2]ASSET InterTech, US

1545 **CO-OPTIMIZATION OF MEMORY BIST GROUPING, TEST SCHEDULING, AND LOGIC PLACEMENT**

Ilgweon Kang and Andrew B. Kahng, UC San Diego, US

1600 **COFFEE BREAK** in Exhibition Area

7.8 FD-SOI - the Enabling European Technology for Energy Efficient Solutions - Creating a Solution Hive & Design Hub as Eco-System for Future Success

Exhibition Theatre 1430 – 1600

1600 **COFFEE BREAK** in Exhibition Area

IP3 Interactive Presentations

Conference Level, Foyer 1600 – 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP3-1 **DESIGN AND FABRICATION OF A 315 µH BONDWIRE MICRO-TRANSFORMER FOR ULTRA-LOW VOLTAGE ENERGY HARVESTING**

Enrico Macrelli[1], Ningning Wang[2], Saibal Roy[2], Michael Hayes[2], Rudi Paolo Paganelli[3], Marco Tartagni[1] and Aldo Romani[1]
[1]DEI, University of Bologna, IT; [2]Tyndall National Institute, UCC, IE; [3]CNR-IEIIT, University of Bologna, IT

IP3-2 **PROVIDING REGULATION SERVICES AND MANAGING DATA CENTER PEAK POWER BUDGETS**

Baris Aksanli and Tajana Rosing, University of California San Diego, US

IP3-3 **THE ENERGY BENEFIT OF LEVEL-CROSSING SAMPLING INCLUDING THE ACTUATOR'S ENERGY CONSUMPTION**

Burkhard Hensel and Klaus Kabitzsch, Dresden University of Technology, DE

IP3-4 **SKETCHILOG: SKETCHING COMBINATIONAL CIRCUITS**

Andrew Becker, David Novo and Paolo Ienne, École Polytechnique Fédérale de Lausanne, CH

IP3-5 **TOWARDS VERIFYING DETERMINISM OF SYSTEMC DESIGNS**

Hoang M. Le and Rolf Drechsler, University of Bremen, DE

IP3-6 **USING GUIDED LOCAL SEARCH FOR ADAPTIVE RESOURCE RESERVATION IN LARGE-SCALE EMBEDDED SYSTEMS**

Timon ter Braak, University of Twente, NL

IP3-7 **ACCELERATING GRAPH COMPUTATION WITH RACETRACK MEMORY AND POINTER-ASSISTED GRAPH REPRESENTATION**

Eunhyek Park[1], Helen Li[2], Sungjoo Yoo[1] and Sunggu Lee[1]
[1]POSTECH, KR; [2]Univ. of Pittsburgh, US

IP3-8 **PSP-CACHE: A LOW-COST FAULT-TOLERANT CACHE MEMORY ARCHITECTURE**

Hamed Farbeh and Seyed Ghassem Miremadi, Sharif University of Technology, IR

IP3-9 **A HYBRID NON-VOLATILE SRAM CELL WITH CONCURRENT SEU DETECTION AND CORRECTION**

Pilin Junsangsri[1], Fabrizio Lombardi[1] and Jie Han[2]
[1]Northeastern University, US; [2]University of Alberta, CA

IP3-10 **BATTERY AWARE STOCHASTIC QOS BOOSTING IN MOBILE COMPUTING DEVICES**

Hao Shen, Qiuwen Chen and Qinru Qiu, Syracuse University, US

IP3-11 **A THERMAL RESILIENT INTEGRATION OF MANY-CORE MICROPROCESSORS AND MAIN MEMORY BY 2.5D TSI I/OS**

Sih-Sian Wu[1], Kanwen Wang[1], Sai Manoj P. D.[1], Tsung-Yi Ho[2] and Hao Yu[1]
[1]Nanyang Technological University, SG; [2]National Cheng Kung University, TW

IP3-12 **LEVERAGING ON-CHIP NETWORKS FOR EFFICIENT PREDICTION ON MULTICORE COHERENCE**

Libo Huang, National University of Defense Technology, CN

IP3-13 **AN ADAPTIVE MEMORY INTERFACE CONTROLLER FOR IMPROVING BANDWIDTH UTILIZATION OF HYBRID AND RECONFIGURABLE SYSTEMS**

Vito Giovanni Castellana[1], Antonino Tumeo[2] and Fabrizio Ferrandi[1]
[1]Politecnico di Milano, DEIB, IT; [2]Pacific Northwest National Laboratory, US

IP3-14 **ENERGY EFFICIENT IN-MEMORY AES ENCRYPTION BASED ON NONVOLATILE DOMAIN-WALL NANOWIRE**

Yuhao Wang[1], Pingfan Kong[1], Hao Yu[1] and Dennis Sylvester[2]
[1]Nanyang Technological University, SG; [2]University of Michigan, US

IP3-15 **ICE: INLINE CALIBRATION FOR MEMRISTOR CROSSBAR-BASED COMPUTING ENGINE**

Boxun Li[1], Yu Wang[1], Yiran Chen[2], Helen Li[2] and Huazhong Yang[1]
[1]Tsinghua University, CN; [2]University of Pittsburgh, US

IP3-16 **COMPLEMENTARY RESISTIVE SWITCH BASED STATEFUL LOGIC OPERATIONS USING MATERIAL IMPLICATION**

Yuanfan Yang[1], Jimson Mathew[1], Dhiraj K Pradhan[1], Marco Ottavi[2] and Salvatore Pontarelli[2]
[1]University of Bristol, GB; [2]University of Rome "Tor Vergata", IT

IP3-17 **A LAYERED APPROACH FOR TESTING TIMING IN THE MODEL-BASED IMPLEMENTATION**

BaekGyu Kim[1], Hyeon I Hwang[2], Taejoon Park[2], Sanghyuk Son[2] and Insup Lee[1]
[1]University of Pennsylvania, US; [2]Daegu Gyeongbuk Institute of Science & Technology, KR

IP3-18 **MODEL-BASED PROTOCOL LOG GENERATION FOR TESTING A TELECOMMUNICATION TEST HARNESS USING CLP**

Kenneth Balck[1], Olga Grinchtein[1] and Justin Pearson[2]
[1]Ericsson AB, SE; [2]Uppsala University, SE

IP3-19 **TIME-DECOUPLED PARALLEL SYSTEMC SIMULATION**

Jan Weinstock[1], Christoph Schumacher[1], Rainer Leupers[1], Gerd Ascheid[1] and Laura Tosoratto[2]
[1]RWTH Aachen, DE; [2]Istituto Nazionale di Fisica Nucleare, Sezione di Roma, IT

IP3-20 **A UNIFIED METHODOLOGY FOR A FAST BENCHMARKING OF PARALLEL ARCHITECTURE**

Alexandre Guerre, Jean-Thomas Acquaviva and Yves Lhuillier, CEA LIST, FR

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.1 SPECIAL DAY System Simulation and Virtual Prototyping

Saal 1 1700 – 1830

Organiser: **Johannes Stahl,** Synopsys, US
Chair: **Johannes Stahl,** Synopsys, US

In this session we will review several practical applications of virtual prototyping for architecture design work and software development across different markets such as mobile, industrial and automotive. The authors will share their practical experiences in using the virtual prototyping methodology and current commercial tools.

1700 **POWER MODELING AND ANALYSIS IN EARLY DESIGN PHASES**

Bernhard Fischer, Christian Cech and Hannes Muhr, Siemens, AT

1730 **SYSTEM-LEVEL DESIGN METHODOLOGY ENABLING FAST DEVELOPMENT OF BASEBAND MP-SOC FOR 4G SMALL CELL BASE STATION**

Shan Tang, Zhu Ziyuan and Yongtao su, Institute of Computing Technology, Chinese Academy of Sciences, CN

1800 **VIRTUAL PROTOTYPE LIFE CYCLE IN AUTOMOTIVE APPLICATIONS**

Manfred Thanner, Freescale, DE

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.2 Hot Topic: Near Threshold Computing (NTC)

Konferenz 6 1700 – 1830

Organiser: **Michael Huebner,** Ruhr-University Bochum, DE
Chair: **Michael Huebner,** Ruhr-University Bochum, DE

To face with the power/utilization wall, Near-Threshold Computing (NTC) has emerged as one of the most promising approach to achieve an order of magnitude improvement or more in energy efficiency of microprocessors and reconfigurable hardware. NTC takes advantage of the quadratic relation between the supply voltage (Vdd) and the dynamic power, by lowering the supply voltage of chips to a value only slightly higher than the threshold voltage.

1700 **EXTREME-SCALE COMPUTER ARCHITECTURE: ENERGY EFFICIENCY FROM THE GROUND UP**

Josep Torrellas, University of Illinois Urbana Champaign, US

1730 **VOLTAGE ISLAND MANAGEMENT IN NEAR THRESHOLD MANYCORE ARCHITECTURES TO MITIGATE DARK SILICON**

Cristina Silvano[1], Gianluca Palermo[1], Sotirios Xydis[2] and Ioannis Stamelakos[1]
[1]Politecnico di Milano, IT; [2]National Technical University of Athens, GR

1800 **RESOLVING THE MEMORY BOTTLENECK FOR SINGLE SUPPLY NEAR-THRESHOLD COMPUTING**

Tobias Gemmeke[1], Mohamed Sabry[2], Jan Stuijt[1], Praveen Raghavan[3], Francky Catthoor[3] and David Atienza[2]
[1]Holst-Centre / IMEC, NL; [2]ESL-EPFL, CH; [3]IMEC, BE

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.3 Physical Attacks and countermeasures

Konferenz 1 1700 – 1830

Chair: **Francesco Regazzoni,** Alari, CH
Co-Chair: **Shivam Bhasin,** Telecom Paristech, FR

Physical Attacks are a major security threat for embedded system applications. This session focuses on several aspects of this problem. The presented papers range from countermeasures against power analysis and fault-based attacks, including electromagnetic and laser injections.

1700 **EFFICIENCY OF A GLITCH DETECTOR AGAINST ELECTROMAGNETIC FAULT INJECTION**

Loic Zussa[1], Amine Dehbaoui[1], Karim Tobich[2], Jean-Max Dutertre[1], Philippe Maurine[2], Ludovic Guillaume-Sage[2], Jessy Clediere[3] and Assia Tria[3]
[1]ENSM-SE, FR; [2]LIRMM, FR; [3]CEA, FR

1730 **ANALYZING AND ELIMINATING THE CAUSES OF FAULT SENSITIVITY ANALYSIS**

Nahid Farhady Ghalaty, Aydin Aysu and Patrick Schaumont, Virginia Tech, US

1800 **A SMALLER AND FASTER VARIANT OF RSM**

Noritaka Yamashita, Kazuhiko Minematsu, Toshihiko Okamura and Yukiyasu Tsunoo, NEC, JP

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.4 Efficient Designs for Telecom and Financial Applications

Konferenz 2 1700 – 1830

Chair: **Sergio Saponara,** University of Pisa, IT
Co-Chair: **Amer Baghdadi,** Telecom Bretagne, FR

The session presents energy and performance efficient implementations of wireless communication and financial applications

1700 **ENERGY EFFICIENT MIMO PROCESSING: A CASE STUDY OF OPPORTUNISTIC RUN-TIME APPROXIMATIONS**

David Novo[1], Nazanin Farahpour[1], Ubaid Ahmad[2], Francky Catthoor[2] and Paolo Ienne[1]
[1]EPFL, CH; [2]IMEC, BE

1730 **ENERGY-EFFICIENT FPGA IMPLEMENTATION FOR BINOMIAL OPTION PRICING USING OPENCL**

Valentin Mena Morales[1], Pierre-Henri Horrein[1], Erik Hochapfel[2], Sandrine Vaton[3] and Amer Baghdadi[1]
[1]Institut Mines-Telecom; Telecom Bretagne; Lab-STICC, FR; [2]ADACSYS, FR; [3]Institut Mines-Telecom; Telecom Bretagne; IRISA, FR

1800 **HARDWARE IMPLEMENTATION OF A REED-SOLOMON SOFT DECODER BASED ON INFORMATION SET DECODING**

Stefan Scholl and Norbert Wehn, TU Kaiserslautern, DE

1815 **AMBIENT VARIATION-TOLERANT AND INTER COMPONENTS AWARE THERMAL MANAGEMENT FOR MOBILE SYSTEM ON CHIPS**

Francesco Paterna[1], Joe Zanotelli[2] and Tajana Rosing[1]
[1]University of California, San Diego, US; [2]Qualcomm Inc., US

IPS **IP4-2, IP4-3**

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.5 Modeling & Specification

Konferenz 3 1700 – 1830

Chair: **Wolfgang Mueller,** University of Paderborn, DE
Co-Chair: **Francois PECHEUX,** UPMC, FR

The first presentation proposes an analytical model to estimate the contention and the resulting delays on accessing shared components in a multi-core environment. In order to find the right granularity for design space exploration, the second presentation provides an algorithm for automatic aggregation of design blocks based upon their static computation demands. Finally, the last presentation proposes a novel formal notation for reactive system requirements in order to reduce translational efforts and thus make specifications both easier and quicker to create.

1700 **AN ACTIVITY-SENSITIVE CONTENTION DELAY MODEL FOR HIGHLY EFFICIENT DETERMINISTIC FULL-SYSTEM SIMULATIONS**

Shu-Yung Chen, Chien-Hao Chen and Ren-Song Tsay, The Department of Computer Science National Tsing Hua University, Taiwan, TW

1730 **AUTOMATIC SPECIFICATION GRANULARITY TUNING FOR DESIGN SPACE EXPLORATION**

Jiaxing Zhang and Gunar Schirner, Northeastern University, US

1800 **EDT: A SPECIFICATION NOTATION FOR REACTIVE SYSTEMS**

Murali Krishna Goldsmith, Venkatesh R, Ulka Shrotri and Supriya Agrawal, Tata Research Development and Design Centre, Tata Consultancy Services Limited, IN

IPS **IP4-4, IP4-5, IP4-6**

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.6 Mapping and Scheduling for Many-Core Embedded Systems

Konferenz 4 1700 – 1830

Chair: **Marc Geilen,** Eindhoven University of Technology, NL
Co-Chair: **Sébastien Le Beux,** Ecole Centrale de Lyon, FR

This session discusses novel ideas for embedded software implementation on many-core architectures. The first presentation deals with an optimized implementation of a H265 video coding algorithm on many-core architectures. A run-time scheduling approach for GPGPU architectures for priority-based systems is presented in the second presentation. The third talk presents an efficient run-time resource manager heuristic for many-core architectures based on a Lagrangian relaxation technique.

1700 **SOFTWARE ARCHITECTURE OF HIGH EFFICIENCY VIDEO CODING FOR MANY-CORE SYSTEMS WITH POWER-EFFICIENT WORKLOAD BALANCING**

Muhammad Usman Karim Khan, Muhammad Shafique and Jörg Henkel, Karlsruhe Institute of Technology (KIT), DE

1730 **GPU-EVR: RUN-TIME EVENT BASED REAL-TIME SCHEDULING FRAMEWORK ON GPGPU PLATFORM**

Haeseung Lee and Mohammad Abdullah Al Faruque University of California, Irvine, US

1800 **MULTI-OBJECTIVE DISTRIBUTED RUN-TIME RESOURCE MANAGEMENT FOR MANY-CORES**

Stefan Wildermann, Michael Glaß and Jürgen Teich
University of Erlangen-Nuremberg, DE

IPS **IP4-7, IP4-8, IP4-9, IP4-10**

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.7 Performance Modeling and Delay Test

Konferenz 5 1700 – 1830

Chair: **Robert Aitken,** ARM, US
Co-Chair: **Mehdi Tahoori,** KIT, DE

As technology dimensions shrink and process complexity increases, it becomes vital to accurately model performance limiters such as device and metal variability, as well as to determine when these effects become so critical that delay requirements are exceeded.

1700 **EFFICIENT PERFORMANCE ESTIMATION WITH VERY SMALL SAMPLE SIZE VIA PHYSICAL SUBSPACE PROJECTION AND MAXIMUM A POSTERIORI ESTIMATION**

Li Yu[1], Sharad Saxena[2], Christopher Hess[2], Ibrahim (Abe) Elfadel[3], Dimitri Antoniadis[4] and Duane Boning[4]
[1]Massachusetts Institute of Technology, US; [2]PDF Solution, Inc, US; [3]Masdar Institute of Science and Technology, AE; [4]MIT, US

1730 **JOINT VIRTUAL PROBE: JOINT EXPLORATION OF MULTIPLE TEST ITEMS' SPATIAL PATTERNS FOR EFFICIENT SILICON CHARACTERIZATION AND TEST PREDICTION**

Shuangyue Zhang[1], Fan Lin[2], Chun-Kai Hsu[2], Kwang-Ting Cheng[2] and Hong Wang[1]
[1]Department of Automation, Tsinghua University, CN; [2]Department of Electrical and Computer Engineering, University of California, Santa Barbara, US

1800 **SUBSTITUTING TRANSITION FAULTS WITH PATH DELAY FAULTS AS A BASIC DELAY FAULT MODEL**

Irith Pomeranz, Purdue University, US

1815 **STANDARD CELL LIBRARY TUNING FOR VARIABILITY TOLERANT DESIGNS**

Sebastien Fabrie[1], Juan Diego Echeverri[2], Maarten Vertregt[2] and Jose Pineda[2]
[1]Eindhoven University of Technology, NL; [2]NXP Semiconductors, NL

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

8.8 Hot Topic: Beyond CMOS Ultra-low-power Computing

Exhibition Theatre 1700 – 1830

Organiser: **Saibal Mukhopadhyay,** Georgia Institute of Technology, US
Chair: **Arijit Raychowdhury,** Georgia Institute of Technology, US
Co-Chair: **Saibal Mukhopadhyay,** Georgia Institute of Technology, US

With conventional CMOS scaling becoming increasingly challenging, the designers wonder what opportunities and challenges exist beyond-CMOS for both Boolean and non-Boolean computing. This session will discuss three very different and promising emerging technologies -- Tunneling Field-Effect Transistor, Spintronics, and nano-electro-mechanical switches (NEMS) -- for low-power electronics. The talks will discuss the need for innovating and evaluating new circuit and system design methods as new device technologies emerge.

1700 **ULTRA-LOW POWER ELECTRONICS WITH SI/GE TUNNEL FET**

Amit Trivedi, Mohammad Faisal Amir and Saibal Mukhopadhyay, Georgia Institute of Technology, US

1730 **BRAIN-INSPIRED COMPUTING WITH SPIN TORQUE DEVICES**

Kaushik Roy, Mrigank Sharad, Deliang Fan and Karthik Yogendra, Purdue University, US

1800 **TOWARD ULTRALOW-POWER COMPUTING AT EXTEME WITH SILICON CARBIDE (SIC) NANOELECTROMECHANICAL LOGIC**

Swarup Bhunia, Vaishnavi Ranganathan, Tina He, Srihari Rajgopal, Rui Wang, Mehran Mehregany and Philip Feng
Case Western Reserve University, US

1930 **DATE PARTY** in "Gläserne Manufaktur" of the Volkswagen AG

special day more-than-moore

THURSDAY 27 MARCH, 2014

9.1 SPECIAL DAY Hot Topic: CMOS scaling - from evolutionary to revolutionary computing

Saal 1 0830 – 1000

Organisers: **Thomas Mikolajick,** NamLab gGmbH, DE
Ian O'Connor, Lyon Institute of Nanotechnology, FR
Chair: **Thomas Mikolajick,** NamLab gGmbH, DE
Co-Chair: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR

Transistors as switches have now scaled down to a point where the classical bulk structure is no longer tenable and it is necessary to change the nature of the channel structure. In this session, the three principal contenders for following on from conventional devices will be examined. The first paper looks at the use of III-V nanowires, with expected benefits in terms of speed and energy, as well as integration challenges. The second paper looks at how the use of switches with controllable polarity, such as in silicon nanowire devices, can improve the energy efficiency of systems on chip. The devices themselves are explored in detail in the third paper, with the concept of fine-grain reconfigurability at the fore. The fourth and final paper gives a reality check on carbon electronics and the most promising devices in this class.

0830 **III-V SEMICONDUCTOR NANOWIRES FOR FUTURE DEVICES**

H. Schmid, B. Borg, K. Moselund, P. Das Kunungo, G. Signorello, S. Karg, P. Mensch, V. Schmidt and H. Riel, IBM Research, CH

0850 **ADVANCED SYSTEM ON A CHIP DESIGN BASED ON CONTROLLABLE-POLARITY FETS**

Pierre-Emmanuel Gaillardon, Luca Amaru, Jian Zhang and Giovanni De Micheli, Integrated Systems Laboratory – Swiss Federal Institute of Technology, CH

0915 **RECONFIGURABLE SILICON NANOWIRE DEVICES AND CIRCUITS: OPPORTUNITIES AND CHALLENGES**

Walter Weber[1], André Heinzig[2], Jens Trommer[1], Markus König[2], Matthias Grube[1] and Thomas Mikolajick[1]
[1]Namlab gGmbH, DE; [2]TU Dresden, DE

0935 **ADVANCING CMOS WITH CARBON ELECTRONICS**

Franz Kreupl, TU Munich, DE

1000 **COFFEE BREAK** in Exhibition Area

9.2 Low-Cost, High-Performance NoCs

Konferenz 6 0830 – 1000

Chair: **Kees Goossens,** Eindhoven University, NL
Co-Chair: **Luca Ramini,** University of Ferrara, IT

This session pushes the boundaries of NoC performance optimization while at the same time accounting for implementation constraints. The first paper takes a perspective where express channels are added to the topology, and then smart application mapping is performed. The second paper instead chooses the TDM NoC route to provide guaranteed performance, and significantly optimizes the TDM scheduling process. Finally, the last paper reduces buffer sizes, while also providing elasticity, in a router's virtual channel buffers.

0830 **APPLICATION MAPPING FOR EXPRESS CHANNEL-BASED NETWORKS-ON-CHIP**

Di Zhu, Lizhong Chen, Siyu Yue and Massoud Pedram University of Southern California, US

0900 **PARALLEL PROBE BASED DYNAMIC CONNECTION SETUP IN TDM NOCS**

Shaoteng Liu, Axel Jantsch and Zhonghai Lu, KTH, SE

0930 **ELASTISTORE: AN ELASTIC BUFFER ARCHITECTURE FOR NETWORK-ON-CHIP ROUTERS**

Giorgos Dimitrakopoulos[1], Ioannis Seitanidis[1], Anastasios Psarras[1] and Chrysostomos Nicopoulos[2]
[1]Democritus University of Thrace, GR; [2]University of Cyprus, CY

IPS **IP4-12, IP4-13**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.3 Hardware Implementations for Data Security

Konferenz 1 0830 – 1000

Chair: **Viktor Fischer,** St Etienne, FR
Co-Chair: **Tim Gueneysu,** RUB, DE

Hardware features are used as a trust anchor in many secure systems. This includes design obfuscation techniques, encrypted processing, and biometric systems which are discussed in this session.

0830 **EMBEDDED RECONFIGURABLE LOGIC FOR ASIC DESIGN OBFUSCATION AGAINST SUPPLY CHAIN ATTACKS**

Bao Liu[1] and Brandon Wang[2]
[1]University of Texas San Antonio, US; [2]Cadence Design Systems, Inc., US

0900 **A MINIMALIST APPROACH TO REMOTE ATTESTATION**

Aurélien Francillon[1], Quan Nguyen[2], Kasper Rasmussen[2] and Gene Tsudik[2]
[1]EURECOM, FR; [2]University of California, Irvine, US

THURSDAY

0915 **MULTI RESOLUTION TOUCH PANEL WITH BUILT-IN FINGERPRINT SENSING SUPPORT**

Pranav Koundinya, Sandhya Theril, Tao Feng, Varun Prakash, Jimming Bao and Weidong Shi, University of Houston, US

0930 **HEROIC: HOMOMORPHICALLY ENCRYPTED ONE INSTRUCTION COMPUTER**

Nektarios Georgios Tsoutsos[1] and Michail Maniatakos[2]
[1]NYU Polytechnic School of Engineering, US; [2]NYU Abu Dhabi, AE

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.4 Timing challenges in validation

Konferenz 2 0830 – 1000

Chair: **Elena Ioana Vatajelu,** Politecnico di Torino, IT
Co-Chair: **Mark Zwolinski,** University of Southampton, GB

Accelerated timing simulation is essential for today's chip designs, whether it is performed at the gate-level or at the system-level. This session provides solutions to address the challenges of timing analysis and timing validation performance across multiple levels of design's abstractions.

0830 **FAST STA PREDICTION-BASED GATE-LEVEL TIMING SIMULATION**

Tariq Bashir Ahmad and Maciej Ciesielski, UMASS Amherst, US

0900 **A CROSS-LEVEL VERIFICATION METHODOLOGY FOR DIGITAL IPS AUGMENTED WITH EMBEDDED TIMING MONITORS**

Valerio Guarnieri[1], Massimo Petricca[2], Alessandro Sassone[2], Sara Vinco[1], Nicola Bombieri[1], Franco Fummi[3], Enrico Macii[2] and Massimo Poncino[2]
[1]University of Verona, IT; [2]Politecnico di Torino, IT; [3]Universita' di Verona, IT

0930 **EMPOWERING STUDY OF DELAY BOUND TIGHTNESS WITH SIMULATED ANNEALING**

Xueqian Zhao and Zhonghai Lu, KTH Royal Institute of Technology, SE

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.5 Hot Topic: Connecting Different Worlds – Technology Abstraction for Reliability-Aware Design and Test

Konferenz 3 0830 – 1000

Organisers: **Ulf Schlichtmann,** Technische Universität München, DE
Andreas Herkersdorf, Technische Universität München, DE
Chair: **Nikil Dutt,** University of California, Irvine, US
Co-Chair: **Mehdi Tahoori,** Karlsruhe Institute of Technology, DE

The rapid shrinking of device geometries in the nanometer regime requires new technology-aware design methodologies. These must be able to evaluate the resilience of the circuit throughout all System on Chip (SoC) abstraction levels. To successfully guide design decisions at the system level, reliability models, which abstract technology information, are required to identify those parts of the system where additional protection in the form of hardware or software countermeasures is most effective. Interfaces such as the presented Resilience Articulation Point (RAP) or the Reliability Interchange Information Format (RIIF) are required to enable EDA-assisted analysis and propagation of reliability information. The models are discussed from different perspectives, such as design and test.

0830 **INTRODUCTION TO RAP (RESILIENCE ARTICULATION POINT)**

Andreas Herkersdorf, TU München, DE

0845 **SYSTEM LEVEL DESIGN USING RAP (RESILIENCE ARTICULATION POINT)**

Ulf Schlichtmann, Technische Universität München, DE

0900 **CROSS-LAYER RELIABILITY IN THE DESIGN OF AN ERROR RESILIENT COMMUNICATION SYSTEM**

Norbert Wehn, University of Kaiserslautern, DE

0915 **RIIF - TOWARD A STANDARD APPROACH FOR CREATING RELIABILITY MODELS FOR COMPLEX SILICON DEVICES**

Adrian Evans, IROC Technologies, FR

0930 **TEST PERSPECTIVES**

Jacob Abraham, UT Austin, US

0945 **INDUSTRIAL PERSPECTIVE**

Sani Nassif, IBM, US

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.6 Schedulability analysis

Konferenz 4 0830 – 1000

Chair: **Giuseppe Lipari,** ENS - Cachan, FR
Co-Chair: **Benny Akesson,** CTU Prague, CZ

This session deals with scheduling and schedulability analysis of real-time systems. In particular, it presents different models of scheduling, including fixed and dynamic priority, and real-time calculus.

0830 **RATE-ADAPTIVE TASKS: MODEL, ANALYSIS, AND DESIGN ISSUES**

Giorgio Buttazzo[1], Enrico Bini[2] and Darren Buttle[3]
[1]Scuola Superiore Sant'Anna, IT; [2]Lund University, SE; [3]ETAS-PGA/PRM-E, DE

0900 **ACCEPTANCE AND RANDOM GENERATION OF EVENT SEQUENCES UNDER REAL TIME CALCULUS CONSTRAINTS**

Kajori Banerjee and Pallab Dasgupta, Indian Institute of Technology Kharagpur, IN

0930 **GENERAL AND EFFICIENT RESPONSE TIME ANALYSIS FOR EDF SCHEDULING**

Nan Guan and Wang Yi, Uppsala University, SE

0945 **THE SCHEDULABILITY REGION OF TWO-LEVEL MIXED-CRITICALITY SYSTEMS BASED ON EDF-VD**

Dirk Mueller and Alejandro Masrur, TU Chemnitz, DE

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.7 Timing Analysis and Cell Design

Konferenz 5 0830 – 1000

Chair: **Jose Monteiro,** INESC-ID / Tecnico, University of Lisboa, PT
Co-Chair: **Elena Dubrova,** Royal Institute of Technology, SE

The papers in this session present static timing techniques and tools for the analysis and synthesis of logic circuits. The papers take into account new aspects of timing analysis like variability, leakage and sign-off.

0830 **FACILITATING TIMING DEBUG BY LOGIC PATH CORRESPONDENCE**

Oshri Adler, Eli Arbel, Ilia Averbouch, Ilan Beer and Inna Grijnevitch, IBM, IL

0900 **STATISTICAL STATIC TIMING ANALYSIS USING A SKEW-NORMAL CANONICAL DELAY MODEL**

Vijaykumar M and V Vasudevan, Department of Electrical Engineering Indian Institute of Technology Madras, IN

0930 **LEAKAGE-POWER-AWARE CLOCK PERIOD MINIMIZATION**

Hua-Hsin Yeh[1], Shih-Hsu Huang[1] and Yow-Tyng Nieh[2]
[1]Chung Yuan Christian University, TW; [2]Industrial Technology Research Institute, TW

0945 **A DEEP LEARNING METHODOLOGY TO PROLIFERATE GOLDEN SIGNOFF TIMING**

Seung-Soo Han[1], Andrew B. Kahng[2], Siddhartha Nath[2] and Ashok S. Vydyanathan[2]
[1]Myongji University, Yongin, KR; [2]University of California, San Diego, US

IPS **IP4-17, IP4-18, IP4-19**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.8 Embedded Tutorial: Memcomputing: the Cape of Good Hope

Exhibition Theatre 0830 – 1000

Organisers: **Yiyu Shi,** Missouri University of Science & Technology, US
Hung-Ming Chen, National Chiao Tung University, TW
Chair: **Tsung-Yi Ho,** CSIE, NCKU, TW
Co-Chair: **Hung-Ming Chen,** National Chiao Tung University, TW

Energy efficiency has emerged as a major barrier to performance scalability for modern processors. On the other hand, significant breakthroughs have been achieved in memory technologies recently. As such, the fascinating idea of memcomputing (i.e., use memory for computation purposes) has drawn wide attention from both academia and industry as an effective remedy. Compared with conventional logic computing, memory array provides large set of parallel resources with high bandwidth, which can be configured to perform computing in spatial/temporal manner leading to dramatic reduction in processor-memory traffic. Moreover, memory computing brings the computing engine close to the data, thus drastically minimizing the von Neumann bottleneck. Finally, it exploits the advances in memory technologies and integration approaches (e.g. 3D integration) to achieve better technology scalability. This special session offers a broad-spectrum retreat (devices, processes and systems) on this hot topic to the general CAD community, hoping to inspire more contributions from the design automation perspective.

0830 **MEMCOMPUTING: A BRAIN-INSPIRED COMPUTING PARADIGM**

Yuriy Pershin, University of South Carolina, US

0900 **MSIM: A GENERAL CYCLE ACCURATE SIMULATION PLATFORM FOR MEMCOMPUTING STUDIES**

Chun Zhang[1], Peng Deng[2], Hui Geng[1], Jianming Liu[1], Qi Zhu[2], Jinjun Xiong[3] and Yiyu Shi[1]
[1]Missouri University of Science and Technology, US; [2]University of California, Riverside, US; [3]IBM T.J. Watson Research Center, US

0930 **ENERGY-EFFICIENT HARDWARE ACCELERATION THROUGH COMPUTING IN THE MEMORY**

Somnath Paul[1], Robert Karam[2], Swarup Bhunia[2] and Ruchir Puri[3]
[1]Intel Corporation, US; [2]Case Western Reserve University, US; [3]IBM Watson Research Center, US

1000 **COFFEE BREAK IN EXHIBITION AREA**

IP4 Interactive Presentations

Conference Level, Foyer 1000 – 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP4-1 **A MULTIPLE FAULT INJECTION METHODOLOGY BASED ON CONE PARTITIONING TOWARDS RTL MODELING OF LASER ATTACKS**

Athanasios Papadimitriou[1], David Hely[1], Vincent Beroulle[1], Paolo Maistri[2] and Regis Leveugle[3]
[1]LCIS Laboratory - Grenoble INP, FR; [2]TIMA Laboratory / CNRS, FR; [3]TIMA Laboratory / Grenoble INP, FR

IP4-2 **ENERGY EFFICIENT DATA FLOW TRANSFORMATION FOR GIVENS ROTATION BASED QR DECOMPOSITION**

Namita Sharma[1], Preeti Ranjan Panda[1], Min Li[2], Prashant Agrawal[2] and Francky Catthoor[2]
[1]Indian Institute of Technology Delhi, IN; [2]IMEC, BE

IP4-3 **MODE-CONTROLLED DATAFLOW BASED MODELING & ANALYSIS OF A 4G-LTE RECEIVER**

Hrishikesh Salunkhe[1], Orlando Moreira[2] and Kees van Berkel[1]
[1]TU Eindhoven, NL; [2]ST-Ericsson, NL

IP4-4 **MODEL-BASED ACTOR MULTIPLEXING WITH APPLICATION TO COMPLEX COMMUNICATION PROTOCOLS**

Christian Zebelein[1], Christian Haubelt[1], Joachim Falk[2], Tobias Schwarzer[2] and Jürgen Teich[2]
[1]University of Rostock, DE; [2]University of Erlangen-Nuremberg, DE

IP4-5 **A NOVEL MODEL FOR SYSTEM-LEVEL DECISION MAKING WITH COMBINED ASP AND SMT SOLVING**

Alexander Biewer[1], Jens Gladigau[1] and Christian Haubelt[2]
[1]Robert Bosch GmbH, DE; [2]University of Rostock, DE

IP4-6 **DESPERATE: SPEEDING-UP DESIGN SPACE EXPLORATION BY USING PREDICTIVE SIMULATION SCHEDULING**

Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano, Politecnico di Milano, IT

IP4-7 **COMIK: A PREDICTABLE AND CYCLE-ACCURATELY COMPOSABLE REAL-TIME MICROKERNEL**

Andrew Nelson[1], Ashkan Beyranvand Nejad[1], Anca Molnos[2], Martijn Koedam[3] and Kees Goossens[3]
[1]TU Delft, NL; [2]CEA Leti, FR; [3]TU Eindhoven, NL

IP4-8 **UTILIZATION-AWARE LOAD BALANCING FOR THE ENERGY EFFICIENT OPERATION ON THE BIG.LITTLE PROCESSOR**

Myungsun Kim[1], KIBEOM KIM[2], James Geraci[1] and Seongsoo Hong[3]
[1]Samsung Electronics, KR; [2]SAMSUNG Electronics, KR; [3]Seoul National University, KR

IP4-9 **HEVCDTM: APPLICATION-DRIVEN DYNAMIC THERMAL MANAGEMENT FOR HIGH EFFICIENCY VIDEO CODING**

Daniel Palomino[1], Muhammad Shafique[2], Hussam Amrouch[2], Altamiro Susin[3] and Jörg Henkel[2]
[1]Karlsruhe Institute of Technology (KIT), BR; [2]Karlsruhe Institute of Technology (KIT), DE; [3]Federal University of Rio Grande do Sul, BR

IP4-10 **IMPROVING EFFICIENCY OF EXTENSIBLE PROCESSORS BY USING APPROXIMATE CUSTOM INSTRUCTIONS**

Mehdi Kamal[1], Amin Ghasem Azar[1], Ali Afzali-Kusha[1] and Massoud Pedram[2]
[1]University of Tehran, IR; [2]University of Southern California, US

IP4-11 **PROBABILISTIC STANDARD CELL MODELING CONSIDERING NON-GAUSSIAN PARAMETERS AND CORRELATIONS**

André Lange[1], Christoph Sohrmann[1], Roland Jancke[1], Joachim Haase[1], Ingolf Lorenz[2] and Ulf Schlichtmann[3]
[1]Fraunhofer Institute for Integrated Circuits (IIS), Design Automation Division (EAS), DE; [2]GLOBALFOUNDRIES Inc., DE; [3]Technische Universität München, DE

IP4-12 **DYNAMIC CONSTRUCTION OF CIRCUITS FOR REACTIVE TRAFFIC IN HOMOGENEOUS CMPS**

Marta Ortín-Obón[1], Darío Suárez-Gracia Suárez-Gracia[1], María Villaroya-Gaudó[1], Cruz Izu[2] and Víctor Viñals-Yúfera[1]
[1]University of Zaragoza, ES; [2]University of Adelaide, AU

IP4-13 **IMPROVING HAMILTONIAN-BASED ROUTING METHODS FOR ON-CHIP NETWORKS: A TURN MODEL APPROACH**

Poona Bahrebar and Dirk Stroobandt, Ghent University, BE

IP4-14 **EDA TOOLS TRUST EVALUATION THROUGH SECURITY PROPERTY PROOFS**

Yier Jin, The University of Central Florida, US

IP4-15 **ANALYSIS AND EVALUATION OF PER-FLOW DELAY BOUND FOR MULTIPLEXING MODELS**

Yanchen Long[1], Zhonghai Lu[2] and Xiaolang Yan[3]
[1]Zhejiang University and KTH Royal Institute of Technology, SE; [2]KTH Royal Institute of Technology, SE; [3]Zhejiang University, CN

IP4-17 **AGING-AWARE STANDARD CELL LIBRARY DESIGN**

Saman Kiamehr[1], Farshad Firouzi[1], Mojtaba Ebrahimi[2] and Mehdi Tahoori[2]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]Karlsruhe Institute of Technology, DE

IP4-18 **PASS-XNOR LOGIC: A NEW LOGIC STYLE FOR P-N JUNCTION BASED GRAPHENE CIRCUITS**

Valerio Tenace, Andrea Calimera, Enrico Macii and Massimo Poncino, Politecnico di Torino, IT

IP4-19 **MIXED ALLOCATION OF ADJUSTABLE DELAY BUFFERS COMBINED WITH BUFFER SIZING IN CLOCK TREE SYNTHESIS OF MULTIPLE POWER MODE DESIGNS**

Kitae Park, Geunho Kim and Taewhan Kim, Seoul National University, KR

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

1230 **LUNCH BREAK** in Exhibition Area

10.1 SPECIAL DAY Hot Topic: Memories today and tomorrow

Saal 1 1100 – 1230

Organisers: **Thomas Mikolajick,** NamLab gGmbH, DE
Ian O'Connor, Lyon Institute of Nanotechnology, FR
Chair: **Tahoori Mehdi,** Karlsruhe Institute of Technology, DE
Co-Chair: **Thomas Mikolajick,** NamLab gGmbH, DE

Memory devices and technologies have undergone huge transformations in recent years and many industrially viable replacements to conventional technologies are on the brink of entering the market. The first paper in this session gives an overview of alternative memory technologies and how each can contribute or disrupt accepted memory hierarchies. The quest for a universal memory device is still underway, and the other papers in this session focus on various approaches for future memory devices. The second paper examines phase change memories, while magnetic memories are discussed in the third paper, both in terms of standard memory applications but also in terms of how they can improve logic performance. Resistive memories are the topic of the fourth paper, where new applications are considered – in FPGAs, NoCs and crossbars. The fifth paper in this session looks at low-cost memory with a printable manufacturing approach, leading to other applications and market segments.

1100 **SEMICONDUCTOR MEMORY PERSPECTIVE**

Roberto Bez, Micron, IT

1120 **EXPLORING THE LIMITS OF PHASE CHANGE MEMORIES**

Matthias Wuttig, RWTH Aachen University of Technology, DE

1135 **MAGNETIC MEMORIES: FROM DRAM REPLACEMENT TO ULTRA LOW POWER LOGIC CHIPS**

Jean-Pierre Nozières, Spintec, FR

1155 **RESISTIVE MEMORIES: WHICH APPLICATIONS?**

Fabien Clermidy[1], Natalija Jovanovic[1], Santhosh Onkaraiah[1], Houcine Oucheikh[1], Ogun Turkyilmaz[1], Olivier Thomas[1], Elisa Vianello[1], Jean-Michel Portal[2] and Marc Bocquet[2]
[1]CEA-LETI, FR; [2]Université d'Aix-Marseille, FR

1210 **THINFILM PRINTED FERRO-ELECTRIC MEMORIES AND INTEGRATED PRODUCTS**

Christer Karlsson and Peter Fischer, Thin Film Electronics AB, SE

1230 **LUNCH BREAK** in Exhibition Area

10.2 Wireless NoCs

Konferenz 6 1100 – 1230

Chair: **Giorgos Dimitrakopoulos,** Democritus University of Thrace, GR
Co-Chair: **Valeria Bertacco,** University of Michigan, US

This session comprises three papers devoted to studying different aspects of wireless NoC design and optimization. The first paper focuses on energy efficiency, by effectively tuning the transmission power of on-chip antennas. The second paper compares the performance and power of different routing algorithms for wireless NoCs, while the third paper explores the adoption of wireless NoCs in 3D chip designs.

1100 **AN ADAPTIVE TRANSMITTING POWER TECHNIQUE FOR ENERGY EFFICIENT MM-WAVE WIRELESS NOCS**

Andrea Mineo[1], Maurizio Palesi[2], Giuseppe Ascia[1] and Vincenzo Catania[1]
[1]University of Catania, IT; [2]Kore University, IT

1130 **PERFORMANCE EVALUATION OF WIRELESS NOCS IN PRESENCE OF IRREGULAR NETWORK ROUTING STRATEGIES**

Paul Wettin, Jacob Murray, Ryan Kim, Xinmin Yu, Partha Pande and Deukhyoun Heo, Washington State University, US

1200 **LOW-LATENCY WIRELESS 3D NOCS VIA RANDOMIZED SHORTCUT CHIPS**

Hiroki Matsutani[1], Michihiro Koibuchi[2], Ikki Fujiwara[2], Takahiro Kagami[1], Yasuhiro Take[1], Tadahiro Kuroda[1], Paul Bogdan[3], Radu Marculescu[4] and Hideharu Amano[1]
[1]Keio University, JP; [2]National Institute of Informatics, JP; [3]University of Southern California, US; [4]Carnegie Mellon University, US

IPS **IP5-1, IP5-2**

1230 **LUNCH BREAK** in Exhibition Area

10.3 Green Computing Systems

Konferenz 1 1100 – 1230

Chair: **Ayse Coskun,** Boston University, US
Co-Chair: **Martino Ruggiero,** University of Bologna, IT

This session discusses techniques to improve energy efficiency in large-scale computing systems, many-core systems, servers, and the cloud. The papers in this session particularly emphasize the practical experiences in academia and in industry.

1100 **GLOBAL FAN SPEED CONTROL CONSIDERING NON-IDEAL TEMPERATURE MEASUREMENTS IN ENTERPRISE SERVERS**

Jungsoo Kim[1], Mohamed M. Sabry[2], David Atienza[1], Kalyan Vaidyanathan[3] and Kenny Gross[3]
[1]EPFL, CH; [2]ESL-EPFL, CH; [3]Physical Sciences Research Center, Oracle, US

1130 **UNVEILING EURORA - THERMAL AND POWER CHARACTERIZATION OF THE MOST ENERGY-EFFICIENT SUPERCOMPUTER IN THE WORLD**

Andrea Bartolini[1], Matteo Cacciari[1], Carlo Cavazzoni[2], Giampietro Tecchiolli[3] and Luca Benini[4]
[1]University of Bologna, IT; [2]CINECA, IT; [3]EUROTECH, IT; [4]Università di Bologna, IT

1200 **CONTENTION AWARE FREQUENCY SCALING ON CMPS WITH GUARANTEED QUALITY OF SERVICE**

Hao Shen and Qinru Qiu, Syracuse University, US

1215 **CONCURRENT PLACEMENT, CAPACITY PROVISIONING, AND REQUEST FLOW CONTROL FOR A DISTRIBUTED CLOUD INFRASTRUCTURE**

Shuang Chen, Yanzhi Wang and Massoud Pedram, University of Southern California, US

IPS **IP5-3, IP5-4**

1230 **LUNCH BREAK** in Exhibition Area

10.4 System-level evaluation

Konferenz 2 1100 – 1230

Chair: **Pablo Sanchez,** University of Cantabria, ES
Co-Chair: **Florian Letombe,** Synopsys, FR

The session presents system-level verification and simulation techniques, as well as specific solutions for particular system components. The first paper analyzes how to detect concurrency errors from multi-threaded software on a virtual platform. The second one proposes a hybrid simulation platform for cache configuration analysis. The last paper explores SSD verification challenges. The session is completed by three IPs that introduce novel approaches for parallel simulation and efficient NoC/Smart systems validation.

1100 **AUTOMATIC DETECTION OF CONCURRENCY BUGS THROUGH EVENT ORDERING CONSTRAINTS**

Luis Gabriel Murillo, Simon Wawroschek, Jeronimo Castrillon, Rainer Leupers and Gerd Ascheid, RWTH Aachen University, DE

1130 **HARDWARE-BASED FAST EXPLORATION OF CACHE HIERARCHIES IN APPLICATION SPECIFIC MPSOCS**

Isuru Nawinne, Josef Schneider, Haris Javaid and Sri Parameswaran, The University of New South Wales, AU

1200 **SSDEXPLORER: A VIRTUAL PLATFORM FOR FINE-GRAINED DESIGN SPACE EXPLORATION OF SOLID STATE DRIVES**

Lorenzo Zuolo[1], Cristian Zambelli[1], Rino Micheloni[2], Salvatore Galfano[3], Marco Indaco[3], Stefano Di Carlo[3], Paolo Prinetto[3], Pirero Olivo[1] and Davide Bertozzi[1]
[1]Università degli Studi di Ferrara, IT; [2]PMC-Sierra, IT; [3]Politecnico di Torino, IT

IPS **IP5-5, IP5-6**

1230 **LUNCH BREAK** in Exhibition Area

10.5 Analysis of Components and Systems

Konferenz 3 1100 – 1230

Chair: **Frank Oppenheimer,** OFFIS, DE
Co-Chair: **Todor Stefanov,** Leiden University, NL

The first paper proposes a new static analysis approach based on segment graphs that identifies a tight set of potential access conflicts in segments that may-happen-in-parallel in system-level models. In the second paper, a technique for latency analysis for shared resource systems is introduced. The third paper proposes a method that improves the tradeoff between simulation speed and accuracy of performance models of architectures. Finally, the fourth paper deals with cross-correlating specification and RTL to discover versioning issues, poor documentation, and mismatches between specification and RTL.

1100 **MAY-HAPPEN-IN-PARALLEL ANALYSIS BASED ON SEGMENT GRAPHS FOR SAFE ESL MODELS**

Weiwei Chen[1], Xu Han[2] and Rainer Doemer[3]
[1]University of California, Irvine, US; [2]Qualcomm Inc., US; [3]EECS, UC Irvine, US

1130 **TIMING ANALYSIS OF FIRST-COME FIRST-SERVED SCHEDULED INTERVAL-TIMED DIRECTED ACYCLIC GRAPHS**

Raymond Frijns[1], Shreya Adyanthaya[1], Sander Stuijk[1], Jeroen Voeten[1], Marc Geilen[1], Ramon Schiffelers[2] and Henk Corporaal[1]
[1]Eindhoven University of Technology, NL; [2]ASML, NL

1200 **A DYNAMIC COMPUTATION METHOD FOR FAST AND ACCURATE PERFORMANCE EVALUATION OF MULTI-CORE ARCHITECTURES**

Sebastien Le Nours[1], Adam Postula[2] and Neil Bergmann[2]
[1]University of Nantes, FR; [2]University of Queensland, AU

1215 **CROSS-CORRELATION OF SPECIFICATION AND RTL FOR SOFT IP ANALYSIS**

Bhanu Singh[1], Arunprasath Shankar[1], Francis Wolff[1], Christos Papachristou[1], Daniel Weyer[2] and Steve Clay[2]
[1]Case Western Reserve University, US; [2]Rockwell Automation, US

1230 **LUNCH BREAK** in Exhibition Area

10.6 Multi-processor and distributed systems

Konferenz 4 1100 – 1230

Chair: **Orlando Moreira,** Ericsson, NL
Co-Chair: **Giuseppe Lipari,** ENS - Cachan, FR

This session features new results in scheduling, allocation and management of real-time application in multi-core and distributed systems. The first paper presents a control algorithm for managing real-time tasks so to meet thermal constraints in a multi-core chip. The second paper proposes an algorithm for mixed-criticality task allocation in a multiprocessor platform. The third paper proposes a method for generating a schedule for a multi-mode application in a distributed system.

1100 **THERMAL-AWARE FREQUENCY SCALING FOR ADAPTIVE WORKLOADS ON HETEROGENEOUS MPSOCS**

Heng Yu, Rizwan Syed and Yajun Ha, National University of Singapore, SG

1130 **PARTITIONED MIXED-CRITICALITY SCHEDULING ON MULTIPROCESSOR PLATFORMS**

Chuancai Gu[1], Nan Guan[2], Qingxu Deng[1] and Wang Yi[2]
[1]Northeastern University, CN; [2]Uppsala University, SE

1200 **GENERATION OF COMMUNICATION SCHEDULES FOR MULTI-MODE DISTRIBUTED REAL-TIME APPLICATIONS**

Akramul Azim, Gonzalo Carvajal, Rodolfo Pellizzoni and Sebastian Fischmeister, University of Waterloo, CA

1230 **LUNCH BREAK** in Exhibition Area

10.7 Advances in Synthesis

Konferenz 5 1100 – 1230

Chair: **John Hayes,** University of Michigan, US
Co-Chair: **Kim Taemin,** Intel Labs, US

Papers in this session address synthesis algorithms and tools at different levels, targeting power, area and delay minimization.

1100 **PROVABLY MINIMAL ENERGY USING COORDINATED DVS AND POWER GATING**

Nathaniel Conos, Saro Meguerdichian, Foad Dabiri and Miodrag Potkonjak, UCLA, US

1130 **A TREE ARBITER CELL FOR HIGH SPEED RESOURCE SHARING IN ASYNCHRONOUS ENVIRONMENTS**

Syed Rameez Naqvi and Andreas Steininger, Vienna University of Technology, AT

1200 **AN EFFICIENT MANIPULATION PACKAGE FOR BICONDITIONAL BINARY DECISION DIAGRAMS**

Luca Amaru, Pierre-Emmanuel Gaillardon and Giovanni De Micheli, EPFL, CH

1215 **SYNTHESIS ALGORITHM OF PARALLEL INDEX GENERATION UNITS**

Yusuke Matsunaga, Kyushu University, JP

IPS **IP5-7, IP5-8, IP5-9, IP5-10**

1230 **LUNCH BREAK** in Exhibition Area

10.8 EDA+3D+MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics

Exhibition Theatre 1100 – 1230

Organiser: **Jürgen Haase,** edacentrum, DE
Moderator: **Ahmed Jerraya,** CEA-LETI, FR
Panelists: **Gabriel Kittler,** X-FAB, DE
Brandon Wang, Cadence, US
Brent Gregory, Synopsys, US
Horst Symanzik, Bosch-Sensortec GmbH, DE
Gerd Teepe, GLOBALFOUNDRIES, DE

Today the most powerful innovations in the major industries and the most promising approaches to tackle burning societal challenges are substantially influenced by and depending from the innovations provided by the microelectronics industry. Breakthroughs in manufacturing technologies enable the realization of novel types of devices and of systems, which enable applications with fascinating functionality and enormous performance. However, this innovation chain is not operational without appropriate innovations in design technology: We need an innovation Agenda 2020 for design methodology and EDA tools fueling the innovation chain of electronics.

2014 the technologies for MEMS and for 3D chips have reached a maturity level that enables them to reshape our lives until 2020. This panel will discuss how to utilize these technologies: Which applications will become possible with the upcoming innovations in 3D and MEMS technologies, what kind of EDA innovations will be required in order to be able to implement these applications effectively and efficiently, yielding powerful yet reliable components and systems.

The set-up of the panel includes the manufacturers GLOBALFOUNDRIES and X-FAB, Bosch as leading supplier of technology and one of the MEMS pioneers as well as leading EDA vendors Cadence and Synopsys.

1230 **LUNCH BREAK** in Exhibition Area

11.0 Special Day Keynote

Saal 1 1330 – 1400

Organic semiconductors with conjugated electron system are currently intensively investigated for optoelectronic applications. This interest is spurred by novel devices such as organic light-emitting diodes (OLED), organic solar cells, and flexible electronics. I this talk, I will discuss some of the recent progress in realizing devices, in particular highly efficient white OLED for lighting and flexible organic solar cells.

1330 **ORGANIC ELECTRONICS - FROM LAB TO MARKETS**

Karl Leo, Technische Universität Dresden, DE

11.1 SPECIAL DAY Embedded Tutorial: Alternatives to CMOS

Saal 1 1400 – 1530

Organisers: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Thomas Mikolajick, NamLab gGmbH, DE
Chair: **Aida Todri,** LIRMM, FR
Co-Chair: **Thomas Mikolajick,** NamLab gGmbH, DE

Alternative approaches to CMOS-based computing structures abound, for logic, memory, interconnect and interfaces. This embedded tutorial aims to give in-depth analyses of three promising technologies. The first paper covers spintronics and its use in logic and memory to achieve low-power computing architectures. Silicon photonics, with anticipated benefits for interconnect structures, is examined in the second paper. The third paper looks at the status of organic electronics and the properties of thin-film transistors for large displays and sensor arrays on flexible supports.

1400 **SPINTRONICS FOR LOW-POWER COMPUTING**

Yue Zhang[1], Weisheng Zhao[1], Jacques-Olivier Klein[1], Wang Kang[1], Damien Querlioz[1], Youguang Zhang[2], Dafiné Ravelosona[1] and Claude Chappert[1]
[1]IEF - Univ. Paris Sud, FR; [2]Univ. Beihang, CN

1430 **CHAMELEON: CHANNEL EFFICIENT OPTICAL NETWORK-ON-CHIP**

Sébastien Le Beux[1], Hui Li[1], Ian O'Connor[1], Kazem Cheshmi[2], Xuchen Liu[1], Jelena Trajkovic[2] and Gabriela Nicolescu[3]
[1]Lyon Institute of Nanotechnology, FR; [2]Concordia University, CA; [3]Ecole Polytechnique de Montréal, CA

1500 **LOW-VOLTAGE ORGANIC TRANSISTORS FOR FLEXIBLE ELECTRONICS**

Ute Zschieschang[1], Reinhold Rödel[1], Ulrike Kraft[1], Kazuo Takimiya[2], Tarek Zaki[3], Florian Letzkus[4], Jörg Butschke[4], Harald Richter[4], Joachim Burghartz[4], Wei Xiong[5], Boris Murmann[5] and Hagen Klauk[1]
[1]Max Planck Institute for Solid State Research, DE; [2]Riken Advanced Science Institute, JP; [3]University of Stuttgart, DE; [4]IMS CHIPS, DE; [5]Stanford University, US

11.2 Transitioning NoC Design Techniques to Future Challenges

Konferenz 6 1400 – 1530

Chair: **Masoud Daneshtalab,** University of Turku, FI
Co-Chair: **Hiroki Matsutani,** Keio University, JP

The first paper of the session presents an approach to tolerating faults in NoCs through runtime reconfiguration, which is of increasing importance. The second paper focuses on management of thermal behaviour in NoCs to improve the reliability of optical communication given the tight tolerances of silicon photonics. Finally, the third paper also provides an outlook on optical NoCs by contrasting their properties against those of aggressive electrical baselines, to provide directions for future research in the field.

1400 **BRISK AND LIMITED-IMPACT NOC ROUTING RECONFIGURATION**

Doowon Lee, Ritesh Parikh and Valeria Bertacco, University of Michigan, US

1430 **THERMAL MANAGEMENT OF MANYCORE SYSTEMS WITH SILICON-PHOTONIC NETWORKS**

Tiansheng Zhang, José L. Abellán, Ajay Joshi and Ayse K. Coskun, Boston University, US

1500 **ASSESSING THE ENERGY BREAK-EVEN POINT BETWEEN AN OPTICAL NOC ARCHITECTURE AND AN AGGRESSIVE ELECTRONIC BASELINE**

Luca Ramini[1], Paolo Grani[2], Herve Tatenguem Fankem[1], Alberto Ghiribaldi[1], Sandro Bartolini[2] and Davide Bertozzi[1]
[1]Engineering Department of the University of Ferrara, IT; [2]University of Siena, IT

IPS **IP5-11, IP5-12**

1530 **COFFEE BREAK** in Exhibition Area

11.3 Industry relevant research and practice for system design

Konferenz 1 1400 – 1530

Chair: **Emil Matus,** Technische Universität Dresden, DE
Co-Chair: **Norbert Wehn,** TU Kaiserslautern, DE

This session addresses various aspects of system modeling, synthesis, validation and verification with the strong focus on industrial relevance.

1400 **THE METAMODELING APPROACH TO SYSTEM LEVEL SYNTHESIS**

Wolfgang Ecker[1], Michael Velten[1], Leily Zafari[1] and Ajay Goyal[2]
[1]Infineon Technologies, DE; [2]Infineon Technologies, IN

1415 **LOGIC SYNTHESIS OF LOW-POWER ICS WITH ULTRA-WIDE VOLTAGE AND FREQUENCY SCALING**

Yu Pu, Juan Echeverri, Maurice Meijer and Jose Pineda de Gyvez, NXP Research, NL

1430 **FORMAL VERIFICATION OF TAINT-PROPAGATION SECURITY PROPERTIES IN A COMMERCIAL SOC DESIGN**

Pramod Subramanyan[1] and Divya Arora[2]
[1]Princeton University, US; [2]Intel Corporation, US

1445 **EARLY DESIGN STAGE THERMAL EVALUATION AND MITIGATION: THE LOCOMOTIV ARCHITECTURAL CASE**

Tanguy Sassolas[1], Chiara Sandionigi[1], Alexandre Guerre[1], Alexandre Aminot[1], Pascal Vivet[2], Hela Boussetta[3], Luca Ferro[3] and Nicolas Peltier[3]
[1]CEA, LIST, FR; [2]CEA-LETI, FR; [3]DOCEA Power, FR

1500 **MULTI-DISCIPLINARY INTEGRATED DESIGN AUTOMATION TOOL FOR AUTOMOTIVE CYBER-PHYSICAL SYSTEMS**

Arquimedes Canedo[1], Mohammad Abdullah Al Faruque[2] and Jan Richter[1]
[1]Siemens Corporation, US; [2]University of California Irvine, US

1515 **PREDICTIVE PARALLEL EVENT-DRIVEN HDL SIMULATION WITH A NEW POWERFUL PREDICTION STRATEGY**

Seiyang Yang[1], Jaehoon Han[1], Doowhan Kwak[1], Namdo Kim[2], Daeseo Cha[2], Junhyuck Park[2] and Jay Kim[2]
[1]Pusan National University, KR; [2]Samsung Electronics Co., KR

1530 **COFFEE BREAK** in Exhibition Area

11.4 Enabling validation on fast platforms

Konferenz 2 1400 – 1530

Chair: **Ronny Morad,** IBM, IL
Co-Chair: **Franco Fummi,** Universita' di Verona, IT

Fast platforms, whether acceleration, post-silicon or virtual prototypes, are key technologies to enabling validation of complex systems. However, they present enormous challenges to become effective. This session presents four papers and two IPs that propose solutions to overcome some of them, thus enabling much higher performance and coverage.

1400 **COVERAGE EVALUATION OF POST-SILICON VALIDATION TESTS WITH VIRTUAL PROTOTYPES**

Kai Cong, Li Lei, Zhenkun Yang and Fei Xie, Portland State University, US

1430 **ARCHIVED: ARCHITECTURAL CHECKING VIA EVENT DIGESTS FOR HIGH PERFORMANCE VALIDATION**

Chang-Hong Hsu[1], Debapriya Chatterjee[2], Ronny Morad[3], Raviv Gal[3] and Valeria Bertacco[1]
[1]University of Michigan, Ann Arbor, US; [2]IBM Research - Austin, US; [3]IBM Research - Haifa, IL

1500 **EFFECTIVE POST-SILICON FAILURE LOCALIZATION USING DYNAMIC PROGRAM SLICING**

Ophir Friedler, Wisam Kadry, Arkadiy Morgenshtein, Amir Nahir and Vitali Sokhin, IBM Research - Haifa, IL

1515 **DESIGN-FOR-DEBUG ROUTING FOR FIB PROBING**

Chia-Yi Lee, Tai-Hung Li and Tai-Chen Chen, National Central University, TW

IPS **IP5-13, IP5-14**

1530 **COFFEE BREAK** in Exhibition Area

11.5 Memory Resource Allocation and Scheduling in MPSoC

Konferenz 3 1400 – 1530

Chair: **Andreas Herkersdorf,** Technische Universität München, DE
Co-Chair: **Donatella Sciuto,** Politecnico di Milano, IT

Low-latency data access and efficient interprocess communication are critical to MPSoC performance and power efficiency. This session introduces innovative approaches for data placement, memory bandwidth allocation and scheduling techniques in MPSoC architectures with heterogeneous 2D/3D memory hierarchies.

1400 **SCENARIO-AWARE DATA PLACEMENT AND MEMORY AREA ALLOCATION FOR MULTI-PROCESSOR SYSTEM-ON-CHIPS WITH RECONFIGURABLE 3D-STACKED SRAMS**

Meng-Ling Tsai, Yi-Jung Chen, Yi-Ting Chen and Ru-Hua Chang, Department of Computer Science and Information Engineering, National Chi Nan University, TW

1430 **OPTIMIZED BUFFER ALLOCATION IN MULTICORE PLATFORMS**

Maximilian Odendahl[1], Andres Goens[1], Rainer Leupers[1], Gerd Ascheid[1], Benjamin Ries[1], Berthold Vöcking[1] and Tomas Henriksson[2]
[1]RWTH Aachen University, DE; [2]Huawei Technologies, SE

1500 **MEMORY-CONSTRAINED STATIC RATE-OPTIMAL SCHEDULING OF SYNCHRONOUS DATAFLOW GRAPHS VIA RETIMING**

Xue-Yang Zhu[1], Marc Geilen[2], Twan Basten[3] and Sander Stuijk[2]
[1]State Key Laboratory of Computer Science, Institute of Software, Chinese Academy of Sciences, CN; [2]Department of Electrical Engineering, Eindhoven University of Technology, NL; [3]Department of Electrical Engineering, Eindhoven University of Technology. Embedded Systems Institute, NL

1515 **A CONSTRAINT-BASED DESIGN SPACE EXPLORATION FRAMEWORK FOR REAL-TIME APPLICATIONS ON MPSOCS**

Kathrin Rosvall and Ingo Sander, KTH Royal Institute of Technology, SE

IPS **IP5-15, IP5-16**

1530 **COFFEE BREAK** in Exhibition Area

11.6 System-Level Thermal Estimation and Management

Konferenz 4 1400 – 1530

Chair: **Coskun Ayse,** Boston University, US
Co-Chair: **Oliver Bringmann,** University of Tübingen, DE

This session deals with thermal management issues in multicore and battery-operated systems. In particular the papers cover three orthogonal aspects, specifically, thermal estimation and tracking from sparse sensor readings, proactive dynamic thermal management via task migration, and thermal management of hybrid energy storage devices based on idle period insertion.

1400 **MINIMAL SPARSE OBSERVABILITY OF COMPLEX NETWORKS: APPLICATION TO MPSOC SENSOR PLACEMENT AND RUN-TIME THERMAL ESTIMATION & TRACKING**

Santanu Sarma and Nikil Dutt, University of California Irvine, US

1430 **MDTM: MULTI-OBJECTIVE DYNAMIC THERMAL MANAGEMENT FOR ON-CHIP SYSTEMS**

Heba Khdr, Thomas Ebi, Muhammad Shafique, Hussam Amrouch and Jörg Henkel, Karlsruhe Institute of Technology (KIT), DE

1500 **THERMAL MANAGEMENT OF BATTERIES USING A HYBRID SUPERCAPACITOR ARCHITECTURE**

Donghwa Shin[1], Massimo Poncino[2] and Enrico Macii[3]
[1]Department of Computer Engineering, Yeungnam University, KR; [2]Politecnico di Torino, IT; [3]Dipartimento di Automatica e Informatica, Politecnico di Torino, IT

IPS **IP5-17, IP5-18, IP5-19**

1530 **COFFEE BREAK** in Exhibition Area

11.7 Power and Emerging Technologies in Reconfigurable Computing

Konferenz 5 1400 – 1530

Chair: **Diana Goehringer,** Ruhr-University Bochum (RUB), DE
Co-Chair: **Fabrizio Ferrandi,** Politecnico di Milano, IT

The first two papers in this session propose new architectures that take advantage of emerging nonvolatile memory technologies. The third paper proposes a battery cell aware task partitioning and mapping to maximize battery runtime.

1400 **EXPLOITING STT-NV TECHNOLOGY FOR RECONFIGURABLE, HIGH PERFORMANCE, LOW POWER, AND LOW TEMPERATURE FUNCTIONAL UNIT DESIGN**

Adarsh Reddy[1], Hamid Mahmoodi[2] and Houman Homayoun[1]
[1]George Mason University, US; [2]San Francisco State University, US

1430 **A POWER-EFFICIENT RECONFIGURABLE ARCHITECTURE USING PCM CONFIGURATION TECHNOLOGY**

Ali Ahari[1], Hossein Asadi[1], Behnam Khaleghi[1] and Mehdi Tahoori[2]
[1]Sharif University of Technology, IR; [2]Karlsruhe Institute of Technology, DE

1500 **EXTENDING LIFETIME OF BATTERY-POWERED COARSE-GRAINED RECONFIGURABLE COMPUTING PLATFORMS**

Shouyi Yin[1], Peng Ouyang[1], Leibo Liu[2] and Shaojun Wei[1]
[1]Tsinghua University, CN; [2]Institute of Microelectronics and The National Lab for Information Science and Technology, Tsinghua University, CN

IPS **IP5-20, IP5-21, IP5-22**

1530 **COFFEE BREAK** in Exhibition Area

11.8 Embedded Tutorial: GPGPUs: how to combine high computational power with high reliability

Exhibition Theatre 1400 – 1530

Organiser: **Matteo Sonza Reorda,** Politecnico di Torino, IT
Chair: **Dimitris Gizopoulos,** University of Athens, GR
Co-Chair: **Rob Aitken,** ARM, US

The embedded tutorial aims at providing with an updated view on what GPGPUs can provide not only in terms of performance and power, but also in terms of reliability, and how the latter can be evaluated and possibly improved.

1400 **RELIABILITY REQUIREMENTS FOR GPUS IN HPC**

Nathan A. DeBardeleben[1], Leonardo Bautista Gomez[2] and Franck Cappello[2]
[1]Los Alamos National Laboratory, US; [2]Argonne National Laboratory, US

1430 **GPU RELIABILITY ASSESSMENT AND ENHANCEMENT**

Paolo Rech[1], Luigi Carro[1] and Steve Keckler[2]
[1]UFRGS, BR; [2]NVIDIA, US

1500 **EVALUATING THE ROBUSTNESS OF GPU APPLICATIONS THROUGH FAULT INJECTION**

Karthik Pattabiraman[1], Bo Fang[1] and Sudhanva Gurumurthi[2]
[1]UBC, CA; [2]AMD, US

1530 **COFFEE BREAK** in Exhibition Area

IP5 Interactive Presentations

Conference Level, Foyer 1530 – 1600

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP5-1 **HYBRID WIRE-SURFACE WAVE ARCHITECTURE FOR ONE-TO-MANY COMMUNICATION IN NETWORK-ON-CHIP**

Ammar Karkar[1], Nizar Dahir[1], Ra'ed Al-Dujaily[2], Kenneth Tong[3], Terrence Mak[4] and Alex Yakovlev[1]
[1]School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, GB; [2]General Systems Company, Baghdad - Iraq, IQ; [3]Depart- ment of Electrical and Electronic Engineering, University College London, GB; [4]Department of Computer Science and Engineering, The Chinese University of Hong Kong, Shatin, Hong, CN

IP5-2 **FAILURE ANALYSIS OF A NETWORK-ON-CHIP FOR REAL-TIME MIXED-CRITICAL SYSTEMS**

Eberle A Rambo, Alexander Tschiene, Jonas Diemer, Leonie Ahrendts and Rolf Ernst
Technische Universität Braunschweig, DE

IP5-3 **COOLIP: SIMPLE YET EFFECTIVE JOB ALLOCATION FOR DISTRIBUTED THERMALLY-THROTTLED PROCESSORS**

Pratyush Kumar, Hoeseok Yang, Iuliana Bacivarov and Lothar Thiele, ETH Zurich, CH

IP5-4 **ENERGY OPTIMIZATION IN 3D MPSOCS WITH WIDE-I/O DRAM USING TEMPERATURE VARIATION AWARE BANK-WISE REFRESH**

Mohammadsadegh Sadri[1], Matthias Jung[2], Christian Weis[2], Norbert Wehn[2] and Luca Benini[1]
[1]Department of Electrical, Electronic and Information Engineering (DEI) University of Bologna, IT; [2]Microelectronic Systems Design Research Group, University of Kaiserslautern, DE

IP5-5 **EFFICIENT SIMULATION AND MODELLING OF NON-RECTANGULAR NOC TOPOLOGIES**

Ji Qi and Mark Zwolinski, University of Southampton, GB

IP5-6 **MOVING FROM CO-SIMULATION TO SIMULATION FOR EFFECTIVE SMART SYSTEMS DESIGN**

Franco Fummi[1], Michele Lora[2], Francesco Stefanni[3], Dimitrios Trachanis[4], Jan Vanhese[4] and Sara Vinco[2]
[1]University of Verona, EDALab s.r.l., IT; [2]University of Verona, IT; [3]EDALab s.r.l., IT; [4]Agilent Technologies, BE

IP5-7 **AUTOMATING DATA REUSE IN HIGH-LEVEL SYNTHESIS**

Wim Meeus[1] and Dirk Stroobandt[2]
[1]Imec and Ghent University, BE; [2]Ghent University, BE

IP5-8 **A UNIVERSAL SYMMETRY DETECTION ALGORITHM**

Peter Maurer, Dept. of Computer Sci., Baylor University, US

IP5-9 **OPTIMIZATION OF DESIGN COMPLEXITY IN TIME-MULTIPLEXED CONSTANT MULTIPLICATIONS**

Levent Aksoy[1], Paulo Flores[2] and Jose Monteiro[3]
[1]INESC-ID, PT; [2]INESC-ID/IST ULisbon, PT; [3]INESC-ID / IST, ULisbon, PT

IP5-10 **HARDWARE PRIMITIVES FOR THE SYNTHESIS OF MULTITHREADED ELASTIC SYSTEMS**

Giorgos Dimitrakopoulos[1], Seitanidis Ioannis[2], Anastasios Psarras[1], Konstantinos Tsiouris[1], Pavlos Matthaiakis[3] and Jordi Cortadella[4]
[1]Democritus University of Thrace, GR; [2]Democritus University of Thrac, GR; [3]Mentor Graphics, FR; [4]Universitat Politecnica de Catalunya, ES

IP5-11 **DCM: AN IP FOR THE AUTONOMOUS CONTROL OF OPTICAL AND ELECTRICAL RECONFIGURABLE NOCS.**

Wolfgang Büter[1], Christof Osewold[1], Daniel Gregorek[1] and Alberto Garcia-Ortiz[2]
[1]University of Bremen, DE; [2]ITEM (U.Bremen), DE

IP5-12 **MINIMALLY BUFFERED SINGLE-CYCLE DEFLECTION ROUTER**

Gnaneswara Rao Jonna[1], John Jose[1], Rachana Radhakrishnan[2] and Madhu Mutyam[1]
[1]Indian Institute of Technology, Madras., IN; [2]Rajagiri School of Engineering & Technology, Kochhi., IN

IP5-13 **FUNCTIONAL TEST GENERATION GUIDED BY STEADY-STATE PROBABILITIES OF ABSTRACT DESIGN**

Jian Wang[1], Huawei Li[2], Tao Lv[2], Tiancheng Wang[2] and Xiaowei Li[2]
[1]Institute of Computing Technology, Chinese Academy of Sc iences, CN; [2]Institute of Computing Technology, Chinese Academy of Sciences, CN

IP5-14 **AUTOMATED SYSTEM TESTING USING DYNAMIC AND RESOURCE RESTRICTED CLIENTS**

Mirko Caspar, Mirko Lippmann and Wolfram Hardt, Technische Universität Chemnitz, DE

IP5-15 **RELIABILITY-AWARE MAPPING OPTIMIZATION OF MULTI-CORE SYSTEMS WITH MIXED-CRITICALITY**

Shin-Haeng Kang[1], Hoeseok Yang[2], Sungchan Kim[3], Iuliana Bacivarov[2], Soonhoi Ha[1] and Lothar Thiele[2]
[1]Seoul National University, KR; [2]ETH Zurich, CH; [3]Chonbuk National University, KR

IP5-16 **FROM SIMULINK TO NOC-BASED MPSOC ON FPGA**

Francesco Robino and Johnny Öberg, KTH Royal Institute of Technology, SE

IP5-17 **THERMAL ANALYSIS AND MODEL IDENTIFICATION TECHNIQUES FOR A LOGIC + WIDEIO STACKED DRAM TEST CHIP**

Francesco Beneventi[1], Andrea Bartolini[1], Pascal Vivet[2], Denis Dutoit[2] and Luca Benini[1]
[1]DEI - University of Bologna, IT; [2]CEA-Leti, Grenoble, FR

IP5-18 **ADAPTIVE POWER ALLOCATION FOR MANY-CORE SYSTEMS INSPIRED FROM MULTIAGENT AUCTION MODEL**

Xiaohang Wang[1], Baoxin Zhao[1], Terrence Mak[2], Mei Yang[3], Yingtao Jiang[3], Masoud Daneshtalab[4] and Maurizio Palesi[5]
[1]Guangzhou Institute of Advanced Technology, CN; [2]The Chinese University of Hong Kong, CN; [3]University of Nevada, Las Vegas, US; [4]University of Turku, FI; [5]University of Enna, Kore, IT

IP5-19 **UNIFIED, ULTRA COMPACT, QUADRATIC POWER PROXIES FOR MULTI-CORE PROCESSORS**

Muhammad Yasin[1], Ibrahim (Abe) Elfadel[2] and Anas Shahrour[2]
[1]New York University - Abu Dhabi, AE; [2]Masdar Institute of Science and Technology, AE

IP5-20 **3D FPGA USING HIGH-DENSITY INTERCONNECT MONOLITHIC INTEGRATION**

Ogun Turkyilmaz[1], Gerald Cibrario[2], Olivier Rozeau[2], Perrine Batude[2] and Fabien Clermidy[3]
[1]CEA-LETI, Minatec Campus, FR; [2]CEA, FR; [3]CEA-LETI, FR

IP5-21 **JOINT COMMUNICATION SCHEDULING AND INTERCONNECT SYNTHESIS FOR FPGA-BASED MANY-CORE SYSTEMS**

Alessandro Cilardo, Edoardo Fusella, Luca Gallo and Antonino Mazzeo, University of Naples Federico II, IT

IP5-22 **A NOVEL EMBEDDED SYSTEM FOR VISION TRACKING**

Antonis Nikitakis[1], Theofilos Paganos[1] and Ioannis Papaefstathiou[2]
[1]Technical University of Crete, Department of Electronic and Computer Engineering Kounoupidiana, Chania, Crete, GR73100, Greece, GR; [2]Synelixis Solutions Ltd, Farmakidou 10,Chalkida, GR34100, Greece, GR

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

12.1 SPECIAL DAY Hot Topic: The future of interfacing to the natural world

Saal 1 1600 – 1730

Organisers: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Thomas Mikolajick, NamLab gGmbH, DE
Chair: **Michael Huebner,** Ruhr Universitaet Bochum, DE
Co-Chair: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR

Challenges for acquiring and processing data from the real world includes the development of interfaces capable of extracting relevant information from massive sensor networks or from living organisms, sifting through the wealth of data to arrive systematically at a meaningful conclusion, and building hardware platforms suited to carry out these operations in an energy-efficient way. The first paper in this session looks at the necessarily complex processing of chemical information with hardware components that are capable of responding to various chemical conditions. Interfaces to living organisms are examined in the second paper, which discusses challenges and approaches for efficient detection of disease. In the third paper, novel hardware devices and architectures are explored for use in energy-efficient video analysis applications such as movement detection and face recognition. The fourth paper discusses handling of complex data with large-scale GPU-based recurrent networks, exploiting specific features of the data to improve energy efficiency.

THURSDAY

1600 **INTEGRATED CIRCUITS PROCESSING CHEMICAL INFORMATION: PROSPECTS AND CHALLENGES**

Andreas Richter, Axel Voigt, René Schüffny, Stephan Henker and Marcus Völp, Technische Universität Dresden, DE

1625 **INTERFACING TO LIVING CELLS**

Rudy Lauwereins, IMEC, BE

1645 **VIDEO ANALYTICS USING BEYOND CMOS DEVICES**

Vijaykrishnan Narayanan[1], Gert Cauwenberghs[2], Donald Chiarulli[3], Suman Datta[4], Steve Levitan[3] and Philip Wong[5]
[1]Penn State University, US; [2]University of California at San Deigo, US; [3]University of Pittsburgh, US; [4]The Pennsylvania State University, US; [5]Stanford University, US

1710 **ENERGY EFFICIENT NEURAL NETWORKS FOR BIG DATA ANALYTICS**

Wang Yu, Boxun Li, Rong Luo, Yiran Chen, Ningyi Xu and Huazhong Yang, Tsinghua University, CN

12.2 Hot Topic: How Secure are PUFs Really? On the Reach and Limits of Recent PUF Attacks

Konferenz 6 1600 – 1730

Organiser: **Ulrich Rührmair,** TU München, DE
Chair: **Ulf Schlichtmann,** TU München, DE

PUFs are an emerging and promising security primitive. However, some strong attacks on their core security features have been reported recently, for example on their unclonability. We discuss the reach, but also the limits of these attacks, aiming at a well-balanced treatment, and also evaluate the future perspectives of the field.

1600 **PUFS AT A GLANCE**

Ulrich Rührmair[1] and Daniel E. Holcomb[2]
[1]TU München, DE; [2]University of Michigan, US

1615 **PUF MODELING ATTACKS: AN INTRODUCTION AND OVERVIEW**

Ulrich Rührmair[1] and Jan Sölter[2]
[1]TU München, DE; [2]Freie Universität Berlin, DE

1630 **HYBRID SIDE-CHANNEL / MACHINE-LEARNING ATTACKS ON PUFS: A NEW THREAT?**

Xiaolin Xu and Wayne Burleson, Umass, Amherst, US

1645 **PHYSICAL VULNERABILITIES OF PHYSICALLY UNCLONABLE FUNCTIONS**

Clemens Helfmeier, Dmitry Nedospasov, Shahin Tajik, Christian Boit and Jean-Pierre Seifert, Technische Universität Berlin, DE

1700 **PROTOCOL ATTACKS ON ADVANCED PUF PROTOCOLS AND COUNTERMEASURES**

Marten van Dijk[1] and Ulrich Rührmair[2]
[1]University of Connecticut, US; [2]TU München, DE

1715 **QUO VADIS, PUF? TRENDS AND CHALLENGES OF EMERGING PHYSICAL-DISORDER BASED SECURITY**

Masoud Rostami[1], Farinaz Koushanfar[1], James Wendt[2] and Miodrag Potkonjak[2]
[1]Rice University, US; [2]UCLA, US

12.3 Multimedia Systems

Konferenz 1 1600 – 1730

Chair: **Theocharides Theocharis,** University of Cyprus, CY
Co-Chair: **Cristiana Bolchini,** Politecnico di Milano, IT

The session presents designs for energy efficient and flexible implementations of advanced video coders or image acquisition/processing systems

1600 **FLEXIBLE AND SCALABLE IMPLEMENTATION OF H.264/AVC ENCODER FOR MULTIPLE RESOLUTIONS USING ASIPS**

Hong Chinh Doan, Haris Javaid and Sri Parameswaran, School of Computer Science and Engineering, University of New South Wales, Sydney, AU

1630 **A FLEXIBLE ASIP ARCHITECTURE FOR CONNECTED COMPONENTS LABELING IN EMBEDDED VISION APPLICATIONS**

Juan Fernando Eusse[1], Rainer Leupers[1], Gerd Ascheid[1], Patrick Sudowe[1], Bastian Leibe[1] and Tamon Sadasue[2]
[1]RWTH Aachen University, DE; [2]RICOH Company LTD., JP

1700 **IMAGE PROGRESSIVE ACQUISITION FOR HARDWARE SYSTEMS**

Jianxiong Liu, Christos Bouganis and Peter Y.K. Cheung, Imperial College London, GB

1715 **HIGH-QUALITY REAL-TIME HARDWARE STEREO MATCHING BASED ON GUIDED IMAGE FILTERING**

Christos Ttofis and Theocharis Theocharides, University of Cyprus, CY

12.4 Physical Aspects

Konferenz 2 1600 – 1730

Chair: **Carl Sechen,** University of Texas at Dallas, US
Co-Chair: **Jens Lienig,** TU Dresden, DE

This session focuses on contemporary issues in physical design. The first paper concerns detailed placement for sub-20nm technologies. Then pattern matching for more efficient hotspot detection is introduced. Finally, a flow for minimizing the number of wiring layers on multichip interposers is presented.

1600 **OPTIMIZATION OF STANDARD CELL BASED DETAILED PLACEMENT FOR 16 NM FINFET PROCESS**

Yuelin Du and Martin D. F. Wong, University of Illinois at Urbana-Champaign, US

1630 **SIGNATURE INDEXING OF DESIGN LAYOUTS FOR HOTSPOT DETECTION**

Cristian Andrades[1], Andrea Rodriguez[1] and Charles Chiang[2]
[1]Universidad de Concepcion, CL; [2]Synopsys Inc., US

1700 **METAL LAYER PLANNING FOR SILICON INTERPOSERS WITH CONSIDERATION OF ROUTABILITY AND MANUFACTURING COST**

Wen-Hao Liu, Tzu-Kai Chien and Ting-Chi Wang, National Tsing Hua University, TW

12.5 System-level Design Space Exploration

Konferenz 3 1600 – 1730

Chair: **Frederic Petrot,** TIMA, FR
Co-Chair: **Luciano Lavagno,** Politecnico di Torino, IT

The sessions discusses novel aspects and objectives in the exploration of embedded architectures. Papers cover topics including integration of diagnosis, approximate circuit design, custom instruction optimization, and scheduling issues.

1600 **NON-INTRUSIVE INTEGRATION OF ADVANCED DIAGNOSIS FEATURES IN AUTOMOTIVE E/E-ARCHITECTURES**

Ulrich Abelein[1], Alejandro Cook[2], Piet Engelke[3], Michael Glaß[4], Felix Reimann[4], Laura Rodríguez Gómez[2], Thomas Russ[4], Jürgen Teich[4], Dominik Ull[2] and Hans-Joachim Wunderlich[2]
[1]AUDI AG, Ingolstadt, DE; [2]University of Stuttgart, DE; [3]Infineon Technologies AG, DE; [4]University of Erlangen-Nuremberg, DE

1630 **ABACUS: A TECHNIQUE FOR AUTOMATED BEHAVIORAL SYNTHESIS OF APPROXIMATE COMPUTING CIRCUITS**

Kumud Nepal, Yueting Li, R. Iris Bahar and Sherief Reda, Brown University, Providence, Rhode Island, US

1700 **AUTOMATIC GENERATION OF CUSTOM SIMD INSTRUCTIONS FOR SUPERWORD LEVEL PARALLELISM**

Taemin Kim and Yatin Hoskote, Intel/Intel Labs, US

1715 **SYSTEM-LEVEL SCHEDULING OF REAL-TIME STREAMING APPLICATIONS USING A SEMI-PARTITIONED APPROACH**

Emanuele Cannella, Mohamed Bamakhrama and Todor Stefanov, Leiden University, NL

12.6 Error Resilience and Power Management

Konferenz 4 1600 – 1730

Chair: **William Fornaciari,** Politecnico di Milano - DEIB, IT
Co-Chair: **Kim Gruettner,** OFFIS, DE

This session addresses the trade-off between accuracy and power consumption and the management of multi core/multi systems. The power management is addressed at several abstraction levels from circuit and performance counters up to the system level (operating system).

1600 **ASLAN: SYNTHESIS OF APPROXIMATE SEQUENTIAL CIRCUITS**

Ashish Ranjan, Arnab Raha, Swagath Venkataramani, Kaushik Roy and Anand Raghunathan, PURDUE UNIVERSITY, US

1630 **VRCON: DYNAMIC RECONFIGURATION OF VOLTAGE REGULATORS IN A MULTICORE PLATFORM**

Woojoo Lee, Yanzhi Wang and Massoud Pedram, University of Southern California, US

1700 **COARSE-GRAINED BUBBLE RAZOR TO EXPLOIT THE POTENTIAL OF TWO-PHASE TRANSPARENT LATCH DESIGNS**

Hayoung Kim, Jae-joon Kim, Sungjoo Yoo, Sunggu Lee and Dongyoung Kim, POSTECH, KR

1715 **FEPMA: FINE-GRAINED EVENT-DRIVEN POWER METER FOR ANDROID SMARTPHONES BASED ON DEVICE DRIVER LAYER EVENT MONITORING**

Kitae Kim[1], Donghwa Shin[2], Qing Xie[3], Yanzhi Wang[3], Massoud Pedram[3] and Naehyuck Chang[1]
[1]Seoul National University, KR; [2]Politecnico di Torino, IT; [3]University of Southern California, US

12.7 Built-in Self-Test Solutions for Mixed-Signal and RF ICs

Konferenz 5 1600 – 1730

Chair: **Jacob A. Abraham,** University of Texas, US
Co-Chair: **Marian Verhelst,** KU Leuven, BE

Presentations in this session offer solutions to equip mixed-signal and RF circuits with built-in self-test capabilities. These solutions include the use of an on-chip neural network that maps test signatures directly to a pass/fail decision, loopback test where the transmitter is used to test the receiver, and a reconfiguration principle for pipelined data converters.

1600 **AN ANALOG NON-VOLATILE NEURAL NETWORK PLATFORM FOR PROTOTYPING RF BIST SOLUTIONS**

Dzmitry Maliuk[1] and Yiorgos Makris[2]
[1]Yale University, US; [2]University of Texas at Dallas, US

1630 **BUILT-IN SELF-TEST AND CHARACTERIZATION OF POLAR TRANSMITTER PARAMETERS IN THE LOOP-BACK MODE**

Jae Woong Jeong[1], Sule Ozev[1], Shreyas Sen[2], Vishwanath Natarajan[2] and Mustapha Slamani[3]
[1]Arizona State University, US; [2]Intel Corporation, US; [3]IBM Corp., US

1700 **A FLEXIBLE BIST STRATEGY FOR SDR TRANSMITTERS**

Emanuel Dogaru[1], Filipe Vinci dos Santos[2] and William Rebernak[1]
[1]Thales Communications & Security, FR; [2]Thales Chair on Advanced Analog Design, SUPELEC, FR

1715 **SIGMA-DELTA TESTABILITY FOR PIPELINE A/D CONVERTERS**

Antonio Jose Gines Arteaga and Gildas Leger, Instituto de Microelectronica de Sevilla, IMSE-CNM, (CSIC - Universidad de Sevilla), ES

12.8 Panel: Future SoC verification methodology: UVM evolution or revolution?

Exhibition Theatre 1600 – 1730

Organiser: **Alex Goryachev,** IBM Research - Haifa, IL
Chair: **Rolf Drechsler,** University of Bremen/DFKI, DE

It is a recent trend that SoCs are becoming more similar to servers. Many SoCs today are no longer tied to a single application and look more like general purpose PCs and high-end servers. Smartphones are the most notable example of this, but we are also seeing this with TV chips, in-car controllers, network routers, and more. This trend is occurring in parallel to the constantly growing complexity of SoCs, which support diverse IO interfaces and devices, and have complex architectures including multiple heterogeneous cores, multi-level caches, and multiple IO bridges.

Today, common practice for verification is based on Universal Verification Methodology (UVM), which, at the system level, is built on reusing and combining unit-level environments, followed by running real software on an SoC. This methodology leaves a large gap. In high-end systems, this gap is covered by system-level verification that focuses on HW-only system integration. This level has its own methodology, dedicated environment, set of tools, and teams. It looks at the system as a whole and is not based on reusing lower level environments.

Formal methods are a field of intensive research, but they have not been adopted by the industry for SoC-level verification.

In this panel leading experts from industry (both users and vendors) and academy will discuss the future of SoC verification methodology. Is the gap in today's SoC verification methodology significant? Is it growing? Or perhaps it does not exist? What is the right way to close the gap, if one exists? Is it sufficient to extend UVM capabilities (e.g., SystemC, TLM) or are dedicated tools and methodology needed? Are formal methods ready to play a significant role in SoC-level verification? In general, we would like to determine the importance of system-level verification and its unique needs—whether generators, checking, coverage, or teams.

Panelists: **Christophe Chevallaz,** STMicroelectronics, FR
Franco Fummi, University of Verona, IT
Alan J. Hu, University of British Columbia, Vancouver, CA
Ronny Morad, IBM Research - Haifa, IL
Frank Schirrmeister, Cadence Design Systems, US

FRIDAY 28 MARCH, 2014

Chairs: **Lorena Anghel,** TIMA, FR
Cristiana Bolchini, Politecnico di Milano, IT

This is the twelfth edition of DATE Friday's Workshops initiative, started in 2003 and that has hosted workshops on a variety of topics, attracting every year more and more researchers and designers.

The topics have been changing during the years, following the trend on current and emerging issues in design, test, software and EDA, taking the floor after the regular conference programme running throughout the week. The workshops offer a unique opportunity to present and discuss new and in-progress outcomes as well as experiences and visions.

The Friday's Workshops programme for DATE 2014 includes eight workshop themes, presenting innovative ideas on heterogeneous computing architectures to memristor and cyber-physical systems, from design automation to test and dependability.

For attendees interested in dependable computing, two workshops are available, one focused on GPUs, becoming increasingly popular also for non-graphic intensive computaton, the other on multi-core architectures in the nanotechnology era. Cyber-Physical Systems are the focus of another workshop, dealing with simulation for analyzing, designing and evaluating CPS. A workshop on heterogeneous computing will present the emerging trends and discuss challenges in this area that is receiving a lot of attention, given the variety of available computing resources. This plurality of resources is also the topic of a workshop on many-core embedded systems, investigating the performance, power and predictability aspects of these architectures. Design automation is addressed in a workshop with respect to understanding hardware designs, presenting novel contributions in the area. A new edition of the successful workshop on 3D integration is proposed this year, with new solutions and open challenges. Memristors are the focus of a workshop aimed at proposing a multidiscilinary forum on the latest advances in the field.

Friday's Workshops attendees should choose in advance one workshop among W1, W2, W3, W4, W5, W6, W7 or W8. The workshops run from 0830 until 1700. The individual timetables for each workshop may vary, and for the detailed version of the workshop programmes, visit the workshop webpages.

W1 International Workshop on Dependable GPU Computing

Konferenz 1 0830 – 1700

Organisers:
Dimitris Gizopoulos, University of Athens, GR
Hans-Joachim Wunderlich, University of Stuttgart, DE
Paolo Prinetto, Politecnico di Torino, IT

Many-core hardware accelerators offer significant speedup for parallel applications in different computing segments. Some are originally architected for general-purpose parallel computing while others, like Graphics Processing Units (GPUs), are initially designed for graphics applications, only. GPUs are intensively used today for general-purpose computing (GPGPU computing) through the employment of effective software development frameworks. GPUs and other many-core accelerators have penetrated a very wide range of applications: from embedded and low-power devices to the highest performance supercomputers.

This workshop focuses on an important aspect of GPUs and massively parallel hardware accelerators: dependability and corresponding performance and power/energy considerations. GPUs and accelerators implemented in modern manufacturing technologies are vulnerable (like all other chips) to transient as well as to permanent faults due to radiation, manufacturing defects, variability, aging, etc. In general-purpose computing, the correctness of operation has a much higher priority than in graphics and the applications are expected to deliver correct and fast results. Such dependability provision can be realized at different levels of abstraction and affects the delivered performance of the application as well as it its power/energy behavior. Industry and academia views on the dependability of GPUs will be discussed during the workshop.

0830 **OPENING SESSION**

OPENING REMARKS
Dimitris Gizopoulos[1], Hans-Joachim Wunderlich[2] and Paolo Prinetto[3]
[1]University of Athens, GR; [2]University of Stuttgart, DE; [3]Politecnico di Torino, IT

0830 **KEYNOTE 1:**
GPGPU FOR DEPENDABLE SYSTEMS – A BLESSING OR A CURSE?
Avi Mendelson, Technion, IL

0915 **INVITED TALK 1**

GPGPU RELIABILITY – CHALLENGES AND RESEARCH DIRECTIONS
Sudhanva Gurumurthi, AMD, US

0945 **SESSION 1 – "SOFTWARE APPROACHES FOR GPUS DEPENDABILITY ENHANCEMENT"**
Chair: Murali Annavaram, University of Southern California, Los Angeles, US
Co-Chair: Amir Nahir, IBM Research, IL

0945 **AN IMPROVED FAULT MITIGATION STRATEGY FOR CUDA FERMI GPUS**
Stefano Di Carlo, Giulio Gambardella, Ippazio Martella, Paolo Prinetto, Daniele Rolfo and Pascal Trotta
Politecnico di Torino, IT

1005 **SOFTWARE-BASED TECHNIQUES FOR REDUCING THE VULNERABILITY OF GPU APPLICATIONS**
Si Li[1], Vilas Sridharan[2], Sudhanva Gurumurthi[2] and Sudhakar Yalamanchili[1]
[1]Georgia Tech., US
[2]AMD, US

1025 **A-ABFT: AUTONOMOUS ALGORITHM-BASED FAULT TOLERANCE ON GPUS**
Claus Braun, Sebastian Halder and Hans-Joachim Wunderlich
University of Stuttgart, DE

1045 **COFFEE BREAK+POSTERS**

1130 **INVITED TALK 2**

RELIABLE ACCELERATION – RELIABILITY IN A WORLD OF GPUS & OTHER SPECIAL PURPOSE ACCELERATORS
Arijit Biswas, Intel , US

1200 **LUNCH**

1300 **KEYNOTE 2:**
GPU RELATED ERRORS IN LARGE SCALE SYSTEMS: A STUDY OF BLUE WATERS SUPERCOMPUTER AT NCSA-ILLINOIS
Ravishankar K. Iyer
University of Illinois at Urbana-Champaign, US

1345 **SESSION 2 – "FAULT DETECTION AND TOLERANCE IN GPUS"**
Chair: Nathan DeBardeleben, Los Alamos National Laboratory, US
Co-Chair: Hans-Joachim Wunderlich, University of Stuttgart, DE

1345 **BENEFITS AND COUNTERMEASURES OF INCREASING THE GPU CODE DEGREE OF PARALLELISM**
Paolo Rech and Luigi Carro, UFRGS, BR

1405 **ON THE EVALUATION OF SOFT-ERRORS DETECTION TECHNIQUES FOR GPGPUS**
Davide Sabena[1], Matteo Sonza Reorda[1], Luca Sterpone[1], Paolo Rech[2] and Luigi Carro[2]
[1]Politecnico di Torino
[2]UFRGS, BR

1425 **TOLERATING HARD FAULTS IN GPGPUS**
Waleed Dweik, Mohammad AbdelMajeed and Murali Annavaram
University of Southern California, US

1445 **COFFEE BREAK**

1515 **PANEL SESSION**
Organiser: Dimitris Gizopoulos, University of Athens, GR

1515 **FAULTS IN CPUS AND GPUS: SAME OR DIFFERENT PROBLEMS? SAME OR DIFFERENT SOLUTIONS?**
Sudhakar Yalamanchili[1], Ravishankar Iyer[2], Stefano Di Carlo[3], Sudhanva Gurumurthi[4], Arijit Biswas[5] and Bodo Hoppe[6]
[1]Georgia Tech., US; [2]UIUC, US; [3]Politecnico di Torino, IT
[4]AMD, US; [5]Intel, US; [6]IBM, DE

1645 **CLOSING SESSION**

W2 ES4CPS - Engineering Simulations for Cyber-Physical Systems

Konferenz 2 0830 – 1700

Organisers:
Christian Berger, University of Gothenburg, SE
Ina Schaefer, TU Braunschweig, DE

Nowadays, simulative approaches are mandatory to analyze, design, evaluate, and to prepare real test-runs during the development of these CPS. They enable risk-less and resource-efficient experiments to validate system functions and product families. For example, complex simulations of sensors and the environment are required during the development and validation of self-driving vehicles to safely test the sensor data fusion and algorithms for situation-adaptive driving decisions. The models, which are utilized in these simulations, are continuously improved and enable in the foreseeable future complex analyses of the simulated system, its behavior, and its context. However, simulation experts to design, realize, and maintain these interconnected simulations as well as the simulation environments are limited factors during the development. Thus, methods, metrics, and tools for the engineering of these complex simulation systems are required to effectively design and evaluate these CPS also in the future.

0830 **OPENING SESSION**

0845 **FROM SARTRE TOWARDS AUTONOMOUS DRIVING - AN EXPERIENCE REPORT AND OUTLOOK**
Speaker: Eric Coelingh, Volvo Car Corporation, SE

1000 **COFFEE BREAK**

1030 **SESSION 1**

COMBINING FAULT-INJECTION WITH PROPERTY-BASED TESTING
Speakers: Benjamin Vedder[1], Thomas Art[2], Jonny Vinter[1] and Magnus Jonsson[3]
[1] SP Technical Research Institute of Sweden, SE
[2] Quviq AB, SE
[3] Halmstad University, SE

HOME ENERGY SIMULATION FOR NON-INTRUSIVE LOAD MONITORING APPLICATIONS
Speakers: Krishnan Srinivasarengan, Goutam Y G and Girish Chandra
Tata Consultancy Services Ltd., IN

PHYSICAL SECURITY EVALUATION AT AN EARLY DESIGN-PHASE: A SIDE-CHANNEL AWARE SIMULATION METHODOLOGY
Speakers: Shivam Bhasin[1], Tarik Graba[2], Jean-Luc Danger[1], Yves Mathieu[1], Daisuke Fujimoto[3] and Makoto Nagata[3]
[1]Institut TELECOM, TELECOM ParisTech, CNRS LTCI (UMR 5141), FR
[2]TELECOM Institute / TELECOM ParisTech, FR
[3]Kobe University, Kobe, JP

1200 **LUNCH**

1300 **SESSION 2**

ARCHON: ARCHITECTURE-OPEN RESOURCE-DRIVEN CROSS-LAYER MODELLING FRAMEWORK
Speakers: Ashur Rafiev, Alexei Iliasov, Alexander Romanovsky, Andrey Mokhov, Fei Xia and Alex Yakovlev
Newcastle University, GB

DSL METHODS FOR CPS SIMULATION IN THE CLOUD
Speaker: Peter Kourzanov, Delft University Of Technology, NL

REDUCING SIMULATION TESTING TIME BY PARALLEL EXECUTION OF LOOSELY-COUPLED SEGMENTS OF A TEST SCENARIO
Speakers: Md. Abdullah Al Mamun[1] and Jörgen Hansson
[1]Chalmers University of Technology, SE
[2]Högskolan i Skövde, SE

1430 **COFFEE BREAK**

1500 **SESSION 3**

SIMULATIONS ON CONSUMER TESTS: A PERSPECTIVE FOR DRIVER ASSISTANCE SYSTEMS
Speakers: Delf Block[1], Sönke Heeren[2], Stefan Kühnel[1], Andre Leschke[1], Bernhard Rumpe[3] and Vladislavs Serenbro[2]
[1]Volkswagen AG, DE
[2]Automotive Safety Technologies GmbH, DE
[3]RWTH Aachen University, DE

MODELING AND SIMULATION OF ENERGY-AWARE ADAPTIVE POLICIES FOR AUTOMATIC WEATHER STATIONS
Speakers: Daniel Cesarini, Luca Cassano, Alessio Fagioli and Marco Avvenuti
Dept. of Information Engineering - University of Pisa

1600 **FINAL DISCUSSION, CLOSING SESSION AND FINAL REMARKS**

W3 Electronic System-Level Design towards Heterogeneous Computing

Konferenz 3 0830 – 1700

Organisers:
Alessandro Cilardo, University of Naples Federico II, IT
David Thomas, Imperial College, GB

Heterogeneous computing has emerged as a new important trend in computer architecture and high-performance computing. It refers to systems combining a variety of different computational units, such as general-purpose processors, special-purpose units, i.e. digital signal processors or the graphics processing units (GPUs), co-processors, custom accelerators, typically implemented on field-programmable gate arrays (FPGAs). The heterogeneous computing paradigm is rapidly extending its range to the development of complex embedded systems, multi-processor systems on chip and, in general, application-specific custom machines. The inclusion of FPGAs as heterogeneous accelerators for HPC platforms, furthermore, is introducing new challenges related to programmability, abstraction and programming paradigms, as well as new opportunities for hardware-accelerated high-performance and scientific computing applications. In fact, there are currently a large number of ongoing research projects and industrial initiatives centered on heterogeneous computing. The workshop will offer a global view of this rich and diverse research scenario. Representing the perspectives of both academia and industry, the talks will particularly address important cross-cutting issues involving system-level and embedded design in the light of the emerging heterogeneous computing trends.

0830 **OPENING SESSION**

0845 **SESSION 1 TRENDS IN HETEROGENEOUS COMPUTING: THE INDUSTRIAL PERSPECTIVE**

0845 **HETEROGENEOUS COMPUTING IN THE CLOUD: EMERGING TRENDS FROM THE INDUSTRY**
Speaker: Steve Hebert, Nimbix

0915 **HIGHER LEVEL PROGRAMMING ABSTRACTIONS FOR FPGAS USING OPENCL**
Speaker: Bogdan Pasca, Altera European Technology Centre

0945 **PANEL 1**

0945 **INDUSTRY TRENDS: BRINGING DEDICATED HARDWARE ACCELERATION TO THE MARKET**
Panelists: Koen Bertels, Steve Hebert, Bogdan Pasca

1030 **COFFEE BREAK+POSTER SESSION 1**

1100 **SESSION 2 - RESEARCH CHALLENGES IN HETEROGENEOUS COMPUTING DESIGN FLOWS**

1100 **FPGA BASED ACCELERATORS FOR BIG DATA: POLYMORPHIC COMPUTING FOR BIG DATA**
Speaker: Koen Bertels, Delft University of Technology

1130 **MAPPING APPLICATIONS TO HETEROGENEOUS ACCELERATORS: TOOL FLOWS AND RUN-TIME SYSTEMS**
Speaker: Christian Plessl, University of Paderborn

1200 **LUNCH**

1300 **SESSION 3 -COMPILERS AND CODE OPTIMIZATION FOR HARDWARE-ACCELERATED PLATFORMS**

1300 **FROM SOFTWARE CODE TO HARDWARE: DIRECTIONS IN HIGH-LEVEL SYNTHESIS**
Speaker: Philippe Coussy, Université de Bretagne-Sud, Lab-STICC

1330 **POLYHEDRAL COMPILATION AND CODE TRANSFORMATIONS FOR HIGH-LEVEL SYNTHESIS**
Speaker: Louis-Noel Pouchet, University of California Los Angeles

1400 **SESSION 4 - TOWARDS HIGHER-LEVEL DESIGN APPROACHES**

1400 **CODESIGN WITH VERITY: BIDIRECTIONAL CONTROL-FLOW ACROSS THE FPGA-CPU DIVIDE**
Speaker: Eduardo Aguilar Peleaz, Imperial College

1430 **BORROWING HIGH-LEVEL PARADIGMS FROM PARALLEL COMPUTING: AN OPENMP-BASED DESIGN FLOW**
Speaker: Alessandro Cilardo, University of Naples Federico II

1500 **PANEL 2**

1500 **ESL FOR HETEROGENEOUS COMPUTING: ENVISAGING TOMORROW'S TOOL FLOWS**
Panelists: Philippe Coussy, Louis-Noel Pouchet, Eduardo Aguilar Peleaz

1530 **COFFEE BREAK + POSTER SESSION 2**

1600 **SESSION 5 - CURRENT AND EMERGING HETEROGENEOUS COMPUTING APPLICATIONS**

1600 **HETEROGENEOUS HPC: COMBINING FPGAS, CPUS, AND GPUS FOR FINANCIAL ANALYTICS**
Speaker: David Thomas, Imperial College

1630 **PANEL 3**

1630 **WHAT ROLE FOR DEDICATED HARDWARE ACCELERATION IN TOMORROW'S HIGH-PERFORMANCE AND SCIENTIFIC COMPUTING?**
Panelists: Alessandro Cilardo, Steve Hebert, Bogdan Pasca

1645 **CLOSING SESSION**

W4 Workshop on Design Automation for Understanding Hardware Designs

Konferenz 4 0830 – 1700

Technical PCs:
Lyes Benalycherif, ST Microelectronics, FR
Valeria Bertacco, University of Michigan, US
Raik Brinkmann, OneSpinSolutions GmbH, DE
Franco Fummi, Università degli Studi di Verona, IT
Masahiro Fujita, University of Tokyo, JP
Wenchao Li, University of California, US
Tun Li, National University of Defense Technology, CN

Organisers:
Emmanuelle Encrenaz-Tiphene, Université Pierre et Marie Curie, FR
Goerschwin Fey, German Aerospace Center, DE

Understanding a hardware design is tough. When entering a large team as a new member, when extending a legacy design, or when documenting a new design, a lack in understanding the details of a design is a major obstacle for productivity. In software engineering topics like software maintenance, software understanding, reverse engineering are well established in the research community and partially tackled by tools. In the hardware area the re-use of IP-blocks, the growing size of designs and design teams leads to similar problems. Understanding of hardware requires deep insight into concurrently operating units, optimizations to reduce the required area, and specially tailored functional units for a particular use. The workshop is of interest to practitioners working in circuit design and to researchers interested in design automation.

The aim of the 1st Workshop on Design Automation for Understanding Hardware Designs (DUHDe) is to establish a community for these topics in electronic design automation.

0830 **OPENING SESSION**
Chairs: Görschwin Fey, Emmanuelle Encrenaz-Tiphéne

0845 **INVITED TALK**
MANAGING DESIGN KNOWLEDGE FOR IP CORES – STATE-OF-THE-ART AND OPEN QUESTIONS
Speaker: Alexander Rath, Infineon Technologies AG, Munich, DE

0930 **TECHNICAL SESSION: FORMAL AND SEMI-FORMAL**

AUTOMATIC IDENTIFICATION OF LOGICAL RELATIONSHIPS AMONG INTERNAL SIGNALS WITH SMALL NUMBERS OF TEST VECTORS
Speakers: Masahiro Fujita, Takeshi Matsumoto and Satoshi Jo
University of Tokyo, JP

USING NATURAL LANGUAGE DOCUMENTATION IN THE FORMAL VERIFICATION OF HARDWARE DESIGNS
Speakers: Christopher Harris and Ian Harris
University of California, Irvine, US

UNDERSTANDING COMPOUND SYSTEMS FROM THEIR COMPONENTS' PROPERTIES
Speakers: Syed-Hussein Syed-Alwi and Emmanuelle Encrenaz
Université Pierre et Marie Curie Paris 6, FR

DESIGN UNDERSTANDING WITH FAST PROTOTYPING FROM ASSERTIONS
Speakers: Katell Morin-Allory, Fatemeh Javaheri and Dominique Borrione
Univ. Grenoble Alpes, Grenoble, FR

1030 **COFFEE BREAK & POSTER PRESENTATIONS**

DETECTING CONCURRENCY PROBLEMS IN SYSTEM LEVEL DESIGNS
Alper Sen and Onder Kalaci
Bogazici University, Istanbul, TR

AUTOMATICALLY CONNECTING HARDWARE BLOCKS VIA LIGHT-WEIGHT MATCHING TECHNIQUES
Jan Malburg[1], Niklas Krafczyk[1] and Goerschwin Fey[1,2]
[1]University of Bremen, Germany
[2]German Aerospace Center, Bremen, DE

EXACT SOLUTION FOR TRACE SIGNAL SELECTION WITH PSEUDO BOOLEAN OPTIMIZATION (PBO)
Shridhar Choudhary, Kousuke Oshima, Amir Masoud Gharehbaghi, Takeshi Matsumoto and Masahiro Fujita
The University of Tokyo, Tokyo, JP

1100 **INVITED TALK**

CAPTURING AND VALIDATING DESIGN UNDERSTANDING USING FORMAL PROPERTIES
Speaker: Raik Brinkmann
OneSpinSolutions GmbH, Munich, DE

1200 **LUNCH**

1300 **INVITED TALK**

DESIGN UNDERSTANDING IN SOC DEVELOPMENT - RECENT ADVANCES AND NEW CHALLENGES
Speaker: Lyes Benalycherif
ST Microelectronics, Grenoble, FR

1345 **TECHNICAL SESSION: SYSTEM LEVEL PRODUCTIVITY**

DIPLODOCUSDF: ANALYZING HARDWARE/SOFTWARE INTERACTIONS WITH A DINOSAUR
Speakers: Andrea Enrici, Ludovic Apvrille and Renaud Pacalet
Telecom ParisTech, Biot, FR

TOWARDS A MULTI-DIMENSIONAL AND DYNAMIC VISUALIZATION FOR ESL DESIGNS
Speakers: Jannis Stoppe[1], Marc Michael[2], Mathias Soeken[1,2], Robert Wille[1,2,3] and Rolf Drechsler[1,2]
[1]DFKI GmbH, Bremen, DE
[2]University of Bremen, Bremen, DE
[3]Technical University Dresden, DE

1415 **INVITED TALK**

SOFTWARE REVERSE ENGINEERING
Speaker: Rainer Koschke, University of Bremen, DE

1500 **COFFEE BREAK & POSTER PRESENTATIONS**

1530 **TECHNICAL SESSION: REVERSE AND AUTOMATIC ENGINEERING**

INCREASING VERILOG'S GENERATIVE POWER
Speakers: Cherif Salama[1] and Walid Taha[2]
[1]Ain Shams University, Cairo, EG
[2]Halmstad University, Halmstad, SE

ZAMIACAD: UNDERSTAND, DEVELOP AND DEBUG HARDWARE DESIGNS
Speakers: Maksim Jenihhin[1], Valentin Tihhomirov[1], Syed Saif Abrar[1], Jaan Raik[1] and Guenter Bartsch[2]
[1]Tallinn University of Technology, EE
[2]zamiaCAD, DE

MUTATION BASED FEATURE LOCALIZATION
Speakers: Jan Malburg[1], Emmanuelle Encrenaz-Tiphene[2] and Goerschwin Fey[1,3]
[1]University of Bremen, DE
[2]Université Pierre et Marie Curie Paris 6, FR
[3]German Aerospace Center, Bremen, DE

1615 **PANEL**

DESIGN UNDERSTANDING – WHERE DO INDUSTRY AND ACDEMIA TEAM UP?
Panelists: Ian Harris, Lyes Benalycherif, Raik Brinkmann

The panel will summarize the results of the day and prioritize topics focusing on three questions:
- What are the most urgent topics from an industrial perspective?
- What are the most challenging topics from an academic perspective?
- Where can we exploit synergies between academia and industry?

W5 3D Integration: Applications, Technology, Architecture, Design, Automation, and Test

Konferenz 5 0815 – 1630

Programme Chairs:
Pascal Vivet, CEA-LETI, FR
Fabian Hopsch, Fraunhofer IIS/EAS, DE

Panel Chair: **Rishad Shafik,** University of Southampton, GB

Publication Chair: **Bjorn B. Larsen,** NTNU, NO

Steering Committee Members:
Erik Jan Marinissen, IMEC, BE
Q. Xu, Chinese University of Hong Kong, HK

General Chair: **Saqib Khursheed,** University of Liverpool, GB

3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. But in order to produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges.

The last five editions of this workshop took place in conjunction with DATE:

- DATE 2009, Nice, France
  www.date-conference.com/date09/conference/workshop-W5
- DATE 2010, Dresden, Germany
  www.date-conference.com/date10/conference/workshop-W5
- DATE 2011, Grenoble, France
  www.date-conference.com/date11/conference/workshop-W5
- DATE 2012, Dresden, Germany
  www.date-conference.com/date12/conference/session/W5
- DATE 2013, Grenoble, France
  www.date-conference.com/date13/conference/workshop-W5

The workshop program contains the following elements:

- One invited keynote.
- One special session on Reliability and Thermal issues in 3D ICs.
- One panel session on Standardisation of 3D CAD tools.
- One invited talk.
- Two technical sessions with 10 regular presentations.
- Two poster sessions.

0815 **SESSION 1: OPENING**
Chair:Paul Franzon, North Carolina State University, US

0815 **WELCOME ADDRESS**
Speaker: Khursheed Saqib, U of Liverpool, GB

0820 **KEYNOTE PRESENTATION: 3D TECHNOLOGY APPLICATIONS MARKET TRENDS & KEY CHALLENGES**
Speaker: Thibault Buisson, Yole Développement, FR

0900 **SPECIAL SESSION: RELIABILITY AND THERMAL ISSUES IN 3D ICS**

0900 **OVERVIEW OF 3D-RELIABILITY RESEARCH IN IMEC**
Speaker: Kristof Croes, IMEC, BE

0920 **ADVANCED FAILURE ANALYSIS TECHNIQUES FOR 3D PACKAGES**
Speaker: Frank Altmann, Fraunhofer IWM Halle, DE

0940 **RESEARCH DIRECTIONS ON THERMAL IMPACT OF 3D ASSEMBLY**
Speaker: Haykel Ben Jaama, CEA-LETI, FR

1000 **SESSION 2: COFFEE BREAK & POSTERS**

1030 **SESSION 3: INVITED TALK AND PANEL**
Chair: Françoise Von Trapp, Queen of 3D, 3DInCites, US

1030 **INVITED TALK: HETEROGENEOUS SENSOR INTEGRATION; INCREASED TECHNOLOGY READINESS LEVEL**
Speaker: Maaike Visser, SINTEF, NO

1100 **ARE SLOW STANDARDIZATION AND CAD-TOOL DEVELOPMENT HINDERING THE PROGRESS OF 3D IC DESIGN AND INTEGRATION?**
Speakers: Brandon Wang[1], Ron Press[2], Makoto Nagata[3] and Mustafa Badaroglu[4]
[1]Cadence Design Systems, US
[2]Mentor Graphics, US
[3]Kobe University, JP
[4]Qualcomm Technologies, BE

1200 **LUNCH BREAK**

1300 **SESSION 4: TECHNOLOGY AND DESIGN CHALLENGES FOR 3D ICS**

1300 **INTEGRATION OF THROUGH-SILICON VIAS IN A HIGH PERFORMANCE BICMOS TECHNOLOGY FOR RF-GROUNDING AND 3D-INTEGRATION**
Speakers: M. Wietstruck[1], M. Kaynak[1], S. Marschmeyer[1], K. Zoschke[2] and B. Tillack[3]
[1]IHP, DE
[2]Fraunhofer IZM, DE
[3]IHP, Technische Universität Berlin, DE

1318 **2.5D & 3D TECHNOLOGIES REQUIRE INNOVATIVE LITHOGRAPHY SOLUTIONS**
Speakers: Klaus Ruhmer, Philippe Cochet and Roger McCleary, Rudolph Technologies, US

1336 **3D WIREBONDLESS IGBT MODULE FOR HIGH POWER APPLICATIONS**
Speakers: Z. Y. Gao[1], Y. X. Ren[1], Y.C. Lee[2] and X.Q. Shi[1]
[1]Hong Kong Applied Science & Technology Research Institute, HK
[2]Hong Kong Science & Technology Parks Corporation, HK

1354 **TOWARDS TRUSTWORTHY NOC-BASED 3D-MPSOCS**
Speakers: Johanna Sepúlveda[1], Guy Gogniat[2] and Marius Strum[1]
[1]University of São Paulo, BR
[2]LAB-STICC, Lorient, FR

1412 **A TSV-PROPERTY-AWARE SYNTHESIS METHOD FOR APPLICATION SPECIFIC 3D-NOCS**
Speakers: Felix Miller, Thomas Wild, Andreas Herkersdorf, Vladimir Todorov, Daniel Mueller-Gritschneder and Ulf Schlichtmann Technische Universität, München, DE

1430 **SESSION 5: COFFEE BREAK & POSTERS**

1500 **SESSION 6: TEST AND THERMAL CHALLENGES FOR 3D ICS**
Chair: Basel Halak, U. of Southampton, GB

1500 **DESIGN, TEST GENERATION, PROCESSING, AND PRE- AND POST-BOND MEASUREMENT RESULTS OF A 3D-DFT DEMONSTRATOR CHIP STACK**
Speakers: Erik Jan Marinissen[1], Bart De Wachter[1], Stephen O'Loughlin[1], Sergej Deutsch[2], Christos Papameletis[2] and Tobias Burgherr[3]
[1]IMEC, BE
[2]Cadence Design Systems, DE
[3]Cadence Design Systems, US

1518 **POWER AND DFT AWARE PARTITIONING FOR 3D-SOCS**
Speakers: Amit Kumar and Sudhakar M. Reddy
University of Iowa, US

1536 **SYSTEM LEVEL THERMAL MODELLING FOR 3D IC: A MEMORY-ON-LOGIC 3D TEST CASE STUDY**
Speakers: Cristiano Santos[1], Pascal Vivet[2], Denis Dutoit[2], Philippe Garrault[3], Nicolas Peltier[3] and Ricardo Reis[4]
[1]CEA-LETI, UFRGS, FR
[2]CEA-LETI, FR
[3]DOCEA-Power, FR
[4]UFRGS, BR

1554 **THERMAL POWER PLANE ENABLING DUAL-SIDE ELECTRICAL INTERCONNECTS SUPPORTING HIGH-PERFORMANCE CHIP STACKING**
Speakers: Thomas Brunschwiler[1], Stefano Oggioni[2], Timo Tick[1], Gerd Schlottig[1] and Hubert Harrer[3]
[1]IBM Research, Zurich, CH
[2]IBM ISC, Milan, IT
[3]Böblingen, DE

1612 **THERMAL COUPLING IN TSV-BASED 3-D INTEGRATED CIRCUITS**
Speakers: Ioannis Savidis[1] and Eby G. Friedman[2]
[1]Drexel University, US
[2]University of Rochester, US

W6 MEDIAN - Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale

Konferenz 6 0830 – 1630

General Co-Chairs:
Mehdi Tahoori, Karlsruhe Institute of Technology, DE
Oliver Bringmann, FZI/University of Tuebingen, DE

Program Co-Chairs:
Maria K. Michael, University of Cyprus, CY
Ozcan Ozturk, Bilkent University, TR

Panel Session Chair:
Said Hamidioui, Delft University of Technology, NL

Submissions Chair:
Michael Skitsas, University of Cyprus, CY

Constant advances in manufacturing yield and field reliability are important enabling factors for electronic devices pervading our lives, from medical to consumer electronics, from railways to the automotive and avionics scenarios. At the same time, both technology and architectures are today at a turning point; many ideas are being proposed to postpone the end of Moore's law such as extending CMOS technology as well as finding alternatives to it like CNTFET, QCA, memristors, etc., while at the architectural level, the spin towards higher frequencies and aggressive dynamic instruction scheduling has been replaced by the trend of including many simpler cores on a single die. These paradigm shifts imply new dependability issues and thus require a rethinking of design, manufacturing, testing, and validation of reliable next-generation systems. These manufacturability and dependability issues will be resolved efficiently only if a cross-layer approach that takes into account technology, circuit and architectural aspects will be developed.

This workshop will provide an open forum for presentations in the above-mentioned fields. The topics include (but are not limited to) the following ones:

- Methodologies/techniques for manufacturing reliable nanoscale devices
- System level design, on-line testing/fault tolerance
- Dependability Evaluation and Validation/Debug Methodologies
- Fault tolerance for space applications
- Fault tolerance for transportation systems
- Fault tolerance for medical devices

0830 **OPENING SESSION**
General Chairs: Oliver Bringmann, FZI/University of Tuebingen, DE, Mehdi Tahoori, Karlsruhe Institute of Technology, DE
Programme Chairs: Maria K Michael, University of Cyprus, CY, Ozcan Ozturk, Bilkent University, TR

0845 **WELCOMING COMMENTS**

KEYNOTE TALK

DESIGNING EFFICIENT AND RELIABLE MULTICORE PROCESSORS FOR NETWORKING, SERVERS, AND BEYOND
Speaker: Shubu Mukherjee, Cavium Networks, US

0945 **PAPER SESSION I: NEW CHALLENGES AT THE SYSTEM LEVEL**

MULTI-CORE EMULATION FOR DEPENDABLE AND ADAPTIVE SYSTEMS PROTOTYPING
Speakers: Cristiana Bolchini and Matteo Carminati
Politecnico di Milano, IT

FAULT-TOLERANT ROUTING APPROACH FOR 3D STACKED MESHES
Speakers: Masoumeh Ebrahimi, Masoud Daneshtalab and Juha Plosila
University of Turku, FI

1030 **COFFEE BREAK**

1100 **PAPER SESSION II: RELIABILITY THREADS IN NEW TECHNOLOGIES**

INVITED TALK - STEEP SLOPE DEVICES: OPPORTUNITIES AND CHALLENGES FOR PROCESSOR DESIGN
Speaker: Vijaykrishnan Narayanan, Penn State, US

BTI RELIABILITY FROM PLANAR TO FINFET NODES: WILL THE NEXT NODE BE MORE OR LESS RELIABLE?
Speakers: Halil Kukner[1], Pieter Weckx[2], Praveen Raghavan[1], Ben Kaczer[1], Doyoung Jang[1], Francky Catthoor[3], Liesbet Van der Perre[2], Rudy Lauwereins[3] and Guido Groeseneken[3]
[1]IMEC, BE
[2]KU Leuven, BE
[3]IMEC, KU Leuven, BE

ANALYSIS OF RANDOM DOPANT FLUCTUATIONS AND OXIDE THICKNESS ON A 16NM L1 CACHE DESIGN*
Speakers: Cargi Erylmaz[1,2], Azam Seyedi[2,3], Ozman Unsal[2], Andrian Cristal[2,3,4]
[1]Middle Eastern Technical University, TR
[2]Barcelona Supercomputing Center, ES
[3]Universitat Politecnica de Catalunya, ES
[4]IIIA-CSIC, ES

1200 **LUNCH BREAK**

1300 **PAPER SESSION III: APPLICATION SPECIFIC SOLUTIONS**

FPGA DEFECT TOLERANCE BASED ON EQUIVALENT CONFIGURATIONS GENERATION
Speakers: Parthasarathy M. B. Rao, Abdulazim Amouri and Mehdi B. Tahoori
Karlsruhe Institute of Technology, DE

A COMPLEX CONTROL SYSTEM FOR TESTING FAULT-TOLERANCE METHODOLOGIES*
Speakers: Jakub Podivinsky, Marcela Simkova and Zdenek Kotasek
Brno University of Technology, CZ

1330 **PANEL SESSION**
Organiser: Said Hamdioui, TU Delft, NL
Chair: Matteo Sonza Reorda, Politecnico di Torino, IT

1330 **HARDWARE V SOFTWARE ENGINEERING: WHOSE RESPONSIBILITY IS THE REALIZATION OF FUTURE RELIABLE COMPUTER SYSTEMS?**
Speakers:Mehdi Tahoori[1], Oliver Bringmann[2], Adrian Evans[3] and Viacheslav Izosimov[4]
[1]Karlsruhe Institute of Technology, DE
[2]FZI/University of Tuebingen, DE
[3]Adrian Evans, iROC, FR
[4]Viacheslav Izosimov, Semcon, SE

1430 **COFFEE BREAK & POSTER SESSION**

1430 **BADR: BOOSTING RELIABILITY THROUGH DYNAMIC REDUNDANCY**
Speakers: Ihsen Alouani[1], Smail Niar[1], Mazen Saghir[2] and Fadi Kurdahi[3]
[1]University of Valenciennes, FR
[2]Texas A&M University, US
[3]University of California Irvine, US

AUTOMATIC DETECTION AND CORRECTION OF DEFECTIVE PIXELS FOR MEDICAL AND SPACE IMAGERS
Speakers: Eliahu Cohen[1], Moriel Shnitser[2], Tsvika Avraham[2], Ofer Hadar[2], Yocheved Dotan[3]
[1]Tel-Aviv University, IL
[2]Ben-Gurion University, IL
[3]Ruppin Academic Center, IL

IMPLEMENTING DOUBLE ERROR CORRECTION ORTHOGONAL LATIN SQUARES CODES IN XILINX FPGAS
Speakers: Mustafa Demirci[1], Pedro Reviriego[2] and Juan Antonio Maestro[2]
[1]Alesan, TR
[2]Universidad Antonio de Nebrija, ES

ON RELIABILITY ENHANCEMENT USING ADAPTIVE CORE VOLTAGE SCALING AND VARIATIONS ON TSMC 28NM LP PROCESS PROCESS FPGAS
Speakers: Petr Pfeifer and Zdenek Pliva
Technical University of Liberec, CZ

POWER AND PERFORMANCE OPTIMIZATION IN LONG-TERM OPERATION
Speakers: André Romão[1], Jorge Semião[1], Carlos Leong[2], Marcelino Santos[3], Isabel Teixeira[3] and Paulo Teixeira[3]
[1]University of Algarve, PT
[2]INESC-ID, PT
[3]Technical University of Lisbon, PT

1500 **PAPER SESSION IV: RESILIENCY, SELF-TEST AND SELF-DIAGNOSIS**

1500 **INVITED TALK - DEEP-ER: SCALABLE RESILIENCY IN EXASCALE COMPUTING**
Speaker: Michael Kauschke, Intel, DE

FRIDAY

1500 **IMPROVING THE RELIABILITY OF SKEWED CACHES THROUGH ECC BASED HASHES**
Speakers: Sercan Yegin[1], Burak Karsli[1], Oguz Ergin[1], Marco Ottavi[2], Salvatore Pontarelli[2] and Pedro Reviriego[3]
[1]TOBB University, TR
[2]University of Rome Tor Vergata, IT
[3]Universidad Antonio de Nebrija, ES

1500 **A NEW DIAGNOSTIC METHOD FOR VLIW PROCESSORS***
Speakers: Davide Sabena, Luca Sterpone and Matteo Sonza Reorda
Politecnico di Torino, IT

1500 **AGING MONITORING METHODOLOGY FOR BUILT-IN SELF-TEST APPLICATIONS***
Speakers: João Coelho[1], Jorge Semião[1], Carlos Leong[2], Marcelino Santos[3], Isabel Teixeira[3] and Paulo Teixeira[3]
[1]University of Algarve, PT
[2]INESC-ID, PT
[3]Technical University of Lisbon, PT

1615 **CLOSING SESSION**

* indicates short paper

www.date-conference.com

W7 Memristor Science & Technology

Seminar 5+6 0830 – 1700

Organisers:
Ronald Tetzlaff, Technische Universität Dresden, DE
Fernando Corinto, Politecnico di Torino, IT

Programme Chairs:
Alon Ascoli, Technische Universität Dresden, DE
Sandro Carrara, EPFL, CH

Conventional computing, including both hardware platforms and computer languages, seems to be close to its physical limits in terms of speed and data density. Classical Von Neumann architectures are known to be great in number crunching; nevertheless, they struggle with tasks like face recognition, real-time navigation control, object segmentation and depth perception. On top of that, CMOS technologies are also approaching the nano-scale floor, with devices attaining comparable dimensions to their constituting atoms, imposing significant challenges on the performance and reliability of analogue and digital circuits hindering the well-exploited correlation of Moore's law with computation capacity.

Memristors were first conjectured based on the missing constitutive link between flux and charge by Leon Chua as published in his seminal paper in 1971, which was further extended by L. O. Chua and S. M. Kang in their 1976 paper on memristive devices and systems. Recently, a physical realization of memristors was reported in Nature by HP's Stan Williams team in 2008. To date, memristor represents the latest technology breakthrough to build electronics devices with characteristics that show an intriguing resemblance to the brain's synapses.

The One-day Workshop on "Memristor Science & Technology" is organized in plenary talks, Positions papers and sessions with selected and invited contributions.

The One-day Workshop on "Memristor Science & Technology" will be a multidisciplinary forum for researches and industrial companies to present the latest advances in the field of memristor circuits and their latest breakthrough applications.

0830 **OPENING SESSION**
Chair: Fernando Corinto, Politecnico di Torino, IT
Co-Chair: Ronald Tetzlaff, Technische Universität Dresden, DE

0845 **INVITED TALK BY PROF. L. O. CHUA**

MEMRISTOR: STATE-OF-THE-ART
Speaker:L. O. Chua

0945 **INVITED TALK BY DR. S. WILLIAMS**

1045 **COFFEE BREAK**

1115 **INVITED TALK BY DR. THOMAS MIKOLAJICK**

1115 **RESISTIVE SWITCHING - FROM BASIC SWITCHING MECHANISM TO DEVICE APPLICATIONS**
Speakers: T. Mikolajick, H. Mähne, H. Wylezich and S. Slesazeck

1200 **LUNCH**

1300 **SESSION 1**

THE ART OF SPICE MODELING OF MEMRISTIVE SYSTEMS
Speaker: Dalibor Biolek

MODELING AND SIMULATION OF MEMRISTIVE DEVICES FOR MEMORY AND LOGIC APPLICATIONS
Speakers: Stephan Menzel and Rainer Waser

MEMORY INTENSIVE COMPUTING
Speaker: Shahar Kvatinski
Technion – Israel Institute of Technology, IL

1500 **SESSION 2**

MULTI-FUNCTIONAL SPINTRONIC AND FERROELECTRIC NANODEVICES FOR NEUROMORPHIC COMPUTING
Speaker: Julie Grollier

IS MEMRISTOR THE 4TH CIRCUIT ELEMENT?
Speaker: Frank Zhigang Wang

A GENERAL MODEL OF MEMRISTORS BASED ON CHUA'S UNFOLDING CONCEPT FOR TIME-EFFICIENT CIRCUIT SIMULATIONS
Speakers: Ronald Tetzlaff and Alon Ascoli

PATTERN CLASSIFICATION AND RECOGNITION WITH MEMRISTIVE CIRCUITS
Speakers: F. Alibart and D. B. Strukov

MEMRISTOR CROSSBAR ARRAY CIRCUITS FOR NEUROMORPHIC APPLICATIONS
Speaker: Kyeong-Sik Min

1640 **CLOSING SESSION**

W8 3PMCES - Performance, Power and Predictability of Many-Core Embedded Systems

Seminar 3+4 0830 – 1700

Organizing Committee Members:
Tapani Ahonen, Technoconsult (TC) and
Tampere University of Technology (TUT), FI
Mats Brorsson, KTH and Swedish Institute of Computer Science (SICS), SE
Sven Karlsson, DTU, DK
Adam Morawiec, ECSI, FR
Walter Stechele, Technical University of Munich (TUM), DE

The scope of the workshop is to address challenges of embedded portable software development on multi-core structures related to various performance aspects, power efficiency, correctness and reliability including aging.

The workshop will present the current state of these efforts, achieved results so far, and will devise future ways of potential further enhancements. It will address key challenges in the provision of integrated solutions, including secure, reliable, and timely operations, back-annotation based forward system governance, tool-tool, tool-middleware, and middleware-hardware exchange interfaces, and energy management with minimal run-time overhead.

Besides conceptual solutions, it will give an overview of practical in-field experiments on real industry projects provided for "seamless connectivity and middleware" by realizing a common middleware layer that is designed to support new wireless communication standards, while being portable across different platforms. It will also demonstrate some of the developed tools and preliminary results achieved in three European projects: CRAFTERS (www.crafters-project.org), PaPP (www.papp-project.eu) and RELY (www.rely-project.eu). We will discuss the experiences from working with the tools on industrial applications.

0830 **OPENING SESSION**

0845 **KEYNOTE PRESENTATION**

TRUSTWORTHY CONTRACT COMPUTING THROUGH SEAMLESS SYSTEM BUILD AND OPERATION
Tapani Ahonen, Tampere University of Technology, FI

0930 **SESSION 1**

PREDICTABLE PORTABILITY OF PARALLEL CODE BASED ON INCREASED SEMANTIC INFORMATION SHARING AND FORK-JOIN PROGRAMMING
Konstantin Popov, SICS Swedish ICT AB, SE

1000 **SESSION 2: MANAGING EXECUTION IN DYNAMIC ENVIRONMENT**

EFFICIENT LEADER ELECTION FOR SYNCHRONOUS SHARED-MEMORY SYSTEMS
Speakers: Vicent Sanz Marco[1], Raimund Kirner[1], Michael Zolda[1], Guoqing Zhang[2], Tapani Ahonen[2], Nilesh Karavadara[3], Simon Folie[3], Michael Zolda[3], Nga Nguyen[3] and Raimund Kirner[3]
[1]University of Hertfordshire, UK
[2]Tampere University of Technology, FI
[3]University of Hertfordshire, UK

A PROPOSAL ON PARALLEL SOFTWARE DEVELOPMENT FOR NETWORK-ON-CHIP BASED MANY-CORE SYSTEM (short paper)
Speakers: Guoqing Zhang and Tapani Ahonen

A POWER-AWARE FRAMEWORK FOR EXECUTING STREAMING PROGRAMS ON NETWORKS-ON-CHIP (short paper)
Speakers: Nilesh Karavadara, Simon Folie, Michael Zolda, Nga Nguyen and Raimund Kirner

1100 **COFFEE BREAK & POSTER SESSION**

1130 **INVITED TALK**

1130 **PERFORMANCE PREDICTION AND SOFTWARE DEVELOPMENT ON MANY-CORE PROCESSOR PLATFORM**
Speaker: Benoit Dupont de Dinechin, Kalray, FR

1200 **LUNCH AND POSTER SESSION**

1300 **SESSION 3: RELIABILITY AND SAFETY OF MULTI-CORE PLATFORMS**

HARDWARE/SOFTWARE-BASED RUNTIME CONTROL OF MULTICORE PROCESSORS-ON-CHIP FOR RELIABILITY MANAGEMENT UNDER AGING CONSTRAINTS
Speakers: Walter Stechele and Erol Koser, Technical University Munich, DE

1300 **MPSOC PERFORMANCE DEGRADATION (DUE TO AGING) PREDICTABILITY AT HIGH ABSTRACTION LEVEL AND APPLICATIONS**
Speaker: Olivier Heron, CEA-LIST, FR

1400 **SESSION 4: EUROPEAN PROJECTS CLUSTER**

EUROPEAN PROJECT CLUSTER ON MIXED-CRITICALITY SYSTEMS
Speakers: Salvador Trujillo (IK4-IKERLAN, ES), Roman Obermaisser (University of Siegen, DE), Kim Gruettner (OFFIS – Institute for Information Technology, DE), Francisco J. Cazorla (Barcelona Supercomputing Center and IIIA-CSIC, ES), and Jon Perez (IK4-IKERLAN, ES)

1430 **COFFEE BREAK & POSTER SESSION**

1500 **SESSION 5: SYSTEM DESIGN TECHNOLOGIES**

TIMING ANALYSIS OF A HETEROGENEOUS ARCHITECTURE WITH MASSIVELY PARALLEL PROCESSOR ARRAYS
Speakers: Deepak Gangadharan, Alexandru Tanase, Frank Hannig, and Jürgen Teich, University of Erlangen, Nuremberg, DE

AN ACCURATE POWER ESTIMATION METHOD FOR MPSOC BASED ON SYSTEMC VIRTUAL PROTOTYPING
Speaker: Khouloud Zine Elabidine

PARALLELIZATION OF OBJECT DETECTION ALGORITHM THROUGH HARDWARE THREADS FOR MPSOCS
Speakers: David Watson, Ali Ahmadinia, Gordon Morison, and Tom Buggy, Glasgow Caledonian University, UK

1600

PANEL SESSION
Chair: Achim Rettberg, OFFIS, DE

WHAT IS STILL NEEDED TO HAVE A RELIABLE EMBEDDED SYSTEM DEVELOPMENT ECOSYSTEM IN PLACE?
Speakers: Sven Karlsson[1], Tapani Ahonen[2], Kim Grüttner[3], Benoit Dupont de Dinechin[4] and Walter Stechele[5]
[1]DTU, DK
[2]TUT, FI
[3]OFFIS, DE
[4]Kalray, FR
[5]TU Munich, DE

1645

CLOSING SESSION

POSTER PRESENTATIONS

ADAPTIVE RESOURCE CONTROL IN MULTI-CORE SYSTEMS
Alexei Iliasov, Ashur Rafiev, Alexander Romanovsky, Andrey Mokhov, Alex Yakovlev, and Fei Xia, Newcastle University, UK

CRITICALITY-AWARE FUNCTIONALITY ALLOCATION FOR DISTRIBUTED MULTICORE REAL-TIME SYSTEMS
Junhe Gan, Paul Pop, and Jan Madsen, Technical University of Denmark, DK

ESTIMATING VIDEO DECODING ENERGIES AND PROCESSING TIMES UTILIZING VIRTUAL HARDWARE
Sebastian Berschneider, Christian Herglotz, Marc Reichenbach, Dietmar Fey, and André Kaup, Friedrich-Alexander-University Erlangen-Nuremberg, DE

INCREASED RELIABILITY OF MANY-CORE PLATFORMS THROUGH THERMAL FEEDBACK CONTROL
Matthias Becker, Kristian Sandström, Moris Behnam, and Thomas Nolte, MRTC / Mälardalen University, SE

PERFORMANCE ANALYSIS OF A COMPUTER VISION APPLICATION WITH THE STHORM OPENCL SDK
Vítor Schwambach, Sébastien Cleyet-Merle, Alain Issard, STMicroelectronics, FR and Stéphane Mancini, TIMA lab, FR

PSE - PERFORMANCE SIMULATION ENVIRONMENT
Jussi Hanhirova and Vesa Hirvisalo, Aalto University, FI

SCALING PERFORMANCE OF FFT COMPUTATION ON AN INDUSTRIAL INTEGRATED GPU CO-PROCESSOR: EXPERIMENTS WITH ALGORITHM ADAPTATION.
Mohamed Amine Bergach and Serge Tissot, Kontron, FR, Michel Syska and Robert De Simone, Inria, FR

SMART SCHEDULING OF STREAMING APPLICATIONS VIA TIMED AUTOMATA
Waheed Ahmad, Robert de Groote, Philip K.F. Hölzenspies, Mariëlle Stoelinga, and Jaco van de Pol, University of Twente, NL

SYSTEM LEVEL DESIGN FRAMEWORK FOR MANY-CORE ARCHITECTURES
Pablo Peñil, Luis Diaz, and Pablo Sanchez, University of Cantabria, ES

vendor exhibition

DATE 14 Exhibition:

Company	Booth
3D InCites, LLC	K 2
ALMA - ALgorithm parallelization for Multicore Architectures	EP 6
Blue Pearl Software	24
Center for Advancing Electronics Dresden (cfaed)	4+5
City of Dresden, Office of Economic Development	13
CLERECO – Cross-Layer Early Reliability Evaluation for the Computing cOntinuum	EP 4
CMP: Circuits Multi-Projects	17
Codasip	7
Concept Engineering GmbH	11
CONTREX	EP 1
CREATIVE CHIPS GmbH	19
Dream Chip Technologies GmbH	TP 2
DREAMS	EP 1
EDA Confidential	K 3
EDA Solutions LTD	20
Elektronik i Norden	K 4
Elsevier BV	10
Embedded Computing Specialists	2
European Project Cluster on Mixed-Criticality Systems (DREAMS, PROXIMA, CONTREX, MultiPARTES)	EP 1
EUROPRACTICE	1
EuroTraining – Training in Nanoelectronics	EP 2
FlexTiles Consortium	EP 5
Fraunhofer EMFT	TP 3
Fraunhofer Institute for Integrated Circuits IIS	12
Incentia	20
Methodics	15
Micronews Media, powered by Yole Développement	K 1
MOSIS	20
MultiPARTES	EP 1
MunEDA GmbH	14
now publishers inc.	27
OneSpin Solutions GmbH	26
ProPlus Design Solutions, Inc.	9
PROXIMA	EP 1
RacyICs GmbH	TP 1
SFB HAEC (TU Dresden)	6
SGS INSTITUT FRESENIUS GmbH	13
Silicon Saxony e.V.	13
SPRINGER	22+23
Synflow	8
Tanner EDA	20
TOSHIBA	16
University Booth	3
WIBRATE – Wireless, Self-Powered Vibration Monitoring and Control for Complex Industrial Systems	EP 3
Wirtschaftsförderung Sachsen GmbH (WFS)	13
X-FAB Group	13
Zentrum Mikroelektronik Dresden AG	13 & TP 4

fringe technical meetings

A number of specialist interest groups will be holding their meetings at DATE 2014. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage **www.date-conference.com**

Day+Time	Meeting & Contact	Room
Mon 1900-2100	**ACM SIGDA/EDAA PhD Forum** Peter Marwedel, EDAA/ACM SIGDA, DE <peter.marwedel@tu-dortmund.de>	Saal 1
Tue 1300-1430	**eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)** Giorgio Di Natale, LIRMM, FR <giorgio.dinatale@lirmm.fr>	Seminar 3
Tue 1830-1930	**EDAA General Assembly** Georges Gielen, Katholieke Universiteit Leuven, BE <Georges.Gielen@kuleuven.be>	Seminar 2
Tue 1830-2000	**IFIP Working Group 10.5** Dominique Borrione, IMAG, FR <Dominique.Borrione@imag.fr>	Seminar 4
Tue 1830-2030	**IFIP Working Group 10.2** Achim Rettberg, University of Oldenburg, DE <achim.rettberg@iess.org>	Seminar 5
Thu 1230-1400	**DATE Sister-Events Meeting** Georges Gielen, Katholieke Universiteit Leuven, BE <Georges.Gielen@kuleuven.be>	Seminar 5

ACM SIGDA/EDAA PhD Forum

Monday, March 24, 2014, 1900-2100, Saal 1

Organiser: Peter Marwedel, EDAA/ACM SIGDA, DE

The ACM SIGDA/EDAA PhD Forum at the Design, Automation and Test in Europe (DATE) Conference is a poster session and a buffet dinner organised and hosted by ACM SIGDA and the European Design and Automation Association (EDAA).

The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

More information is available on the web **www.date-conference.com**

university booth demonstrations

DATE 2014 will feature the University Booth within the **exhibition area at booth 3** where system and VLSI CAD tools developed in universities and research institutes are demonstrated as well as circuits in their working environment. This provides an alternative and more direct way of communicating CAD research results and displaying working silicon to the interested specialists. A rotating schedule will operate throughout the three days. Access to the exhibition area is free of charge. Please find detailed information and the online programme at the DATE website
www.date-conference.com/group/exhibition/u-booth.

Contacts: Jens Lienig and Andreas Vörg
university-booth@date-conference.com

exhibition programme

EXHIBITION THEATRE

Organiser: **Juergen Haase,** edacentrum, DE

In addition to the conference programme during DATE 14, there will be a presentation theatre from Tuesday 25 March, to Thursday 27 March, 2014. Attendees will profit from having an industry forum in the midst of Europe's leading electronic systems design event. The theatre is located in the exhibition area on the Terrace Level and affords easy access for exhibition visitors as well as for conference delegates.

Like in previous years, seven Special Sessions from the conference programme (track 8, full details are contained in the main conference programme pages, see p. 12) will take place in the Exhibition Theatre. These sessions are open to conference delegates as well as to exhibition visitors and are as follows:

exhibition theatre

2.8	SPECIAL SESSION - Hot Topic Technology Transfer towards Horizon 2020	Tuesday 1130 - 1300
3.8	SPECIAL SESSION - Hot Topic Mission Profile Aware Design – The Solution for Successful Design of Tomorrows Automotive Electronics	Tuesday 1430 - 1600
4.8	EXHIBITION SESSION State-of-the-art in Verification: European Tertulia IC Design - Enabling AMS Structured Verification / Verification in FPGA & IP design flows	Tuesday 1700 - 1830
5.8	SPECIAL SESSION - System Integration - The Bridge between More than Moore and More Moore	Wednesday 0830 - 1000
6.8	EXHIBITION SESSION - First Time Right in Analog Design Enabling New Business Cases	Wednesday 1100 - 1230
7.8	EXHIBITION SESSION - FD-SOI - the Enabling European Technology for Energy Efficient Solutions - Creating a Solution Hive & Design Hub as Eco-System for Future Success	Wednesday 1430 - 1600
8.8	SPECIAL SESSION - Hot Topic Beyond CMOS Ultra-low-power Computing	Wednesday 1700 - 1830
9.8	SPECIAL SESSION - Embedded Tutorial Memcomputing the Cape of Good Hope	Thursday 0830 - 1000
10.8	EXHIBITION PANEL - EDA+3D+MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics	Thursday 1100 - 1230
11.8	SPECIAL SESSION - Embedded Tutorial GPGPUs how to combine high computational power with high reliability	Thursday 1400 - 1530
12.8	SPECIAL SESSION - Panel Future SoC verification methodology UVM evolution or revolution?	Thursday 1600 - 1730

There will be an Exhibition Theatre Panel on the innovation chain: 3D and MEMS technologies – EDA - applications.

In three special Exhibition Theatre Sessions DATE 14 Exhibitors will highlight three parts of the value chain: a new European technology, verification as major design task and new business cases. They will discuss leading-edge approaches for verification of analog/mixed signal, FPGA and IP designs, how to enable new business cases for analog designs and how the European technology FD-SOI enables energy efficient solutions.

Please see presented overleaf information on the Exhibition Theatre Panel and on the Exhibition Theatre Sessions. The full programme with all the details of the exhibition sessions is available on the DATE web portal.

Exhibition Sessions

4.8 Exhibition Session — Tuesday, March 25, 1700 - 1830

State-of-the-art in Verification: European Tertulia IC Design - Enabling AMS Structured Verification/ Verification in FPGA & IP design flows

Details to be announced.

6.8 Exhibition Session — Wednesday, March 26, 1100 - 1230

First Time Right in Analog Design Enabling New Business Cases

Details to be announced.

7.8 Exhibition Session — Wednesday, March 26, 1430 - 160

FD-SOI - the Enabling European Technology for Energy Efficient Solutions - Creating a Solution Hive & Design Hub as Eco-System for Future Success

Details to be announced.

10.8 Exhibition Panel — Thursday, March 27, 1100 - 1230

EDA+3D+MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics

Organiser: **Juergen Haase,** edacentrum, DE
Moderator: **Ahmed Jerraya,** CEA-LETI, FR
Panellists: **Brent Gregory,** Synopsys, US
Gabriel Kittler, X-FAB, DE
Horst Symanzik, Bosch-Sensortec GmbH, DE
Gerd Teepe, GLOBALFOUNDRIES, DE
Brandon Wang, Cadence, US

Today the most powerful innovations in the major industries and the most promising approaches to tackle burning societal challenges are substantially influenced by and depending from the innovations provided by the microelectronics industry. Breakthroughs in manufacturing technologies enable the realization of novel types of devices and of systems, which enable applications with fascinating functionality and enormous performance. However, this innovation chain is not operational without appropriate innovations in design technology: We need an innovation Agenda 2020 for design methodology and EDA tools fueling the innovation chain of electronics.

2014 the technologies for MEMS and for 3D chips have reached a maturity level that enables them to reshape our lives until 2020. This panel will discuss how to utilize these technologies: Which applications will become possible with the upcoming innovations in 3D and MEMS technologies, what kind of EDA innovations will be required in order to be able to implement these applications effectively and efficiently, yielding powerful yet reliable components and systems.

The set-up of the panel includes the manufacturers GLOBALFOUNDRIES and X-FAB, Bosch as leading supplier of technology and one of the MEMS pioneers as well as leading EDA vendors Cadence and Synopsys.

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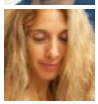

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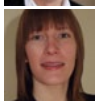

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D1 System Specifications, Models, and Methodologies

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D2 System Design, Synthesis and Optimization

Chair: Luciano Lavagno,
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Co-Chair: Frédéric Pétrot,
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D3 Simulation and Validation

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D4 Design for power, variability and aging

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D5 Power Estimation and Optimization

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Chair: Ayse Coskun,
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technical programme topic chairs

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T2 Test Generation, Simulation, Diagnosis and System Test

Chair: Grzegorz Mrugalski,
Mentor Graphics Poland, PL
Co-Chair: Bernd Becker,
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T3 Test for Mixed-Signal, Analog, RF, MEMS/bioMEMS/MOEMS

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T4 Design-for-Test, Test Compression, Test Access

Chair: Rohit Kapur,
Synopsys, US
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Politecnico di Torino, IT

T5 On-Line Test, Fault Tolerance and Reliable System Design

Chair: Lorena Anghel,
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Chair: Oliver Bringmann,
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TU Eindhoven, NL

E5 Cyber-Physical Systems

Chair: Anuradha Annaswamy,
MIT, US
Co-Chair: Rolf Ernst,
TU Braunschweig, DE

NOTES

DATE 15

Conference & Exhibition

March 09–13, 2015 • Grenoble, France

CALL FOR PAPERS

Scope of the Event

The 18th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of- the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical and Healthcare Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems
- Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles
- Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by **Sunday, September 14, 2014** via: www.date-conference.com
Papers can be submitted either for standard oral presentation or for interactive presentation.
The Programme Committee also encourages proposal submissions for Special Sessions, Tutorials and Friday Workshops as well as submissions for the Special Days on "Designing Electronics for the Internet of Things" and "Designing Electronics for Medical Applications"

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