event guide

DATE 14

ICC, Dresden, Germany

Event 24–28 March Exhibition 25–27 March

Design, Automation & Test in Europe

The European System Design Show

From Systems-on-Chip to Embedded Computing




www.date-conference.com

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DATE 14

Contents

Welcome to DATE 14

On behalf of the whole Organising Committee, we thank you very much for visiting DATE 2014 and are happy to welcoming you in the beautiful city of Dresden, Germany!
This event guide provides all relevant information concerning the DATE 2014 accompanying exhibition, a programme outline as well as venue and floor plans for your orientation.
All participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

The Exhibition Visit is free of charge.

Exhibition visitors have free access to the exhibition area, the opening keynote lectures and the Exhibition Theatre Programme.

OPENING PLENARY KEYNOTES:

Tuesday, March 25, 2014, 0830 – 1030, Grosser Saal, Saal Level

Exhibition Opening Times:

Tuesday, March 25	1000 – 1830*
Wednesday, March 26	1000 – 1800
Thursday, March 27	1000 – 1700

*Exhibition Reception from 1830 to 1930 in the exhibition area on the Terrace Level

DATE 2014 Event Secretariat

c/o K.I.T. Group GmbH Dresden
Muenzgasse 2
01067 Dresden, Germany
Phone: +49 351 4967 541
Fax: +49 351 4956 116
Email: date14@kit-group.org

Exhibition Manager:

Franziska Kremling
K.I.T. Group GmbH, DE
Phone: +49 351 4967 541

Registration & Accommodation

Eva Schubert
K.I.T. Group GmbH, DE
Phone: +49 351 4967 312

www.date-conference.com

The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in the editorial pages. Listed below are the media houses and publications who generously agree to media partnership with DATE, and whose publications can be found on-site near the Press Lounge on the Conference Level.

3D InCites

First launched in 2009, 3D InCites is a community platform that is the only online resource devoted exclusively to 2.5D and 3D integration technologies. 3D InCites is a resource for industry news, technology innovation, market analysis and opinion. As such, it provides a place to learn, share, engage and collaborate with fellow 2.5D and 3D enthusiasts. For 3D IC integration to happen requires open collaboration across the supply chain. Therefore, 3D InCites strives to inform key decision makers about progress in technology development, design, standards, and infrastructure in order to realize commercial production of 2.5D and 3D technologies. 3D InCites has grown to a registered membership of over 1300 with many additional visitors who stop by just to keep up with what's happening in the world of 3D.

www.3DinCites.com

EDA Confidential

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes "Recipes", Freddy Santamaria's "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

www.aycinena.com

Chip Design Magazine

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won't want to miss. And, be sure to visit www.eecatalog.com for valuable information about all of Extension Media's outstanding technology resources.

www.chipdesignmag.com

Elektronik i Norden

Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed copies proves we are the major electronics paper in this area. We publish news, comments and in-depth technical articles.

www.elinor.se

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Engineering & Technology Magazine – Published by The IET

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Each member of the Institution of Engineering & Technology (IET) receives a copy as part of their membership package. Readers include design & development engineers, system designers & integrators, solutions providers & installers, engineering distributors, consultants, planners, facilities managers & end-users.
With its HQ in London & regional offices in Europe, North America & Asia-Pacific, the Institution of Engineering & Technology provides a global knowledge network to facilitate the exchange of ideas & promote the positive role of technology around the World. The Institution of Electrical Engineers, dating from 1889, became the Institution of Engineering & Technology in 2006. It now organises more than 120 conferences & other events each year whilst providing professional advice & briefings to industry, education & governments.

www.eandtmagazine.com

Micronews Media, powered by Yole Développement

Founded in 1998, Yole Développement has grown to become a group of companies providing marketing, technology and strategy consulting, media in addition to corporate finance services. With a strong focus on emerging applications using silicon and/or micro manufacturing, Yole Développement group has expanded to include more than 50 associates worldwide covering MEMS, Compound Semiconductors, LED, Image Sensors, Optoelectronics, Microfluidics & Medical, Photovoltaics, Advanced Packaging, Manufacturing, ok Nanomaterials and Power Electronics. The group supports industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

MEDIA & EVENTS ACTIVITY

- i-Micronews.com, online disruptive technologies website
- Weekly WebTalk
- @Micronews, weekly e-newsletter
- Technology Magazines dedicated to MEMS, Advanced Packaging, LED and Power Electronics
- Communication & webcasts services
- Events: Yole Seminars, Market Briefings

www.i-Micronews.com

MONDAY 24 MARCH

monday 24 march

0730	TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS					
Breaks	1100 – 1130 MORNING COFFEE BREAK, 1600 – 1630 AFTERNOON COFFEE BREAK					
0930 – 1300	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 6	Konferenz 5
	M01 Development of mixed-criticality systems based on system partitioning	M02 Software Debug on ARM Processors in Emulation	M03 Automatic fixed-point conversion: a gate way to high-level power optimization	M04 Dynamic Heterogeneous Architectures to Address The Efficiency Crisis!	M05 Wireless NoC as Interconnection Backbone for Multi-core Chips: Promises, Challenges, and Recent Developments	M06 Testing of TSV-Based 2.5D- and 3D-Stacked ICs
1300 – 1430	LUNCH BREAK					
1330	CONFERENCE REGISTRATION BEGINS					
1430 – 1800	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 6	Konferenz 5
	M07 L4/Fiasco.OC - A Microkernel OS Designed for Security, Real-Time and Reliability	M08 Microfluidic Biochips: A Vision for More than Moore and Biochemistry-on-Chip	M09 Energy-Efficient System Design Through Error-Resilient Computing	M10 A Cyber-Physical Approach to Modeling, Simulation and Verification of Smart Systems	M11 Post-Silicon Validation and Debug: Best Practices and Disruptive Innovation	M12 All You Need to Know About Hardware Trojans and Counterfeit ICs
1800 – 1900	WELCOME RECEPTION, Saal 1					

Conference March 9 – 13, 2015
Exhibition March 10 – 12, 2015
Grenoble, France

TUESDAY 25 MARCH

tuesday 25 march

0730	REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2							
0830 – 1030	1.1 OPENING PLENARY, DATE AWARDS CEREMONY AND KEYNOTE ADDRESSES, Grosser Saal							
1030 – 1130	EXHIBITION AND COFFEE BREAK							
	EXECUTIVE SESSIONS	SPECIAL SESSIONS	A-TRACK	D-TRACK	D-TRACK	E-TRACK	T-TRACK	EXHIBITION THEATRE
1130 – 1300	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
	2.1 EXECUTIVE SESSION: How to Handle Today's Design Complexity	2.2 Panel: Emerging vs. Established Technologies: a Two Sphinxes' Riddle at the Crossroads?	2.3 Making automotive systems safer and more energy efficient	2.4 Modern Challenges in Analog and Mixed-Signal Design	2.5 Low-Power and Efficient Architectures	2.6 Real-Time memory hierarchies	2.7 Yield and Reliability for Robust Systems	2.8 Hot Topic: Technology Transfer towards Horizon 2020
1300 – 1430	LUNCH BREAK							
1430 – 1600	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
	3.1 EXECUTIVE SESSION: Advanced Technology Challenges & Opportunities	3.2 Panel: The World Is Going... Analog & Mixed-Signal! What about EDA?	3.3 Secure Hardware Primitives and Implementations	3.4 Modeling and Optimization of Power Distribution Networks	3.5 Robust Architectures	3.6 Cyber Physical Systems: Security and Co-design	3.7 On line Strategies for Reliability	3.8 Hot Topic: Mission Profile Aware Design – The Solution for Successful Design of Tomorrows Automotive Electronics
1600 – 1700	COFFEE BREAK *co-sponsored by ELSEVIER*							
1600 – 1630	IP1 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer							
1700 – 1830	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
	4.1 EXECUTIVE SESSION: Addressing Challenges of Reliable Chips	4.2 Hot Topic: Multicore Systems in Safety Critical Electronic Control Units for Automotive and Avionics	4.3 Secure Device Identification	4.4 "Almost there" emerging technologies	4.5 Memory System Architectures	4.6 Code Generation and Optimization for Embedded Platforms	4.7 Dependable System Design	4.8 State-of-the-art in Verification: European Tertulia IC Design - Enabling AMS Structured Verification / Verification in FPGA & IP design flows
1830 – 1930	EXHIBITION RECEPTION							

Executive Session
Plenary Session
D-Track
A-Track
T-Track
E-Track
Special Session
IP Session
Exhibition Theatre Session

• WEDNESDAY 26 MARCH • wednesday 26 march

	SPECIAL DAY	SPECIAL SESSIONS	A-TRACK	D-TRACK	D-TRACK	E-TRACK	T-TRACK	EXHIBITION THEATRE
0730	**REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
0830 – 1000	5.1 SPECIAL DAY Hot Topic: Predictable Multi-Core Computing	5.2 Hot Topic: Hacking and Protecting Hardware: Threats and Challenges	5.3 Reliable Systems in the Age of Variability	5.4 Prediction and optimization of timing variations	5.5 Boosting the Scalability of Formal Verification Technologies	5.6 Emerging logic technologies	5.7 Test generation and optimization	5.8 Embedded Tutorial: System Integration – The Bridge between More than Moore
1000 – 1100	**EXHIBITION AND COFFEE BREAK**							
1000 – 1030	**IP2 INTERACTIVE PRESENTATIONS, Conference Level, Foyer**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1100 – 1230	6.1 SPECIAL DAY Hot Topic: The fight against Dark Silicon	6.2 Embedded Tutorial: Emerging Transistor Technologies: From Devices to Architectures	6.3 Management of Micro/ Macro Renewable Energy Storage Systems	6.4 Power delivery and distribution	6.5 Beyond EDA: Extending the Application Domain of Formal Methods	6.6 Model-Based Design and Hardware/ Software Interfaces	6.7 Hardening Approaches at Different Design Levels	6.8 First Time Right in Analog Design Enabling New Business Cases
1230 – 1400	**LUNCH BREAK**							
1330 – 1400	**7.0 SPECIAL DAY KEYNOTE, Saal 1**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1430 – 1600	7.1 SPECIAL DAY Panel: HW/SW Co-Development - The Industrial Workflow	7.2 Embedded Tutorial: Cross Layer Resiliency in Real World	7.3 Low power methods and multicore architectures for mobile health applications	7.4 Runtime memory optimization and GPU/ manycore architectures	7.5 Emerging memory technologies	7.6 Performance and timing analysis	7.7 Design-for-Test and Test Access	7.8 FD-SOI – the Enabling European Technology for Energy Efficient Solutions – Creating a Solution Hive & Design Hub as Eco-System for Future Success
1600 – 1700	**COFFEE BREAK**							
1600 – 1630	**IP3 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1700 – 1830	8.1 SPECIAL DAY: System Simulation and Virtual Prototyping	8.2 Hot Topic: Near Threshold Computing (NTC)	8.3 Physical Attacks and counter-measures	8.4 Efficient Designs for Telecom and Financial Applications	8.5 Modeling & Specification	8.6 Mapping and Scheduling for Many-Core Embedded Systems	8.7 Performance Modeling and Delay Test	8.8 Hot Topic: Beyond CMOS Ultra-low-power Computing
1930 – 2300	**DATE PARTY** *co-sponsored by the City of Dresden*							

Special Day 1 | Special Session | IP Session | Exhibition Theatre Session
D-Track | A-Track | T-Track | E-Track

• THURSDAY 27 MARCH • thursday 27 march

	SPECIAL DAY	D-TRACK	A-TRACK	D-TRACK	D-TRACK	E-TRACK	D-TRACK	EXHIBITION THEATRE
0730	**REGISTRATION, Terrace Level, AND SPEAKER'S BREAKFAST, Saal 2**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
0830 – 1000	9.1 SPECIAL DAY Hot Topic: CMOS scaling - from evolutionary to revolutionary computing	9.2 Low-Cost, High-Performance NoCs	9.3 Hardware Implementations for Data Security	9.4 Timing challenges in validation	9.5 Hot Topic: Connecting Different Worlds – Technology Abstraction for Reliability-Aware Design and Test	9.6 Schedulability analysis	9.7 Timing Analysis and Cell Design	9.8 Embedded Tutorial: Memcomputing: the Cape of Good Hope
1000 – 1100	**EXHIBITION AND COFFEE BREAK**							
1000 – 1030	**IP4 INTERACTIVE PRESENTATIONS, Conference Level, Foyer**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1100 – 1230	10.1 SPECIAL DAY Hot Topic: Memories today and tomorrow	10.2 Wireless NoCs	10.3 Green Computing Systems	10.4 System-level evaluation	10.5 Analysis of Components and Systems	10.6 Multi-processor and distributed systems	10.7 Advances in Synthesis	10.8 EDA+3D+ MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics
1230 – 1400	**LUNCH BREAK**							
1330 – 1400	**11.0 SPECIAL DAY KEYNOTE, Saal 1**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1400 – 1530	11.1 SPECIAL DAY Embedded Tutorial: Alternatives to CMOS	11.2 Transitioning NoC Design Techniques to Future Challenges	11.3 Industry relevant research and practice for system design	11.4 Enabling validation on fast platforms	11.5 Memory Resource Allocation and Scheduling in MPSoC	11.6 System-Level Thermal Estimation and Management	11.7 Power and Emerging Technologies in Reconfigurable Computing	11.8 Embedded Tutorial: GPGPUs: how to combine high computational power with high reliability
1530 – 1600	**COFFEE BREAK**							
1530 – 1600	**IP5 INTERACTIVE PRESENTATIONS AND BEST IP AWARD, Conference Level, Foyer**							
	Saal 1	Konferenz 6	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre
1600 – 1730	12.1 SPECIAL DAY Hot Topic: The future of interfacing to the natural world	12.2 Hot topic: How Secure are PUFs Really? On the Reach and Limits of Recent PUF Attacks	12.3 Multimedia Systems	12.4 Physical Aspects	12.5 System-level Design Space Exploration	12.6 Error Resilience and Power Management	12.7 Built-in self-test solutions for mixed-signal and RF ICs	12.8 Panel: Future SoC verification methodology: UVM evolution or revolution?

Special Day 2 | Special Session | IP Session | Exhibition Theatre Session
D-Track | A-Track | T-Track | E-Track

0730	WORKSHOP REGISTRATION AND WELCOME REFRESHMENTS
Breaks	PLEASE SEE INDIVIDUAL WORKSHOP PROGRAMMES FOR LUNCH AND BREAK TIMES

0830-1700 Konferenz 1	0830-1700 Konferenz 2	0830-1700 Konferenz 3	0830-1700 Konferenz 4
W1 International Workshop on Dependable GPU Computing	W2 ES4CPS - Engineering Simulations for Cyber-Physical Systems	W3 Electronic System-Level Design towards Heterogeneous Computing	W4 Workshop on Design Automation for Understanding Hardware Designs

0815-1630 Konferenz 5	0830-1630 Konferenz 6	0830-1700 Seminar 5+6	0830-1700 Seminar 3+4
W5 3D Integration: Applications, Technology, Architecture, Design, Automation, and Test	W6 MEDIAN - Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale	W7 Memristor Science & Technology	W8 3PMCES – Performance, Power and Predictability of Many-Core Embedded Systems

INTERACTIVE PRESENTATIONS

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held on the Conference Level of the congress centre in 30-minute time slots on the following days:

IP Session 1, Tuesday, March 25, 2014	Conference Level, Foyer	**1600 – 1630**
IP Session 2, Wednesday, March 26, 2014	Conference Level, Foyer	**1000 – 1030**
IP Session 3, Wednesday, March 26, 2014	Conference Level, Foyer	**1600 – 1630**
IP Session 4, Thursday, March 27, 2014	Conference Level, Foyer	**1000 – 1030**
IP Session 5, Thursday, March 27, 2014	Conference Level, Foyer	**1530 – 1600**

After the last IP Session of each day, the "Best IP of the Day" will be awarded.

PLENARY SESSION · plenary session

Tuesday, March 25, 2014, 0830 – 1030, Grosser Saal
Opening Plenary, DATE Awards Ceremony and Keynote Addresses

KEYNOTE ADDRESS · first keynote address

Tuesday, March 25, 2014, 0910

1.1.1 System design challenges for next generation wireless and embedded Systems

David Fuller, National Instruments, US

Application demands in our embedded world are growing dramatically. Consumer expectations and the industry's forward-looking technology roadmaps paint a picture of a connected world full of intelligent devices once thought to have fixed functionalities. Researchers exploring next generation wireless systems, Internet of Things (IOT), and even machine-to-machine (M2M) communications face many challenges in making this vision a reality. Where once a single, isolated design flow addressed the discrete application, heterogeneous multi-processing architectures must be considered and embraced along with the connections to other devices and systems, and real-world sensor data. As the systems grow in complexity, new design approaches must also be developed and employed to expedite the research, design, and development cycle. David Fuller will outline challenges system designers face in developing cyber-physical systems and explore a graphical system design approach that includes hardware abstraction and comprehends a heterogeneous multiprocessing environment while embracing different models of computation. Through this new approach, system designers can shorten design cycles and the time to prototype ultimately accelerating deployment.

KEYNOTE ADDRESS · second keynote address

Tuesday, March 25, 2014, 0950

1.1.2 The growing importance of microelectronics from a foundry perspective

Gerd Teepe, GLOBALFOUNDRIES, DE

Microelectronics is the dominant industrial technology of today. Its rate of innovation, spelled out by Moore's Law, is exceptional by any commercial metric, especially, as it has been on this trajectory for almost 40 years. It is not surprising, that other industrial sectors are taking advantage of the innovation engine of the semiconductors for its own product innovation: Cars are safer and more economic, medical diagnostics are performing to a significantly higher level, and energy efficiency from the generation to the consumer is a lot more efficient. "The Internet" has become the basis for our communication, organization and planning in our economies with significant impact to our society. However, the Semiconductor industry is under a powerful transformation marked by the following trends: - Design Complexity is facing new challenges, as technological complexity is transferred to the design space at an accelerated pace - The SOC is dominating the design space - Intelligent Things are emerging with unprecedented cognitive and motion capabilities - The supply chain transformation is in full motion, with the foundry model at the forefront With these powerful trends in motion, we will have to rethink our approach towards semiconductors as part of the industrial system. It will not be sufficient any more to "enhance" traditional products like Cars, TVs, machines or phones with semiconductor content to make them perform at a higher level to increase its value to consumers. We need to rethink the connected world around us to truly assess the next generation of intelligent applications, which we are about to enter.

SPECIAL DAY · special day keynote addresses

KEYNOTE ADDRESS · wednesday keynote address

Wednesday, March 26, 2014, 1330 – 1400, Saal 1

7.0 The connected car and its implication to the automotive chip roadmap

Michael Bolle, Robert Bosch GmbH, DE

The automotive industry is in a radical change process driven by technology. On the one hand side the proliferation of communication technologies into the car leads to internet connected vehicles. The vehicle will become an integral part of the internet – opening new processing paradigms for the car itself. On the other hand the vehicle itself significantly expands its sensor and processing capabilities by the use of radar, video, ultrasound sensors and usage of state of the art CPU and GPU processor architectures. In our talk we will address both developments and outline foreseen future applications as future driving assistant and infotainment systems as well as highly automated driving. We will discuss major requirements for the future electrical architectures and implications for future automotive chips.

KEYNOTE ADDRESS · thursday keynote address

Thursday, March 27, 2014, 1330 – 1400, Saal 1

11.0 Organic electronics – from lab to markets

Karl Leo, Technische Universität Dresden, DE

Organic semiconductors with conjugated electron system are currently intensively investigated for optoelectronic applications. This interest is spurred by novel devices such as organic light-emitting diodes (OLED), organic solar cells, and flexible electronics. During this talk, I will discuss some of the recent progress in realizing devices, in particular highly efficient white OLED for lighting and flexible organic solar cells.

Executive Sessions

Organiser: **Yervant Zorian,** Synopsys, US

DATE 2014 will again feature an Executive Track of presentations by leading company executives representing a range of semiconductor manufacturers, EDA vendors, fables houses and IP providers. This one-day program will be held on Tuesday 25 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks.

All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view.

2.1 EXECUTIVE SESSION: How to Handle Today's Design Complexity

Saal 1 1130 – 1300

Organiser: **Yervant Zorian,** Synopsys, US
Executives: **Sanjive Agarwala,** Texas Instruments, US
Paul Lo, Synopsys, US
Rainer Kress, Infineon, DE
Leon Stock, IBM, US
Sanjiv Taneja, Cadence, US

The widening gap between growing SOC complexity and designer productivity limits traditional chip design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of complex SOC design. Executives in this session will discuss the impact of complexity and the new opportunities it may bring in designing today's SOC.

3.1 EXECUTIVE SESSION: Advanced Technology Challenges & Opportunities

Saal 1 1430 – 1600

Organiser: **Yervant Zorian,** Synopsys, US
Executives: **Giorgio Cesana,** STMicroelectronics, FR
Joachim Kunkel, Synopsys, US
Rudy Lauwereins, IMEC, BE
Maria Merced, TSMC, NL
Gerd Teepe, GLOBALFOUNDRIES, DE

The continuous technology scaling and their new applications are dramatically impacting the semiconductor industry. This may also significantly affect the dependency between eco-system players necessitating smooth interdependency between them. The executives in this session will discuss upcoming innovations in the semiconductor industry and their impact on the solutions offered by the eco system players.

4.1 EXECUTIVE SESSION: Addressing Challenges of Reliable Chips

Saal 1 1700 – 1830

Organiser: **Yervant Zorian,** Synopsys, US
Executive: **Dan Alexandrescu,** iROC Technologies, FR
Robert Aitken, ARM, US
Robert Hum, Mentor Graphics, US
Ronald Martino, Freescale, US

While today's SOCs systematically use semiconductor production quality assessment and optimization solutions, meeting end-product requirements for reliability and availability augments the need to prepare the SOC design in advance to address such requirements. The speakers in this executive session will address the current trends and challenges in the semiconductor reliability and discuss the level of readiness needed in a chip to meet today's SOC requirements.

SPECIAL DAY: System-Level Design

Organisers and Co-Chairs: **Jürgen Teich,** University of Erlangen-Nuremberg, DE
Johannes Stahl, Synopsys, US

The special day System-Level Design will reflect current industrial practices as well as present recent advances in this research area. A particular emphasis will be on ultra-low power design and modeling at multiple abstraction levels, virtual platforms for software development and architecture design of MPSoCs. We will also take a look at high-level synthesis from different input languages as well as software code generation techniques. Important topics also include multicore enablement for safety-critical and real-time embedded systems as well as accelerator-rich design for the fight against dark silicon.

5.1 HOT TOPIC: Predictable Multi-Core Computing

Saal 1 0830 – 1000

Organiser: **Jürgen Teich,** University of Erlangen-Nuremberg, DE
Chair: **Petru Eles,** Linkoping University, SE
Co-Chair: **Jürgen Teich,** University of Erlangen-Nuremberg, DE

The requirement of high performance computing at low power can be met by the parallel execution of an application on a possibly large number of programmable cores. However, the lack of accurate timing properties may prevent parallel execution from being applicable to time-critical applications. This session treats this important problem of time predictability of applications on multi-core platforms by presenting results of the impact of resource sharing on performance, an architecture that has been designed to meet predictability requirements as well as new results on scheduling mixed critical applications on multi-core platforms.

6.1 HOT TOPIC: The fight against Dark Silicon

Saal 1 1100 – 1230

Organiser: **Jörg Henkel,** Karlsruhe Institute of Technology, DE
Chair: **Jörg Henkel,** Karlsruhe Institute of Technology, DE
Co-Chair: **Jürgen Teich,** University of Erlangen-Nuremberg, DE

Dark Silicon is predicted to dominate the chip footage of upcoming many-core systems within a decade since Dennard Scaling fails mainly due to the voltage-scaling problem that results in higher power densities. It would deem upcoming technologies nodes inefficient since a majority of cores would lie fallow. Significant research efforts have started within the last couple of years to investigate and mitigate Dark Silicon effects to ensure an effective use of available chip footage. This special session gives a snapshot of current research activities of this grand challenge. In particular, the three talks present the newest trends and developments starting with the problem of Dennard Scaling and how it mandates new design constraints followed by the problem of power delivery and cooling, and concluding with the newest directions in efficient resource management for many-core systems.

7.0 The connected car and its implication to the automotive chip roadmap

Saal 1 1330 – 1400

Michael Bolle, Robert Bosch GmbH, DE

→ See page 11

7.1 PANEL: HW/SW Co-Development – The Industrial Workflow

Saal 1 1430 – 1600

Organiser: **Johannes Stahl,** Synopsys, US
Chair: **Iris Stroh,** Markt & Technik, DE

This panel brings together the entire supply chain for the use of virtual prototyping starting with the end users at an automotive Tier1, a semiconductor supplier, IP providers and the virtual prototyping and software development tool providers. The panelists will discuss what are the benefits and challenges of accelerating software development using virtual prototyping are for deployment in industrial projects.

8.1 System Simulation and Virtual Prototyping

Saal 1 1700 – 1830

Organiser: **Johannes Stahl,** Synopsys, US
Chair: **Johannes Stahl,** Synopsys, US

In this session we will review several practical applications of virtual prototyping for architecture design work and software development across different markets such as mobile, industrial and automotive. The authors will share their practical experiences in using the virtual prototyping methodology and current commercial tools.

Special Day: Advancing Electronics beyond CMOS

Organisers and Co-Chairs: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Thomas Mikolajick, Namlab (cfAED), DE

As the issues associated with CMOS scaling become harder and more costly to solve, the special day Advancing Electronics beyond CMOS will cover the latest trends towards alternative devices and paradigms for computing and data acquisition, storage and transport. Important topics include nanoscale switching devices and computing nanofabrics, trends in memory technologies in hybrid 3D integration, flexible and organic electronics, new state variable vectors (spintronics, photonics) and interfaces to the natural world (sensor networks, data analysis, displays, MEMS).

9.1 HOT TOPIC: CMOS scaling - from evolutionary to revolutionary computing

Saal 1 0830 – 1000

Organisers: **Thomas Mikolajick,** NamLab gGmbH, DE, **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Chair: **Thomas Mikolajick,** NamLab gGmbH, DE
Co-Chair: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR

Transistors as switches have now scaled down to a point where the classical bulk structure is no longer tenable and it is necessary to change the nature of the channel structure. In this session, the three principal contenders for following on from conventional devices will be examined. The first paper looks at the use of III-V nanowires, with expected benefits in terms of speed and energy, as well as integration challenges. The second paper looks at how the use of switches with controllable polarity, such as in silicon nanowire devices, can improve the energy efficiency of systems on chip. The devices themselves are explored in detail in the third paper, with the concept of fine-grain reconfigurability at the fore. The fourth and final paper gives a reality check on carbon electronics and the most promising devices in this class.

10.1 HOT TOPIC: Memories today and tomorrow

Saal 1 1100 – 1230

Organisers: **Thomas Mikolajick,** NamLab gGmbH, DE, **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Chair: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Co-Chair: **Thomas Mikolajick,** NamLab gGmbH, DE

Memory devices and technologies have undergone huge transformations in recent years and many industrially viable replacements to conventional technologies are on the brink of entering the market. The first paper in this session gives an overview of alternative memory technologies and how each can contribute or disrupt accepted memory hierarchies. The quest for a universal memory device is still underway, and the other papers in this session focus on various approaches for future memory devices. The second paper examines phase change memories, while magnetic memories are discussed in the third paper, both in terms of standard memory applications but also in terms of how they can improve logic performance. Resistive memories are the topic of the fourth paper, where new applications are considered – in FPGAs, NoCs and crossbars. The fifth paper in this session looks at low-cost memory with a printable manufacturing approach, leading to other applications and market segments.

11.0 Organic electronics – from lab to markets

Saal 1 1330 – 1400

Karl Leo, Technische Universität Dresden, DE

→ See page 11

11.1 EMBEDDED TUTORIAL: Alternatives to CMOS

Saal 1 1400 – 1530

Organisers: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR, **Thomas Mikolajick,** NamLab gGmbH, DE
Chair: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Co-Chair: **Thomas Mikolajick,** NamLab gGmbH, DE

Alternative approaches to CMOS-based computing structures abound, for logic, memory, interconnect and interfaces. This embedded tutorial aims to give in-depth analyses of three promising technologies. The first paper covers spintronics and its use in logic and memory to achieve low-power computing architectures. Silicon photonics, with anticipated benefits for interconnect structures, is examined in the second paper. The third paper looks at the status of organic electronics and the properties of thin-film transistors for large displays and sensor arrays on flexible supports.

12.1 HOT TOPIC: The future of interfacing to the natural world

Saal 1 1600 – 1730

Organisers: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR, **Thomas Mikolajick,** NamLab gGmbH, DE
Chair: **Thomas Mikolajick,** NamLab gGmbH, DE
Co-Chair: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR

Challenges for acquiring and processing data from the real world includes the development of interfaces capable of extracting relevant information from massive sensor networks or from living organisms, sifting through the wealth of data to arrive systematically at a meaningful conclusion, and building hardware platforms suited to carry out these operations in an energy-efficient way. The first paper in this session looks at the necessarily complex processing of chemical information with hardware components that are capable of responding to various chemical conditions. Interfaces to living organisms are examined in the second paper, which discusses challenges and approaches for efficient detection of disease. In the third paper, novel hardware devices and architectures are explored for use in energy-efficient video analysis applications such as movement detection and face recognition. The fourth paper discusses handling of complex data with large-scale GPU-based recurrent networks, exploiting specific features of the data to improve energy efficiency.

Organiser: **Juergen Haase,** edacentrum, DE

In addition to the conference programme during DATE 14, there will be a presentation theatre from Tuesday, 25 March, to Thursday, 27 March, 2014. Attendees will profit from having an industry forum in the midst of Europe's leading electronic systems design event. The theatre is located in the exhibition area on the Terrace Level and affords easy access for exhibition visitors as well as for conference delegates.

2.8 SPECIAL SESSION

Hot Topic: Technology Transfer towards Horizon 2020

Tuesday, March 25, 2014, 1130 – 1300

Organiser: **Rainer Leupers,** RWTH Aachen, DE
Chair: **Norbert Wehn,** TU Kaiserslautern, DE

European research projects produce many excellent results, and the quality of research papers at DATE and other major European conferences is often outstanding. But how many academic research results in computing technologies and EDA actually make it into industrial practice? In the context of the transition into the Horizon 2020 framework program, the European research community is currently investigating novel ways of stimulating additional academia-industry technology transfer. This special session contributes by discussing concrete transfer experiences and new concepts. Furthermore it will exemplify several success stories from both academic and industrial perspectives.

3.8 SPECIAL SESSION

Hot Topic: Mission Profile Aware Design – The Solution for Successful Design of Tomorrows Automotive Electronics

Tuesday, March 25, 2014, 1430 – 1600

Organisers: **Goeran Jerke,** Robert Bosch GmbH, DE
Oliver Bringmann, University of Tuebingen, DE
Chair: **Goeran Jerke,** Robert Bosch GmbH, DE
Co-Chair: **Oliver Bringmann,** University of Tuebingen, DE

In order to benefit from modern automotive semiconductor technologies, application robustness must now be considered as a design target. This includes the consequent consideration of environmental stress conditions and functional loads, which are formalized in so-called "mission profiles". We introduce the motivation to use mission profiles from an OEM and Tier n perspective. Additionally, we introduce the mission profile aware design flow and present several application scenarios.

4.8 EXHIBITION THEATRE SESSION

State-of-the-art in Verification: European Tertulia IC Design – Enabling AMS Structured Verification / Verification in FPGA & IP design flows

Tuesday, March 25, 2014, 1700 – 1830

Details to be announced.

5.8 SPECIAL SESSION

System Integration - The Bridge between More than Moore and More Moore

Wednesday, March 26, 2014, 0830 – 1000

Organiser: **Manfred Dietrich,** Fraunhofer IIS/EAS Dresden, DE
Kai Hahn, University Siegen, DE
Chair: **Manfred Dietrich,** Fraunhofer IIS/EAS Dresden, DE
Co-Chair: **Kai Hahn,** University Siegen, DE

System Integration using 3D technology is a very promising way to cope with current and future requirements for electronic systems. Since the pure shrinking of devices (known as "More Moore") will come to an end due to physical and economic restrictions, the integration of systems (e.g. by stacking dies, or by adding sensor functions) shows a way to maintain the growth in complexity as well as in diversity which is necessary for future applications. This so called "More than Moore" approach complements the conventional SoC product engineering. This session gives insights in System Integration design challenges from different perspectives, ranging from design technology over MEMS product engineering and 3D interconnect to automotive cyber physical systems.

6.8 EXHIBITION THEATRE SESSION

First Time Right in Analog Design Enabling New Business Cases

Wednesday, March 26, 2014, 1100 – 1230

Details to be announced.

7.8 EXHIBITION THEATRE SESSION

FD-SOI – the Enabling European Technology for Energy Efficient Solutions – Creating a Solution Hive & Design Hub as Eco-System for Future Success

Wednesday, March 26, 2014, 1430 – 1600

Details to be announced.

8.8 SPECIAL SESSION

Hot Topic: Beyond CMOS Ultra-low-power Computing

Wednesday, March 26, 2014, 1700 – 1830

Organiser: **Saibal Mukhopadhyay,** Georgia Institute of Technology, US
Chair: **Arijit Raychowdhury,** Georgia Institute of Technology, US
Co-Chair: **Saibal Mukhopadhyay,** Georgia Institute of Technology, US

With conventional CMOS scaling becoming increasingly challenging, the designers wonder what opportunities and challenges exist beyond-CMOS for both Boolean and non-Boolean computing. This session will discuss three very different and promising emerging technologies – Tunneling Field-Effect Transistor, Spintronics, and nano-electro-mechanical switches (NEMS) – for low-power electronics. The talks will discuss the need for innovating and evaluating new circuit and system design methods as new device technologies emerge.

9.8 SPECIAL SESSION

Embedded Tutorial: Memcomputing: the Cape of Good Hope

Thursday, March 27, 0830 – 1000

Organisers: **Yiyu Shi,** Missouri University of Science & Technology, US
Hung-Ming Chen, National Chiao Tung University, TW
Chair: **Tsung-Yi Ho,** CSIE, NCKU, TW
Co-Chair: **Hung-Ming Chen,** National Chiao Tung University, TW

Energy efficiency has emerged as a major barrier to performance scalability for modern processors. On the other hand, significant breakthroughs have been achieved in memory technologies recently. As such, the fascinating idea of memcomputing (i.e., use memory for computation purposes) has drawn wide attention from both academia and industry as an effective remedy. Compared with conventional logic computing, memory array provides large set of parallel resources with high bandwidth, which can be configured to perform computing in spatial/temporal manner leading to dramatic reduction in processor-memory traffic. Moreover, memory computing brings the computing engine close to the data, thus drastically minimizing the von Neumann bottleneck. Finally, it exploits the advances in memory technologies and integration approaches (e.g. 3D integration) to achieve better technology scalability. This special session offers a broad-spectrum retreat (devices, processes and systems) on this hot topic to the general CAD community, hoping to inspire more contributions from the design automation perspective.

10.8 EXHIBITION THEATRE PANEL

EDA+3D+MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics

Thursday, March 27, 2014, 1100 – 1230

Organiser: **Jürgen Haase,** edacentrum, DE
Moderator: **Ahmed Jerraya,** CEA-LETI, FR
Panelists: **Gabriel Kittler,** X-FAB, DE
Brandon Wang, Cadence, US
Brent Gregory, Synopsys, US
Horst Symanzik, Bosch-Sensortec GmbH, DE
Gerd Teepe, GLOBALFOUNDRIES, DE

Today the most powerful innovations in the major industries and the most promising approaches to tackle burning societal challenges are substantially influenced by and depending from the innovations provided by the microelectronics industry. Breakthroughs in manufacturing technologies enable the realization of novel types of devices and of systems, which enable applications with fascinating functionality and enormous performance. However, this innovation chain is not operational without appropriate innovations in design technology: We need an innovation Agenda 2020 for design methodology and EDA tools fueling the innovation chain of electronics. 2014 the technologies for MEMS and for 3D chips have reached a maturity level that enables them to reshape our lives until 2020. This panel will discuss how to utilize these technologies: Which applications will become possible with the upcoming innovations in 3D and MEMS technologies, what kind of EDA innovations will be required in order to be able to implement these applications effectively and efficiently, yielding powerful yet reliable components and systems. The set-up of the panel includes the manufacturers GLOBALFOUNDRIES and X-FAB, Bosch as leading supplier of technology and one of the MEMS pioneers as well as leading EDA vendors Cadence and Synopsys.

11.8 SPECIAL SESSION

Embedded Tutorial: GPGPUs: how to combine high computational power with high reliability

Thursday, March 27, 1400 – 1530

Organiser: **Matteo Sonza Reorda,** Politecnico di Torino, IT
Chair: **Dimitris Gizopoulos,** University of Athens, GR
Co-Chair: **Rob Aitken,** ARM, US

The embedded tutorial aims at providing with an updated view on what GPGPUs can provide not only in terms of performance and power, but also in terms of reliability, and how the latter can be evaluated and possibly improved.

12.8 SPECIAL SESSION

Panel: Future SoC verification methodology: UVM evolution or revolution?

Thursday, March 27, 1600 – 1730

Organiser: **Alex Goryachev,** IBM Research, Haifa, IL
Chair: **Rolf Drechsler,** University of Bremen/DFKI, DE

It is a recent trend that SoCs are becoming more similar to servers. Many SoCs today are no longer tied to a single application and look more like general purpose PCs and high-end servers. Smartphones are the most notable example of this, but we are also seeing this with TV chips, in-car controllers, network routers, and more. This trend is occurring in parallel to the constantly growing complexity of SoCs, which support diverse IO interfaces and devices, and have complex architectures including multiple heterogeneous cores, multi-level caches, and multiple IO bridges.

Today, common practice for verification is based on Universal Verification Methodology (UVM), which, at the system level, is built on reusing and combining unit-level environments, followed by running real software on an SoC. This methodology leaves a large gap. In high-end systems, this gap is covered by system-level verification that focuses on HW-only system integration. This level has its own methodology, dedicated environment, set of tools, and teams. It looks at the system as a whole and is not based on reusing lower level environments.

Formal methods are a field of intensive research, but they have not been adopted by the industry for SoC-level verification.

In this panel leading experts from industry (both users and vendors) and academy will discuss the future of SoC verification methodology. Is the gap in today's SoC verification methodology significant? Is it growing? Or perhaps it does not exist? What is the right way to close the gap, if one exists? Is it sufficient to extend UVM capabilities (e.g., SystemC, TLM) or are dedicated tools and methodology needed? Are formal methods ready to play a significant role in SoC-level verification? In general, we would like to determine the importance of system-level verification and its unique needs—whether generators, checking, coverage, or teams.

The DATE 2014 Programme Committee has again put emphasis on providing plenty of opportunities for conference delegates to visit the exhibition, get in touch with colleagues and attend the sessions in the exhibition theatre.

A number of specialist interest groups will be holding their meetings at DATE 2014. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage www.date-conference.com.

Day+Time	Meeting & Contact	Room
Mon 1900-2100	**ACM SIGDA/EDAA PhD Forum** Peter Marwedel, EDAA/ACM SIGDA, DE <peter.marwedel@tu-dortmund.de>	Saal 1
Tue 1300-1430	**eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)** Giorgio Di Natale, LIRMM, FR <giorgio.dinatale@lirmm.fr>	Seminar 3
Tue 1830-1930	**EDAA General Assembly** Georges Gielen, Katholieke Universiteit Leuven, BE <Georges.Gielen@kuleuven.be>	Seminar 2
Tue 1830-2000	**IFIP Working Group 10.5** Dominique Borrione, IMAG, FR <Dominique.Borrione@imag.fr>	Seminar 4
Tue 1830-2030	**IFIP Working Group 10.2** Achim Rettberg, University of Oldenburg, DE <achim.rettberg@iess.org>	Seminar 5
Thu 1230-1400	**DATE Sister-Events Meeting** Georges Gielen, Katholieke Universiteit Leuven, BE <Georges.Gielen@kuleuven.be>	Seminar 5

Coffee & Lunch Breaks

The exhibition area on the Terrace Level of the International Congress Centre also hosts the coffee and lunch break area. During the below-mentioned times, coffee and tea will be served during the coffee breaks as well as light snacks during the lunch breaks (for full conference delegates only). Furthermore, there is a cash bar on the Terrace Level for visitors and exhibitors.

Tuesday, March 25, 2014	Coffee Break 1030 – 1130	Lunch Break 1300 – 1430	Coffee Break 1600 – 1700
Wednesday, March 26, 2014	Coffee Break 1000 – 1100	Lunch Break 1230 – 1400	Coffee Break 1600 – 1700
Thursday, March 27, 2014	Coffee Break 1000 – 1100	Lunch Break 1230 – 1400	Coffee Break 1530 – 1600

Exhibition Reception, Tuesday, March 25, 2014

The Exhibition Reception will take place on Tuesday, March 25, 2014, from 1830 – 1930 in the exhibition area (Terrace Level), where free drinks and snacks for all conference delegates and exhibition visitors will be offered.

DATE Party, Wednesday, March 26, 2014

The DATE Party is again scheduled on the second conference day, Wednesday, March 26, 2014, starting from 1930. This year, it will take place in one of Dresden's most exciting and modern buildings, the "Gläserne Manufaktur" of the car manufacturer Volkswagen AG (www.glaesernemanufaktur.de/en/). The party will feature a flying buffet style dinner with various catering points and accompanying drinks. Light background music and the possibility of guided visits through the extraordinary premises will round off the evening. It provides a perfect opportunity to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities.
Please kindly note that it is no seated dinner.

All delegates, exhibitors and their guests are encouraged to attend the party. Please be aware that entrance is only possible with a party ticket. Each full conference registration includes a ticket for the DATE Party. Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets).
Ticket price for the full Evening Social Programme: 75 € per person.

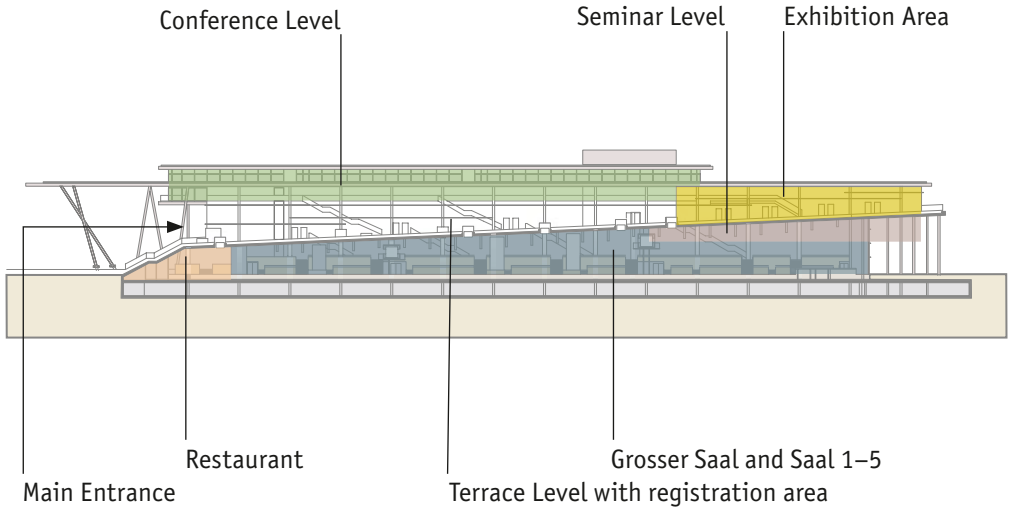
DATE Party Shuttle: There will be an organised shuttle by tram to the DATE Party venue and back for all conference delegates having a Party Ticket.
Meeting point: 1845 in front of the main entrance of the International Congress Center Dresden (ICCD). The trams then start at 1900 from the tram station "Kongresszentrum".

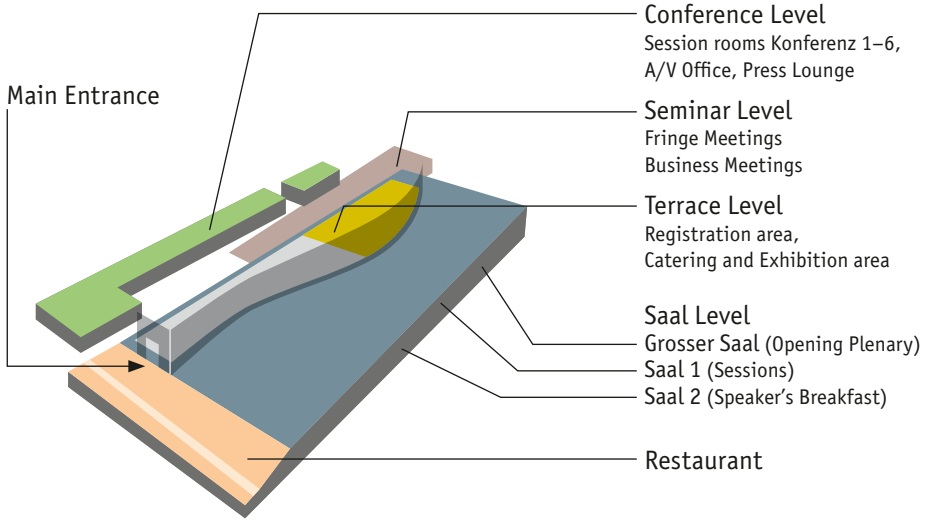
The DATE Party is co-sponsored by the City of Dresden.

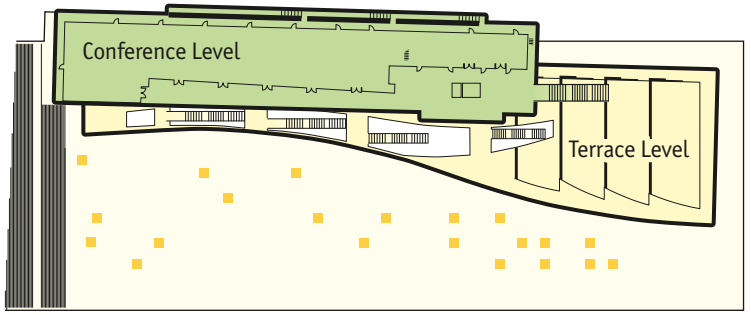
Interactive Presentations

Interactive presentations will take place from Tuesday, March 25, 2014 until Thursday, March 27, 2014 on the Conference Level, Foyer. → See page 8

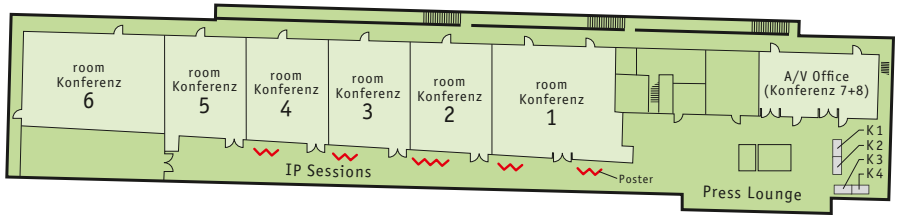
International Congress Center Dresden (ICCD)



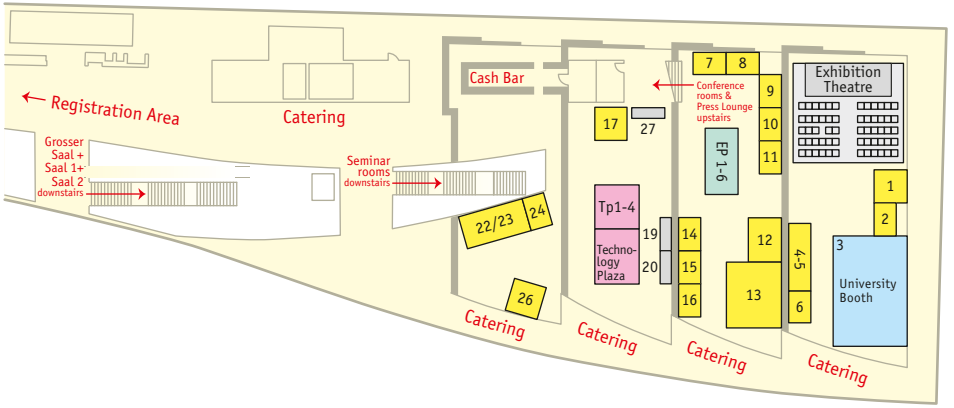




Conference Level



Terrace Level



Company	Booth
3D InCites, LLC	K 2
ALMA - ALgorithm parallelization for Multicore Architectures	EP 6
Blue Pearl Software	24
Center for Advancing Electronics Dresden (cfaed)	4+5
City of Dresden, Office of Economic Development	13
CLERECO – Cross-Layer Early Reliability Evaluation for the Computing cOntinuum	EP 4
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CREATIVE CHIPS GmbH	19
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EDA Confidential	K 3
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European Project Cluster on Mixed-Criticality Systems (DREAMS, PROXIMA, CONTREX, MultiPARTES)	EP 1
EUROPRACTICE	1
EuroTraining – Training in Nanoelectronics	EP 2
FlexTiles Consortium	EP 5
Fraunhofer EMFT	TP 3
Fraunhofer Institute for Integrated Circuits IIS	12
Incentia	20
Methodics	15

Company	Booth
Micronews Media, powered by Yole Développement	K 1
MOSIS	20
MultiPARTES	EP 1
MunEDA GmbH	14
now publishers inc.	27
OneSpin Solutions GmbH	26
ProPlus Design Solutions, Inc.	9
PROXIMA	EP 1
RacyICs GmbH	TP 1
SFB HAEC (TU Dresden)	6
SGS INSTITUT FRESENIUS GmbH	13
Silicon Saxony e.V.	13
SPRINGER	22+23
Synflow	8
Tanner EDA	20
TOSHIBA	16
University Booth	3
WIBRATE – Wireless, Self-Powered Vibration Monitoring and Control for Complex Industrial Systems	EP 3
Wirtschaftsförderung Sachsen GmbH (WFS)	13
X-FAB Group	13
Zentrum Mikroelektronik Dresden AG	13 & TP 4

booth K 2

3D InCites, LLC

Contact: Françoise von Trapp

3DInCites
605 E. Grant Street, Ste. 106
Phoenix, AZ 85004
United States

Phone: +1 978 340-0773

Email: francoise@3dincites.com
Website: www.3DinCites.com

First launched in 2009, 3D InCites is a community platform that is the only online resource devoted exclusively to 2.5D and 3D integration technologies. 3D InCites is a resource for industry news, technology innovation, market analysis and opinion. As such, it provides a place to learn, share, engage and collaborate with fellow 2.5D and 3D enthusiasts. For 3D IC integration to happen requires open collaboration across the supply chain. Therefore, 3D InCites strives to inform key decision makers about progress in technology development, design, standards, and infrastructure in order to realize commercial production of 2.5D and 3D technologies. 3D InCites has grown to a registered membership of over 1300 with many additional visitors who stop by just to keep up with what's happening in the world of 3D.

booth EP 6

ALMA - ALgorithm parallelization for Multicore Architectures

Contact: Jürgen Becker

Karlsruhe Institute of Technology (KIT)
Institute for Information Processing Technologies
Engesserstr. 5
76131 Karlsruhe
Germany

Email: becker@kit.edu
Website: www.alma-project.eu

Not only traditional PCs but also novel chips in consumer electronics like PDAs or mobile phones are based on multiprocessor systems-on-chip (MPSoC). Programming such embedded systems suffers from a complex tool-chain and programming process.
The ALMA project aims to mitigate this problem through the introduction and exploitation of a Scilab - based tool-chain, which enables the efficient mapping of applications on multiprocessor platforms with a high level of abstraction. Scilab is an open source, cross-platform numerical computational package and a high-level, numerically oriented programming language. ALMA will develop a holistic toolset that will enable faster uptake of embedded multicore technologies, faster time to market and reduced development cost with significant impact on product innovation and consumer prices.
ALMA will define semantics for parallelism that will be introduced in Scilab and develop an innovative approach for parsing input descriptions with annotations for parallelism. Algorithms and tools will be developed for (a) the estimation of the required hardware resources to realize the targeted applications within performance constraints, and (b) the identification of potential partitions and schedules of these, using optimization techniques, utilizing the different resources of the underlying architectures. The tools allow for an iterative algorithm optimization from a high level of abstraction and will be applied in two state-of-the-art architectures provided by Recore and KIT. The resulting gain of the ALMA approach is expected to be twofold: faster design space exploration and faster time to market.

PRODUCT FINDER

Embedded Software Development:
Compilers

booth 24

Blue Pearl Software

Contact: Murielle Lacombled

Blue Pearl Software
4677 Old Ironsides Drive, Suite 390
Santa Clara CA 95054
United States

Phone: +33 616 354 892

Email: murielle@bluepearlsoftware.com
Website: www.bluepearlsoftware.com

Blue Pearl Software automates IP and FPGA verification before debug. From an HDL description, designers run FPGA-centric structural checks for Xilinx and Altera. Blue Pearl's unique clock domain crossing analysis includes checks through CORE Generator™ and MegaCore™ functions using Blue Pearl's Grey Cell™ methodology. Blue Pearl automatically generates SDC timing constraints for downstream tools from Altera, Cadence, Mentor, Synopsys and Xilinx.

booth 4+5

Center for Advancing Electronics Dresden (cfaed)

Contact: Birgit Holthaus

TU Dresden
01062 Dresden
Germany

Phone: +49 351 463 42848
Fax: +49 351 463 41099

Email: birgit.holthaus@tu-dresden.de
Website: www.tu-dresden.de/cfaed

The Cluster of Excellence 'Center for Advancing Electronics Dresden' (cfaed) of Technische Universität Dresden comprises eleven research institutes in Saxony. Further members are the Technische Universität Chemnitz, two Max Planck Institutes, two Fraunhofer Institutes, two Leibniz Institutes and the Helmholtz-Research Center Dresden-Rossendorf. About 300 scientists are working in nine research paths to investigate completely new technologies for electronic information processing. These technologies are inspired by innovative materials such as silicon nanowires, carbon nanotubes or polymers or based on completely new conceptions such as the chemical chip or circuit fabrication methods by self-assembling structures e.g. DNA-Origami. The orchestration of these new devices into heterogeneous information processing systems with focus on their resilience and energy-efficiency is also part of cfaed's research program. To complement the Cluster, the Collaborative Research Center (CRC) 912 'Highly Adaptive Energy-Efficient Computing' (HAEC) has been integrated in cfaed. Both, cfaed and HAEC, are coordinated by Prof. Dr.-Ing. Dr. h.c. Gerhard Fettweis, who also holds the Vodafone Chair Mobile Communications Systems at TU Dresden.
The Dresden Center for Nanoanalysis (DCN) – an interdisciplinary technological platform in the field of nanoscale materials analysis – is also connected to cfaed.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Power & Optimisation

System-Level Design:
Behavioural Modelling & Analysis
Acceleration & Emulation
Hardware/Software Co-Design

Embedded Software Development:
Real Time Operating Systems
Software/Modelling

booth 13

City of Dresden Office of Economic Development

Contact: Michael Kaiser

City of Dresden
Office of Economic Development
Ammonstraße 74
01067 Dresden
Germany

Phone: +49 351 4888700
Fax: +49 351 4888702

Email: wirtschaftsfoerderung@dresden.de
Website: www.dresden.de/business

Network Thinking - Microelectronics in Dresden
- Competencies: Research & Development, IC Design, Photomasks, Chip Manufacturing, Packaging, Equipment, Software
- The Economic Development Office of the City of Dresden is your contact and partner as enterpreneur or investor. Our service ensures that your investment in Dresden can be realised without delay.

Welcome to Dresden!

booth EP 4

CLERECO – Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

Contact: Stefano Di Carlo

Politecnico di Torino
Control and Computer Engineering Department
Corso Duca degli Abruzzi 24
10129 Torino
Italy

Email: stefano.dicarlo@polito.it

Website: www.clereco.eu

Advanced multifunctional computing systems realized in forthcoming technologies hold the promise of a significant increase of the computational capability that will offer end-users ever improving services and functionalities. However, the same path that is leading technologies toward these remarkable achievements is also making electronic devices increasingly unreliable. Reliability of electronic systems is therefore a key challenge for the whole

information and communication technology and must be guaranteed without penalizing or slowing down the characteristics of the final products.
CLERECO research project (http://www.clereco.eu), a FP7 Collaboration Project involving Politecnico di Torino (Italy), National and Kapodistrian University of Athens (Greece), LIRMM (France), Intel Corporation Iberia S.A. (Spain), Thales SA (France), Yogitech spa (Italy) and ABB AS (Norway), recognizes early accurate reliability evaluation as one of the most important and challenging tasks toward this goal. Being able to precisely and early evaluate the reliability of a system means being able to carefully plan for specific countermeasures rather than resorting to worst-case approaches.
The proposed CLERECO framework for efficient reliability evaluation and therefore efficient exploitation of reliability oriented design approaches starting from early phases of the design process will enable circuit integration to continue at exponential rates and enable the design and manufacture of future systems for the computing continuum at a minimum cost contrary to existing worst-case-design solutions for reliability. The applications of such chips will play a major role in several fields ranging from avionics, automobile, smartphones, mobile systems, and future servers utilized in the settings of several types of HPC systems.

★ booth 17

CMP: Circuits Multi-Projects

Contact: Bernard Courtois

CMP: Circuits Multi-Projects
46 avenue Felix Viallet
38031 Grenoble
France

Phone: +33 476574617
Fax: +33 476473814

Email: cmp@imag.fr

Website: cmp.imag.fr

CMP is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 1000 Institutions from 70 countries have been served, more than 6700 projects have been prototyped through 800 manufacturing runs, and 60 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and AMS down to 28 nm FDSOI, 3D-IC from TEZZARON/GLOBALFOUNDRIES. MEMS are available on various processes: specific MEMS technologies (PolyMUMPS, SOIMUMPS, MetalMUMPS from MEMSCAP), THELMA from STMicroelectronics, MIDIS from TELEDYNE DALSA and bulk micromachining from AMS. Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ceramic packages.

PRODUCT FINDER

ASIC and SOC Design:
MEMS Design

Services:
Prototyping
Foundry & Manufacturing

★ booth 7

Codasip

Contact: Karel Masarik

Codasip Ltd.
Bozetechova 1/2
612 66 Brno
Czech Republic

Phone: +420608132875
Fax: +420541 211 479

Email: info@codasip.com
Website: www.codasip.com

Codasip delivers leading-edge IP and EDA tools to enable adoption of Application Specific Instruction Set Processors (ASIP's). ASIP's utilize dedicated instructions to accelerate software and are at the heart of applications such as software defined radio and computer vision - delivering very high performance with low power. Codasip's unique technology makes ASIP adoption as simple and easy as standard embedded processor cores.
The Codasip® Framework provides an all-in-one development environment for ASIP design, verification, programming and debugging. Codasip® Framework shortens development time substantially when compared to competing ASIP design platforms automating many of the otherwise time consuming and error prone tasks, while at the same time delivering higher performance ASIPs. Leveraging open technologies and standards throughout ensures integration with any design and programming environment - these technologies cover synthesizable RTL, UVM and TLM-based verification and LLVM-based programming tool-chain for the target processor. A wide variety of processor verification models are automatically generated supporting virtual prototyping, system simulation and detailed debug. The Codasip® Framework also includes support for multi-processor profiling, verification, programming, and debug.
Codix IP Cores provide a proven extensible processing platform that can be adapted to a customer's needs. These cores are an ideal starting point for customers new to ASIP design allowing for rapid integration while still delivering a great deal of flexibility. A variety of Codix Cores are available covering DSP, RISC, and VLIW technologies.

PRODUCT FINDER

ASIC and SOC Design:
Verification

System-Level Design:
Hardware/Software Co-Design

Services:
Prototyping

Embedded Software Development:
Compilers
Debuggers

Semiconductor IP:
CPUs & Controllers
Processor Platforms

Application-Specific IP:
Digital Signal Processing
Multimedia Graphics

★ booth 11

Concept Engineering GmbH

Contact: Gerhard Angst

Concept Engineering GmbH
Boetzinger Str. 29
79111 Freiburg
Germany

Phone: +49 761 470940
Fax: +49 761 4709429

Email: info@concept.de
Website: www.concept.de

Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers, FPGA and IC designers.

NIview WidgetsTM – a family of schematic generation and visualization engines (Tcl/TK, MFC, Qt, Java, Perl/Tk, wxWidgets) that can be easily integrated into EDA tools.

RTLVisionTM PRO – a graphical debugger for SystemsVerilog, Verilog and VHDL based designs.

GateVision® PRO – a customizable debugger for Verilog, LEF/DEF and EDIF based designs.

SpiceVision® PRO – a customizable debugger for SPICE based designs.

StarVision® PRO - a customizable mixed-signal and mixed-language debugger.

PRODUCT FINDER

ASIC and SOC Design:
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design

Test:
Design for Test

★ booth EP 1

CONTREX

Contact: Kim Grüttner

OFFIS – Institute for Information Technology
Escherweg 2
26121 Oldenburg
Germany

Phone: +49 441 97 22 228

Email: kim.gruettner@offis.de
Website: contrex.offis.de

CONTREX (Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties) will enable energy-efficient and cost aware design through analysis and optimization of real-time, power, temperature and reliability with regard to application demands at different criticality levels.

booth 19

CREATIVE CHIPS GmbH

Contact: Anne Stroot

CREATIVE CHIPS GmbH
Im Bubenstück 1
55411 Bingen
Germany

Phone: +49-6721-98722-14

Fax: +49-6721-98722-70

Email: anne.stroot@creativechips.com
Website: www.creativechips.com

CREATIVE CHIPS offers the complete service of a Fabless Semiconductor Vendor. From specification, complete IC development, sample production, qualification for series production and the documentation up to mass production and volume deliveries of ASICs and ASSPs, tested in our in-house test department.
The company´s headquarter is located in Bingen /Rhein in Germany with design center in Dresden and an Asia sales office located in Israel. As an automotive supplier the company is certified according to the quality standard for the automotive industry ISO/TS 16949.
CREATIVE CHIPS offers the following services:

- Turn-key circuit design, sample production, evaluation and qualification for mass production of a custom specific mixed-signal ASIC or pure analog but also complex digital integrated circuits – ASICs and standard ICs
- Test and delivery of bulk production IC volumes to our customers regarding flexible and defined quality and logistic demands with backend services as tape & reel, dry packing or long time storage of parts
- complete supply chain management for IC production
- FPGA / ASIC conversion
  ASICs from CREATIVE CHIPS are used in various applications like:
- Automotive electronics (f.e. robust sensor and control circuits for car environment)
- Automation industry (f.e. optical transimpedance amplifiers with integrated sensors, bus interface ICs, smart power supply circuits)
- Multimedia (f.e. broadband optical data transmission systems, RF data transmission in 433/868 MHz band, buck-boost converters)
- Consumer electronics and white goods (f.e. motor drivers, battery charging circuits).

PRODUCT FINDER

ASIC and SOC Design:
Analogue and Mixed-Signal Design
RF Design

Test:
Test Automation (ATPG, BIST)
Mixed-Signal Test

Services:
Design Consultancy
Prototyping

Semiconductor IP:
Analogue & Mixed Signal IP
CPUs & Controllers
Encryption IP

Application-Specific IP:
Analogue & Mixed Signal IP

booth TP 2

Dream Chip Technologies GmbH

Contact: Jens Benndorf

Dream Chip Technologies GmbH
Steinriede 10
30827 Garbsen
Germany

Phone: +49 5131 90805-0

Fax: +49 5131 90805-102

Email: info@dreamchip.de
Website: www.dreamchip.de

Dream Chip Technologies (DCT) - located in Garbsen near Hanover - is an independent fabless microelectronic engineering company with a long history in development of embedded Software and PCBs and in FPGAs and ASICs for highly complex System-on-Chips (SoCs). Next to pure development, DCT offers also the delivery of the developed products.
Founded as SICAN more than 20 years ago and belonging as SCI-WORX to Infineon for several years, DCT comes today with outstanding know-how in the development of challenging microelectronics especially for video and imaging applications.
DCT focuses on microelectronic manufacturers for the industrial and the consumer market who want to offer market-driven products in an optimum time frame, without permanently being able to provide the required capacity for development.
Our customers are mainly product makers in the automotive, industrial and medical area, for professional video applications and for consumer electronics.

Next to the design service for customers, DCT develops and delivers also own technologies and products. As well as technologies for 2D and 3D image processing pipelines and for video compression functionality this also includes a Super Slow Motion module which extends the operational area of simple industrial cameras without integrated image processing capability and which is used in professional slow motion systems.
Founded at the beginning of 2010, DCT today employs 35 development engineers; the yearly turnover is around EUR 4 million.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification

System-Level Design:
Acceleration & Emulation
Hardware/Software Co-Design
PCB & MCM Design

Test:
Design for Test
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
System Test

Services:
Design Consultancy
Prototyping
Training

Embedded Software Development:
Real Time Operating Systems
Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms
Development Boards

Semiconductor IP:
Configurable Logic IP
Embedded FPGA
Embedded Software IP
Encryption IP
On-Chip Bus Interconnect
On-Chip Debug
Processor Platforms
Synthesizable Libraries

Application-Specific IP:
Data Communication
Digital Signal Processing
Multimedia Graphics
Networking
Security
Telecommunication
Wireless Communication

booth EP 1

DREAMS

Contact: Roman Obermaisser

Universität Siegen
Department Elektrotechnik und Informatik
Lehrstuhl Embedded Systems
Hölderlinstraße 3
57076 Siegen
Germany

Phone: +49 271 740 3332

Email: roman.obermaisser@uni-siegen.de
Website: www.dreams-project.eu

DREAMS (Distributed Real-time Architecture for Mixed criticality Systems) will develop a cross-domain architecture and design tools for networked complex systems where application subsystems of different criticality, executing on networked multi-core chips, are supported.

booth K 3

EDA Confidential

Contact: Peggy Aycinena

EDA Confidential
San Mateo
CA, 94402-2241
United States

Phone: +1 650-579-7952
Fax: +1 650-579-7952

Email: peggy@aycinena.com
Website: www.aycinena.com

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes “Recipes”, Freddy Santamaria’s “Gourmet Corner”, as well as “Voices” of other contributing authors, “Off the Record” op-ed pieces, and “Conference” coverage.

booth 20

EDA Solutions LTD

Contact: Lynne Wright

EDA Solutions Limited
Unit A5, Segensworth Business Centre
Segenswoth Road, Fareham, Hants PO15 5RQ
United Kingdom

Phone: +44 1489 564 253
Fax: +44 1489 557 367

Email: lynnewright@eda-solutions.com
Website: www.eda-solutions.com

For over 10 years EDA Solutions have provided cost effective and highly productive IC Design software and manufacturing services to European industry. Visit us at our stand to find out more about the digital synthesis tools from Incentia, the analog/mixed signal design, layout and verification tools from Tanner EDA and the MPW and low volume production services from MOSIS.

booth K 4

Elektronik i Norden

Contact: Göte Fagerfjäll

Phone: +46 8 540 865 12

Email: goete.fagerfjaell@elinor.se
Website: www.elinor.se

Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed copies proves we are the major electronics paper in this area. We publish news, comments and in-depth technical articles.

booth 10

Elsevier BV

Contact: James Palser

Elsevier BV
Radarweg 29
1043 NX Amsterdam
The Netherlands

Phone: +44 1865 843237

Email: j.palser@elsevier.com
Website: www.elsevier.com/computerscience

ELSEVIER – COMPUTER SCIENCE
Elsevier is a leading international publisher of Computer Science journals, books and electronic products.
By delivering first class information and innovative tools, we continue to refine our portfolio to serve the research need of industry professionals, researchers and students worldwide.
We are proud to play an integral part within the computer science community and to participate in the advancement of this field. All our journals are available online via ScienceDirect (www.sciencedirect.com) the essential information resource for over 14 million scientists worldwide.
Visit our booth to meet publishers and editors and view the latest journal information on microelectronics and electronic system design. We will be introducing our new editor for Microelectronics Journal and celebrating the 30th Anniversary of Microelectronic Engineering Journal with various activities.
We look forward to meeting you!

booth 2

Embedded Computing Specialists

Contact: Bertrand Rousseau

Embedded Computing Specialists
Av. de Messidor, 213/3
1180 Brussels
Belgium

Phone: +32 498/105 795

Email: contact@ecspec.com
Website: www.ecspec.com

Embedded Computing Specialists provides engineering services and solutions for embedded computing. We specialize in R&D projects where you are looking for technology leap or performance breakthrough.

ECS draws its strength from highly qualified engineers with Ph.D. in computer architecture for embedded systems. Our expertise is based on nearly ten years of track records in advanced R&D projects and product development. Our strong scientific background allows us to quickly find the best solutions for your project challenges.
We have a cross-layer expertise ranging from OS down to ASIC & FPGA physical level. It allows us to quickly understand and evaluate the impact of a technology choice on the final performances of a particular application. This transverse knowledge is a key asset to cope with today's multicore and heterogeneous platform challenges.

PRODUCT FINDER

System-Level Design:
Behavioural Modelling & Analysis
Acceleration & Emulation
Hardware/Software Co-Design

Services:
Design Consultancy
Prototyping
Training

Embedded Software Development:
Compilers
Real Time Operating Systems
Debuggers
Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Workstations & IT Infrastructure

Semiconductor IP:
Configurable Logic IP
CPUs & Controllers
Processor Platforms

Application-Specific IP:
Digital Signal Processing
Multimedia Graphics

booth EP 1

European Project Cluster on Mixed-Criticality Systems (DREAMS, PROXIMA, CONTREX, MultiPARTES)

Contact: Kim Grüttner

OFFIS FuE Bereich Verkehr
R&D Division Transportation
Escherweg 2
26121 Oldenburg
Germany

Phone: +49 441 9722-228/278

Email: kim.gruettner@offis.de
Website: www.offis.de

The European Project Cluster on Mixed-Criticality Systems has been started in October 2013 and consists of the following European projects, attacking several challenges and aspects of Mixed-Criticality Systems:

DREAMS, PROXIMA, CONTREX and MultiPARTES. For a detailed description on the individual projects, please have a look at the exhibitor list.

booth 1

EUROPRACTICE

Contact: Carl Das

IMEC vzw
Kapeldreef 75
3001 Leuven
Belgium

Phone: +32 16 28 12 48

Email: Carl.Das@imec.be
Website: www.imec.be

The EUROPRACTICE Service offers CAD tools for education, low cost and easy access to ASIC prototype and small volume fabrication. The service is offered by IMEC (B), STFC (UK) and Fraunhofer IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW runs whereby many designs are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemi, austiamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on

MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up to more than 5000 wafers per year per ASIC.

PRODUCT FINDER

Test:
Design for Test
Design for Manufacture and Yield
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test

Services:
Prototyping

Semiconductor IP:
Analogue & Mixed Signal IP
Physical Libraries

★ booth EP 2

EuroTraining – Training in Nanoelectronics

Contact: Annette Locher

FSRM – Swiss Foundation for Research in Microtechnology
Ruelle DuPeyrou 4
2001 Neuchâtel
Switzerland

Phone: +41 32 720 09 30

Email: locher@fsrm.ch
Website: www.eurotraining.net

EuroTraining develops and runs the website www.eurotraining.net offering access to hundreds of courses, summer schools, lecturing material and on-line tutorials in the field of nanoelectronics and micro-nano systems.

The service addresses industry and universities which are also encouraged to share the basic development of courses, text books and training material on the EuroTraining website.

Course providers, universities or European project can announce their training offer on eurotraining.net for free. The events can also be included in the monthly newsletter to over 10'000 addresses. Contact: <mailto:eurotraining polito [dot] it> eurotraining polito [dot] it.

Furthermore, Eurotraining establishs the training requirements of EU companies with production or development in Far East and develops dedicated webinars which will be available on www.eurotraining.net.

★ booth EP 5

FlexTiles Consortium

Contact: Philippe Millet

THALES R&T
Campus Polytechnique
1 avenue Augustin Fresnel
91767 Palaiseau Cedex
France

Phone: +33 1 69 41 60 49
Fax: +33 1 69 41 60 01

Email: philippe.millet@thalesgroup.com
Website: www.flextiles.eu

A major challenge in computing is to leverage multi-core technology to develop energy-efficient high performance systems. This is critical for embedded systems with a very limited energy budget as well as for supercomputers in terms of sustainability. Moreover the efficient programming of multi-core architectures, as we move towards manycores with more than a thousand cores predicted by 2020, remains an unresolved issue. The FlexTiles project will define and develop an energy-efficient yet programmable heterogeneous manycore platform with self-adaptive capabilities.
The manycore will be associated with an innovative virtualisation layer and a dedicated tool-flow to improve programming efficiency, reduce the impact on time to market and reduce the development cost by 20 to 50%.
FlexTiles will raise the accessibility of the manycore technology to industry – from small SMEs to large companies – thanks to its programming efficiency and its ability to adapt to the targeted domain using embedded reconfigurable technologies.
Contract number: 288248
Project coordinator: THALES

★ booth TP 3

Fraunhofer EMFT

Contact: Pirjo Larima-Bellinghoven

Fraunhofer EMFT
Hansastraße 27d
80686 München
Germany

Phone: +49 89 54759 542

Email: pirjo.larima-bellinghoven@emft.fraunhofer.de
Website: www.emft.fraunhofer.de

Fraunhofer EMFT conducts cutting-edge applied research into sensors and actuators for man and the environment. The core competences of the research departments in Munich and Regensburg with hundred employees include: silicon technology, flexible electronics, chemical sensor materials and the capability of system integration. Each of these core competences in its own right allows new kinds of sensors and actuators to be created. But the real strength of Fraunhofer EMFT lies in the interaction between these areas: after all, innovations often emerge where technologies reach their limits and begin to cross-fertilize. This enables the creation of innovative solutions for various business and application areas. The business area "Design and Test" offers customized services from development of integrated circuits to integrated components as well as complete systems and equipment. The services portfolio also includes multiparametric characterization and reliability prognoses for the planned application.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design

System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
PCB & MCM Design

Test:
Test Automation (ATPG, BIST)
Silicon Validation
Mixed-Signal Test
System Test

Services:
Design Consultancy
Prototyping
Training

Embedded Software Development:
Software/Modelling

Semiconductor IP:
Analogue & Mixed Signal IP
Verification IO

Application-Specific IP:
Analogue & Mixed Signal IP
Data Communication
Telecommunication
Wireless Communication

★ booth 12

Fraunhofer Institute for Integrated Circuits IIS

Contact: Melanie Ruge

Fraunhofer Institute for Integrated Circuits IIS
Design Automation Division EAS
Zeunerstr. 38
01069 Dresden
Germany

Phone: +49 351 4640 707
Fax: +49 351 4640 703

Email: melanie.ruge@eas.iis.fraunhofer.de
Website: www.eas.iis.fraunhofer.de

The Fraunhofer Institute for Integrated Circuits IIS is one of Germany's most important research facilities for the development of microelectronic systems. The scientists in the Design Automation Division EAS in Dresden work on new methods of modeling, simulation and optimization of systems as well as debugging, analysis and formal verification. These methods ensure that developed complex electronic and mechatronic systems meet the required specifications at every design stage and errors are identified before components are built.
By applying knowledge and innovative solutions, the division aims at achieving a faster, more efficient and last but not least a more cost saving design of products. One goal of particular importance is a high design quality despite ever more complex systems. Thus, our scientists take account of the growing requirements concerning reliability and robustness of systems.
The EAS Division is involved in national and international networks in research and numerous standardization activities. Its results of work and developments are applied in microelectronics and its domains, such as communication technology, automotive industry or automation.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design

System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Hardware/Software Co-Design
Package Design
PCB & MCM Design

Test:
Design for Test
Design for Manufacture and Yield
Test Automation (ATPG, BIST)
Mixed-Signal Test
System Test

Embedded Software Development:
Real Time Operating Systems
Software/Modelling

Semiconductor IP:
Analogue & Mixed Signal IP

Application-Specific IP:
Networking
Wireless Communication

★ booth 20

Incentia

Contact: Lynne Wright

EDA Solutions Limited
Unit A5, Segensworth Business Centre
Segenswoth Road, Fareham, Hants PO15 5RQ
United Kingdom

Phone: +44 1489 564 253
Fax: +44 1489 557 367

Email: lynnewright@eda-solutions.com
Website: www.eda-solutions.com

Incentia Design Systems, Inc. is a leading provider of advanced Timing and Signal Integrity Analysis, Design Closure, and Logic Synthesis software for multi-million-gate nanometre designs. Incentia patented technologies provide the fastest Static Timing Analysis (STA) tool in the market today. Incentia's products are in use at leading semiconductor, fabless IC design, systems, and design service companies worldwide and have produced numerous customer tape-outs, including those using advanced 40nm technologies and designs over 50 million gates. Incentia are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to our stand or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

ASIC and SOC Design:
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)

Test:
Design for Test
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan

★ booth 15

Methodics

Contact: Christian Burisch

Methodics, Inc.
2370 Market St, #506
San Francisco, CA 94114
United States

Phone: +1 415 354 5726
Fax: +1 415 354 5726

Email: christian.burisch@methodics.com
Website: www.methodics.com

Methodics delivers state-of-the-art semiconductor data management (DM) for analog, digital, and SoC design teams.
Integration of IP Lifecycle Management with powerful analytics and industry-standard DM enables Methodic's solutions to significantly reduce design cost; making design more efficient, predictable and with higher quality. Advanced IP distribution infrastructure, cataloging, and workspace management ensure that no matter where designers are located they have full visibility into the IP available to them and can easily access that data regardless of its location.
Methodic's clients for analog and digital designers integrate natively with existing design environments making DM seamless to the users. Building our solutions on top of standard Subversion and Perforce infrastructure ensures data is safe, always available, and that the tools can take advantage of the latest advancements from the software development community.
Our highly scalable and industry proven solutions are ideal for small specialized IP design teams, as well as large multinational, multisite, SoC design teams.
For further information, visit www.methodics.com.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Analogue and Mixed-Signal Design

Services:
Data Management and Collaboration
IP e-commerce & Exchange

★ booth K 1

Micronews Media, powered by Yole Développement

Contact: Camille Veyrier

Yole Développement
Le Quartz, 75 Cours Emile Zola
69100 Villeurbanne – Lyon
France

Phone: +33 472 83 01 01

Email: veyrier@yole.fr
Website: i-Micronews.com

Founded in 1998, Yole Développement has grown to become a group of companies providing marketing, technology and strategy consulting, media in addition to corporate finance services. With a strong focus on emerging applications using silicon and/or micro manufacturing, Yole Développement group has expanded to include more than 50 associates worldwide covering MEMS, Compound Semiconductors, LED, Image Sensors, Optoelectronics, Microfluidics & Medical, Photovoltaics, Advanced Packaging, Manufacturing, ok Nanomaterials and Power Electronics. The group supports industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

MEDIA & EVENTS ACTIVITY:
- i-Micronews.com, online disruptive technologies website
- Weekly WebTalk
- @Micronews, weekly e-newsletter
- Technology Magazines dedicated to MEMS, Advanced Packaging, LED and Power Electronics
- Communication & webcasts services
- Events: Yole Seminars, Market Briefings

★ booth 20

MOSIS

Contact: Lynne Wright

EDA Solutions Limited
Unit A5, Segensworth Business Centre
Segenswoth Road, Fareham, Hants PO15 5RQ
United Kingdom

Phone: +44 1489 564 253
Fax: +44 1489 557 367

Email: lynnewright@eda-solutions.com
Website: www.eda-solutions.com

MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions around the world. Processes offered include SOS, SOI, CMOS and SiGe BiCMOS, in geometries from 0.7um to 32nm, from the foundries IBM, TSMC, ON Semiconductor, austriamicrosystems, Globalfoundries, and Peregrine. MOSIS are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to our stand or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

Services:
Prototyping
Foundry & Manufacturing

booth EP 1

MultiPARTES

Contact: Salvador Trujillo

IKERLAN-IK4
JM Arizmendiarrieta, 2
20500 Arrasate (Gipuzkoa)
Spain

Phone: +34 689022454

Email: STrujillo@ikerlan.es
Website: www.multipartes.eu

MultiPARTES (Multicore Partitioned Systems) aims at developing tools and solutions for building trusted embedded systems with mixed criticality components on multicore platforms based on the XtratuM hypervisor.

booth 14

MunEDA GmbH

Contact: Jin Qiu

MunEDA GmbH
Stefan-George-Ring 29
81929 Munich
Germany

Phone: +49 89 930 86 330
Fax: +49 89 930 86 407

Email: info@muneda.com
Website: www.muneda.com

MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA´s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA´s solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

booth 27

now publishers inc.

Contact: James Finlay

now publishers inc.
PO Box 179
2600 AD Delft
The Netherlands

Phone: +31 6 1448 3632

Email: james.finlay@nowpublishers.com
Website: www.nowpublishers.com

Publishers of the highly acclaimed FOUNDATIONS AND TRENDS journals. Peer-reviewed surveys, reviews and tutorials in electronic design automation. Visit our booth to browse the available titles and meet the publisher. All print titles available for the special DATE price of €35. www.nowpublishers.com/eda

booth 26

OneSpin Solutions GmbH

Contact: Oliver Habeck

OneSpin Solutions GmbH
Nymphenburger Str. 20a
80335 Munich
Germany

Phone: +49 89 99013498

Fax: +49 89 99013 400

Email: oliver.habeck@onespin-solutions.com
Website: www.onespin-solutions.com

OneSpin Solutions is a pioneer of advanced, award winning formal verification technologies, incubated at Infineon and leveraging 300+ engineering years of development and applications experience. The company's product line includes plug & play design analysis requiring no knowledge of formal methods, to powerful, exhaustive, coverage-driven property verification and sequential FPGA and ASIC Equivalency Checking. Excelling in ease-of-use, high-performance and accessibility, OneSpin's products have been leveraged by a large number of electronic product and semiconductor companies on many leading edge designs. The company maintains its headquarters and engineering teams in Munich, Germany and operates on a global basis.

PRODUCT FINDER

ASIC and SOC Design:
Verification

booth 9

ProPlus Design Solutions, Inc.

Contact: Amit Nanda

ProPlus Design Solutions, Inc.
2025 Gateway Place, Suite 130
San Jose, CA 95110
United States

Phone: +1 408-459-6067

Email: amit@proplussolution.com
Website: www.proplussolution.com

ProPlus Design Solutions, Inc. delivers Electronic Design Automation (EDA) solutions with the mission to enhance the link between design and manufacturing. It is the global leader for SPICE modeling solutions and the leading technology provider for unique Design-for-Yield (DFY) products that integrate the key DFY components –– advanced device modeling software, a parallel SPICE simulation circuit simulator and hardware-validated statistical variation analysis tools. Products include: BSIMProPlus™/Model Explorer™, a modeling technology platform for nanometer devices; NoisePro™/9812B/9812D, the golden solution for low-frequency 1/f noise and Random Telegraph Signal (RTS) noise characterization and process monitoring; NanoSpice™, a high-capacity, high-performance parallel SPICE simulator for giga-scale circuit simulation; and NanoYield™/NanoExplorer™, a variation analysis platform for yield versus power, performance and area trade-off of memory, analog and digital circuit designs. ProPlus Design Solutions has R&D centers in the San Jose, Calif. and Beijing and Jinan, China, with sales offices in Tokyo, Japan, Hsinchu, Taiwan, and Shanghai, China.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
RF Design

Test:
Design for Manufacture and Yield

Services:
Design Consultancy

booth EP 1

PROXIMA

Contact: Francisco J. Cazorla

Barcelona Supercomputing Center - Centro Nacional de Supercomputación
C/Jordi Girona, 29, Ed. Nexus II, 3rd Pl.
08034 Barcelona
Spain

Phone: +34 93 413 7173

Email: francisco.cazorla@bsc.es
Website: www.proxima-project.eu

PROXIMA (PRObabilistic real?time control of miXed?crIticality Multicore and mAnycore systems) will define new hardware and software architectural paradigms based on the concept of randomization. It extends this approach across the hardware and software stack ensuring that the risks of temporal pathological cases are reduced to probabilistically quantifiable small levels.

booth TP 1

RacyICs GmbH

Contact: Holger Eisenreich

RacyICs GmbH
Graue-Presse-Weg 11
01445 Radebeul
Germany

Phone: +49 351 418872 10
Fax: +49 351 418872 99

Email: eisenreich@racyics.com
Website: www.racyics.com

RacyICs, an experienced fabless design house based in Dresden, Germany, offers design and implementation services for analog, mixed-signal and digital ICs. Working for leading European semiconductor companies for many years, the RacyICs team contributed to numerous successful chip designs down to 28nm feature size for automotive, consumer and communication applications. As GLOBALFOUNDRIES' channel partner with focus on advanced and leading edge technologies, RacyICs provides access to 28nm prototyping runs

(MPWs) and required design enablement services for European SMEs and academia. For more information, visit www.racyics.com.

PRODUCT FINDER

Services:
Design Consultancy
Prototyping
Data Management and Collaboration
IP e-commerce & Exchange
Foundry & Manufacturing
Training

Semiconductor IP:
Analogue & Mixed Signal IP
Embedded FPGA
Memory IP
On-Chip Bus Interconnect
Physical Libraries
Synthesizable Libraries

★ booth 6

SFB HAEC (TU Dresden)

Contact: Nicolle Seifert

TU Dresden, HAEC
Georg-Schumann-Straße 11
01062 Dresden
Germany

Email: nicolle.seifert@tu-dresden.de
Website: www.tu-dresden.de/sfb912

The collaborative research center HAEC is a first attempt to achieve high adaptivity and energy efficiency in such an integrated approach. At the circuit level, we focus on innovative ideas for optical and wireless chip-to-chip communication. At the network level, we research secure, high performance network coding schemes for wired and wireless board-to-board communication. Innovative results at the hardware/software interface level will include energy control loops, which allow hardware to adapt to varying software requirements and vice versa. Software development in general is supported by energy-aware runtimes, energy-aware resource, stream and configuration management schemes and by an analysis framework for high performance/low energy applications. New internet applications are supported by innovations in energy-aware service execution. And, last but not least, formal methods are developed to offer a new quality of assurance in our systems of tomorrow. Demonstrating our results in a joint prototype - the HAEC Box - our goal is to become a pace setter for industry and academia on the design of future energy efficient-computing systems.

★ booth 13

SGS INSTITUT FRESENIUS GmbH

Contact: Andre Möller

SGS INSTITUT FRESENIUS GmbH
Königsbrücker Landstr. 161
01109 Dresden
Germany

Phone: +49 351 8841 100

Fax: +49 351 8841 190

Email: andre.moeller@sgs.com
Website: www.institut-fresenius.sgsgroup.de

About SGS INSTITUT FRESENIUS
As one of the leading providers of laboratory analysis in Germany, SGS INSTITUT FRESENIUS has a strong reputation among manufacturers and retailers along the supply chain of the high-tech industry. The SGS INSTITUT FRESENIUS laboratory in Dresden offers testing services for microelectronics and nanostructures. The personnel is also specialized in the analysis and testing of material, surface and thin layers as well as in the analysis of process media. The experts analyse nanostructures and nanolayers with regard to their material-specific and structural properties. SGS INSTITUT FRESENIUS also provides services for microelectronic design as construction analysis, failure and damage analysis and FIB modification of integrated circuits. For all testing services the experienced personnel utilise leading edge chemical and physical analytical equipment. SGS INSTITUT FRESENIUS is part of the SGS Group.
About SGS
SGS is the world's leading inspection, verification, testing and certification company. SGS is recognised as the global benchmark for quality and integrity. With more than 80.000 employees, SGS operates a network of over 1.650 offices and laboratories around the world. SGS provides solutions across all industries. Through a unique global network SGS delivers independent results tailored to the precise needs of the industry or sector. Founded in 1878, the company is headquartered in Geneva.
Since 1920, SGS has been operating in Germany. SGS Group Germany provides inspection services for international trade, industrial goods, agriculture, the extractive industry and the consumer goods industry. The company works for producers and traders, governments and businesses, for suppliers and consumers alike.
More information:
www.sgsgroup.de /www.institut-fresenius.sgsgroup.de

★ booth 13

Silicon Saxony e.V.

Contact: Gitta Haupold

Silicon Saxony e.V.
Manfred-von-Ardenne-Ring 20
01099 Dresden
Germany

Phone: +49 351 8925 887
Fax: +49 351 8925 889

Email: info@silicon-saxony.de
Website: www.silicon-saxony.de

Silicon Saxony is Europe's most successful trade association for the semiconductor, microsystems, software and photovoltaic industries. We are connecting 300 commercial enterprises, research institutes, universities and public institutions. The competencies of our members represent the entire value creation chain of the microelectronics industry. In addition, the network is expanding to sectors as the energy and software industries. As a continuously growing and vital high-tech network, we understand ourselves as a communication and cooperation platform for our members. This promotes and stabilizes the economic development of our member companies. Intelligent partnerships among them enable knowledge transfer, synergies, business relationships and promote innovative power. At our joint booth, you can meet us and companies from Silicon Saxony, presenting their expertise in the field of microelectronics – a business sector Saxony has a European leadership role in!

★ booth 22+23

SPRINGER

Contact: Lothar Minicka

SPRINGER
Tiergartenstr. 17
69121 Heidelberg
Germany

Phone: +49 6221 4870
Fax: +49 6221 4878366

Email: lothar.minicka@springer.com
Website: www.springer.com

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★ booth 8

Synflow

Contact: Nicolas Siret

Synflow
2 rue de la Châtaigneraie, CS 17607
35576 Cesson-Sévigné
France

Phone: +33 299127902

Email: nicolas.siret@synflow.com
Website: www.synflow.com

Synflow SAS is an EDA start-up company that helps hardware designers increase their productivity by making design and verification easier. For this purpose, we develop and market EDA software based on a disruptive technology for IP and SoC design combining a new language called C~ (C flow) and an Eclipse-based IDE that verifies C~ designs and translates them (on-the-fly) into Verilog and VHDL. We also provides support for our software to help designers learning the C~ language faster and master the IDE, as well as advice and tips to write better C~ code to design IP cores and SoCs with the highest performance possible. We chose to create a new language to provide designers with a modern, hardware-oriented language that is more adapted to their needs than RTL – this language has the particularity of

allowing any kind of design to be created with ease and efficiency. We also made the choice of generating vendor-neutral, clean, readable Verilog and VHDL that respects the coding rules imposed or recommended by synthesizers and lint tools. Our users have succeeded in designing applications with a mix of control and dataflow up to 10x faster than using RTL with equivalent synthesis results.
The Synflow SAS company was founded by Nicolas Siret and Matthieu Wipliez, two PhDs specialized in hardware engineering and software engineering, who worked on models and code compilation with other researchers in the EU.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification

System-Level Design:
Behavioural Modelling & Analysis

Services:
Prototyping

Semiconductor IP:
Encryption IP
Synthesizable Libraries

Application-Specific IP:
Networking
Telecommunication

★ booth 20

Tanner EDA

Contact: Lynne Wright

EDA Solutions Limited
Unit A5, Segensworth Business Centre
Segenswoth Road, Fareham, Hants PO15 5RQ
United Kingdom

Phone: +44 1489 564 253
Fax: +44 1489 557 367

Email: lynnewright@eda-solutions.com
Website: www.eda-solutions.com

Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. Tanner are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to our stand or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design

Test:
Silicon Validation
Mixed-Signal Test

★ booth 16

TOSHIBA

Contact: Mari Takada

Toshiba Corporation
1-1, Shibaura 1-chome, Minato-Ku
Tokyo, 105-8001
Japan

Phone: +81 3 34573435

Email: mari.takada@toshiba.co.jp
Website: www.toshiba.co.jp/worldwide

In 1987, Toshiba invented NAND Flash technology. Today, Toshiba offers one of the industry's broadest line-ups of NAND Flash-based storage solutions—enabling a wide range of applications in the consumer, mobile, industrial, and enterprise markets. Extending its industry leadership in memory storage solutions, Toshiba offers an innovative new SDHC memory card, "FlashAir", which is the first to support the new Wireless LAN SD standard, iSDIO. "FlashAir" is an SD memory card with embedded wireless LAN functionality. It has a built-in web server function and a wireless LAN access point. If power is supplied to the card, FlashAir can work as a server. Files stored in FlashAir are accessible from smartphones, tablets or PCs through Wi-Fi. Ad-hoc local networks between FlashAir and mobile devices are established, so that Internet access or Wi-Fi access points are not needed. The API of FlashAir is disclosed on the developer site. https://flashair-developers.com
By using FlashAir, you can provide an on-site download service, accessible only at the venues. We have provided the proceedings download service at ASP-DAC this January and at SASIMI last October. There are some academic meetings which are planning to offer this onsite download service. Furthermore, FlashAir allows you both peer-to-peer transfers and uploads to and downloads from servers if the device supports iSDIO. FlashAir opens up many new possibilities. Please stop by our TOSHIBA booth to see some demos.

PRODUCT FINDER

Application-Specific IP:
Wireless Communication

★ booth 3

University Booth

Contact: Andreas Vörg (edacentrum),
Jens Lienig (TU Dresden)

edacentrum
Schneiderberg 32
30167 Hannover
Germany

TU Dresden
Helmholtzstraße 18
01069 Dresden
Germany

Phone: +49 511 762 19686 (Andreas Vörg)
Fax: +49 511 762 19695 (Andreas Vörg)

Email: university-booth@date-conference.com
Website: wwww.date-conference.com/group/exhibition/u-booth

The University Booth is part of the DATE 2014 exhibition programme and is sponsored by the DATE Sponsor Committee. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are presenting innovative hardware and software demonstrations. All demonstrations will take place during the exhibition within a dedicated time slot. The University Booth is organized by Jens Lienig (TU Dresden) and Andreas Vörg (edacentrum).

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RF Design

System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Acceleration & Emulation
Hardware/Software Co-Design
Package Design
PCB & MCM Design

Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test

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IP e-commerce & Exchange
Foundry & Manufacturing
Training

Embedded Software Development:
Compilers
Real Time Operating Systems
Debuggers
Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Workstations & IT Infrastructure

Semiconductor IP:
Analogue & Mixed Signal IP
Configurable Logic IP
CPUs & Controllers
Embedded FPGA
Embedded Software IP
Encryption IP
Memory IP
On-Chip Bus Interconnect
On-Chip Debug
Physical Libraries
Processor Platforms
Synthesizable Libraries
Test IP
Verification IO

Application-Specific IP:
Analogue & Mixed Signal IP
Data Communication
Digital Signal Processing
Multimedia Graphics
Networking
Security
Telecommunication
Wireless Communication

★ booth EP 3

WIBRATE - Wireless, Self-Powered Vibration Monitoring and Control for Complex Industrial Systems

Contact: Paul J. M. Havinga

University of Twente
Pervasive Systems
Drienerlolaan 5
7522NB Enschede
The Netherlands

Email: p.j.m.havinga@utwente.nl
Website: www.wibrate.eu

WiBRATE's key innovation lies in the development of a self-powered, vibration monitoring and control platform. Unlike existing vibration monitoring devices available in the market that operate as individual entities, WiBRATE's unique approach is based on individual intelligent sensor-actuator nodes that communicate wirelessly to collaboratively predict impending failures, perform fault diagnosis or provide real-time feedback. This feedback can then be used to further minimise vibration levels using distributed and autonomous micro-actuators that are capable of carrying our robust, distributed control. The use of robust wireless communication strategies ensures that the system is highly flexible and allows for a new class of monitoring and control applications that are not possible using traditional wired systems. Apart from measuring and controlling vibration levels, WiBRATE's platform also harnesses the vibration itself thus resulting in a system that is both maintenance free and environment friendly.

★ booth 13

Wirtschaftsförderung Sachsen GmbH (WFS)

Contact: Christiane Wagner

Wirtschaftsförderung Sachsen GmbH
Bertolt-Brecht-Allee 22
01309 Dresden
Germany

Phone: +49-351-2138 134
Fax: +49-351-2138 399

Email: christiane.wagner@wfs.saxony.de
Website: www.wfs.saxony.de

We build bridges: Between Saxon companies and cooperation partners from abroad, between potential investors and Saxony´s regions and communes, between research and practice, between business ideas and economic success.

★ booth 13

X-FAB Group

Contact: Anja Noack

X-FAB Semiconductor Foundries AG
Haarbergstrasse 67
99097 Erfurt
Germany

Phone: +49 361 427 6162
Fax: +49 361 427 6161

Email: anja.noack@xfab.com
Website: www.xfab.com

X-FAB is the leading analog/mixed-signal foundry group manufacturing silicon wafers for analog-digital integrated circuits (mixed-signal ICs). As a specialty foundry for so-called "More than Moore" technologies, X-FAB creates a clear alternative to typical foundry services by combining solid, specialized expertise in advanced analog and mixed-signal process technologies with excellent service, a high level of responsiveness and first-class technical support. It manufactures wafers for automotive, industrial, consumer, medical, and other applications on advanced modular CMOS and BiCMOS processes with technologies ranging from 1.0 to 0.13 µm, and special BCD, SOI and MEMS long-lifetime processes. These technologies are not intended for digital applications with the smallest possible structure sizes, but rather are targeted for analog applications that can be integrated with additional functions such as high voltage, non-volatile memory or sensors. With its five manufacturing sites in Germany, the U.S. and Malaysia, the company's combined manufacturing capacity is approximately 62,000 8-inch equivalent wafer starts per month. X-FAB customers benefit from high-performance technologies, excellent technical design and prototyping services; and fast, easy and flexible foundry access worldwide. The company has approximately 2,400 employees worldwide. For more information, please visit www.xfab.com

PRODUCT FINDER

Services:
Prototyping
Foundry & Manufacturing

Semiconductor IP:
Analogue & Mixed Signal IP
Memory IP
Physical Libraries
Synthesizable Libraries

Application-Specific IP:
Analogue & Mixed Signal IP

★ booth 13 & TP 4

Zentrum Mikroelektronik Dresden AG

Contact: Andreas Brüning

Zentrum Mikroelektronik Dresden AG
Grenzstraße 28
01109 Dresden
Germany

Phone: +49 351 8822-306
Fax: +49 351 8822-337

Email: andreas.bruening@zmdi.com
Website: www.zmdi.com

Zentrum Mikroelektronik Dresden AG (ZMDI) is a global, innovation-driven, customer-focused enterprise delivering high-performance analog and mixed signal semiconductor solutions for over 50 years. The ZMDI difference is that we partner fully throughout the development of innovative analog and digital power and sensing technologies, expertly exploring your unique system requirements, solving design challenges and then collaboratively designing and delivering subsystem and/or architectural solutions. ZMDI's solutions enable our customers to create the most energy-efficient products for sensors, power management, and lighting.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
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Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test

Embedded Software Development:
Compilers
Real Time Operating Systems
Debuggers
Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms
Development Boards

Conference & Exhibition

March 09–13, 2015 • Grenoble, France

CALL FOR PAPERS

Scope of the Event

The 18th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of- the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical and Healthcare Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems
- Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles
- Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by **Sunday, September 14, 2014** via: www.date-conference.com
Papers can be submitted either for standard oral presentation or for interactive presentation.
The Programme Committee also encourages proposal submissions for Special Sessions, Tutorials and Friday Workshops as well as submissions for the Special Days on "Designing Electronics for the Internet of Things" and "Designing Electronics for Medical Applications"

Event Secretariat

c/o K.I.T. Group GmbH Dresden
Muenzgasse 2
01067 Dresden, Germany

Phone: +49 351 4967 541
Fax: +49 351 4956 116
Email: conference-management@date-conference.com

Chairs

General Chair: Wolfgang Nebel
OFFIS, Oldenburg, Germany
wolfgang.nebel@offis.de

Programme Chair: David Atienza
EPFL, Lausanne, Switzerland
david.atienza@epfl.ch