DATE '14

ICC, Dresden, Germany
Event 24–28 March  Exhibition 25–27 March

Design, Automation & Test in Europe

The European System Design Show
From Systems-on-Chip to Embedded Computing

www.date-conference.com
Welcome to DATE 14

On behalf of the whole Organising Committee, we thank you very much for visiting DATE 2014 and are happy to welcoming you in the beautiful city of Dresden, Germany!

This event guide provides all relevant information concerning the DATE 2014 accompanying exhibition, a programme outline as well as venue and floor plans for your orientation.

All participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

The Exhibition Visit is free of charge.

Exhibition visitors have free access to the exhibition area, the opening keynote lectures and the Exhibition Theatre Programme.

OPENING PLENARY KEYNOTES:
Tuesday, March 25, 2014, 0830 – 1030, Grosser Saal, Saal Level

Exhibition Opening Times:
Tuesday, March 25 1000 – 1830*
Wednesday, March 26 1000 – 1800
Thursday, March 27 1000 – 1700

*Exhibition Reception from 1830 to 1930 in the exhibition area on the Terrace Level
The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in the editorial pages. Listed below are the media houses and publications who generously agree to media partnership with DATE, and whose publications can be found on-site near the Press Lounge on the Conference Level.

**3D InCites**
First launched in 2009, 3D InCites is a community platform that is the only online resource devoted exclusively to 2.5D and 3D integration technologies. 3D InCites is a resource for Industry news, technology implementation, market analysis and opinion. As such, it provides a place to learn, share, engage and collaborate with fellow 2.5D and 3D enthusiasts. For 3D IC integration to happen requires open collaboration across the supply chain. Therefore, 3D InCites strives to inform key decision makers about progress in technology development, design, standards, and infrastructure in order to realize commercial production of 2.5D and 3D technologies. 3D InCites has grown to a registered membership of over 1300 with many additional visitors who stop by just to keep up with what’s happening in the world of 3D.

www.3DInCites.com

**EDA Confidential**
EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes “Recipes”, Freddy Santamaria’s “Gourmet Corner”, as well as “Voices” of other contributing authors, “Off the Record” op-ed pieces, and “Conference” coverage.

www.aycinena.com

**Chip Design Magazine**
Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today’s complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won’t want to miss. And, be sure to visit www.eecatalog.com for valuable information about all of Extension Media’s outstanding technology resources.

www.chipdesignmag.com

**Elektronik i Norden**
Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed copies proves we are the major electronics paper in this area. We publish news, comments and in-depth technical articles.

www.elinor.se

**Engineering & Technology Magazine – Published by The IET**
Engineering & Technology is packed with articles on the latest technology covering the areas of communications, control, consumer technology, electronics, IT, manufacturing & power engineering. It is Europe’s largest circulation engineering magazine, published monthly & offers a global circulation of over 140,000 copies to more than 100 countries & a high pass-on readership.
Each member of the Institution of Engineering & Technology (IET) receives a copy as part of their membership package. Readers include design & development engineers, system designers & integrators, solutions providers & installers, engineering distributors, consultants, planners, facilities managers & end-users. With its HQ in London & regional offices in Europe, North America & Asia-Pacific, the Institution of Engineering & Technology provides a global knowledge network to facilitate the exchange of ideas & promote the positive role of technology around the World. The Institution of Electrical Engineers, dating from 1889, became the Institution of Engineering & Technology in 2006. It now organises more than 120 conferences & other events each year whilst providing professional advice & briefings to industry, education & governments.

www.eandtMagazine.com

**MICRONews**
MICRONews, powered by Yole Développement
Founded in 1998, Yole Développement has grown to become a group of companies providing marketing, technology and strategy consulting, media in addition to corporate finance services. With a strong focus on emerging applications using silicon and/or micro manufacturing, Yole Développement group has expanded to include more than 50 associates worldwide covering MEMS, Compound Semiconductors, LED, Image Sensors, Optoelectronics, Microfluidics & Medical, Photovoltaics, Advanced Packaging, Manufacturing, ok Nanomaterials and Power Electronics. The group supports industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

**MEDIA & EVENTS ACTIVITY**
- i-Micronews.com, online disruptive technologies website
- Weekly WebTalk
- @Micronews, weekly e-newsletter
- Technology Magazines dedicated to MEMS, Advanced Packaging, LED and Power Electronics
- Communication & webcasts services
- Events: Yole Seminars, Market Briefings
conference March 9 – 13, 2015
Exhibition March 10 – 12, 2015
Grenoble, France
**THURSDAY 27 MARCH**

**0730** REGISTRATION, Terrace Level, AND SPEAKER’S BREAKFAST, Saal 2

**0830-1000** Special Day A-Track

**1000-1030** Exhibition and Coffee Break

**1030-1100** Special Day B-Track

**1100-1130** Lunch Break

**1230-1400** Special Day C-Track

**1400-1600** Exhibition and Coffee Break

**1630-1700** Coffee Break

**1700-1830** Special Day D-Track

**1830-2000** Date Party co-sponsored by the City of Dresden

**WEDNESDAY 26 MARCH**

**0730** REGISTRATION, Terrace Level, AND SPEAKER’S BREAKFAST, Saal 2

**0830-1000** Special Day A-Track

**1000-1030** Exhibition and Coffee Break

**1100-1130** Lunch Break

**1230-1400** Special Day B-Track

**1400-1530** Exhibition and Coffee Break

**1530-1630** Coffee Break

**1630-1830** Special Day D-Track

**1830-2000** Date Party co-sponsored by the City of Dresden
INTERACTIVE PRESENTATIONS

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held on the Conference Level of the congress centre in 30-minute time slots on the following days:

- **IP Session 1, Tuesday, March 25, 2014**
  - Conference Level, Foyer
  - 1600 – 1630

- **IP Session 2, Wednesday, March 26, 2014**
  - Conference Level, Foyer
  - 1000 – 1030

- **IP Session 3, Wednesday, March 26, 2014**
  - Conference Level, Foyer
  - 1600 – 1630

- **IP Session 4, Thursday, March 27, 2014**
  - Conference Level, Foyer
  - 1000 – 1030

- **IP Session 5, Thursday, March 27, 2014**
  - Conference Level, Foyer
  - 1530 – 1600

After the last IP Session of each day, the “Best IP of the Day” will be awarded.
Application demands in our embedded world are growing dramatically. Consumer expectations and the industry’s forward-looking technology roadmaps paint a picture of a connected world full of intelligent devices once thought to have fixed functionalities. Researchers exploring next generation wireless systems, Internet of Things (IoT), and even machine-to-machine (M2M) communications face many challenges in making this vision a reality. Where once a single, isolated design flow addressed the discrete application, heterogeneous multi-processing architectures must be considered and embraced along with the connections to other devices and systems, and real-world sensor data. As the systems grow in complexity, new design approaches must also be developed and employed to expedite the research, design, and development cycle. David Fuller will outline challenges system designers face in developing cyber-physical systems and explore a graphical system design approach that includes hardware abstraction and comprehends a heterogeneous multiprocessor environment while embracing different models of computation. Through this new approach, system designers can shorten design cycles and the time to prototype ultimately accelerating deployment.

Microelectronics is the dominant industrial technology of today. Its rate of innovation, spelled out by Moore’s Law, is exceptional by any commercial metric, especially, as it has been on this trajectory for almost 40 years. It is not surprising, that other industrial sectors are taking advantage of the innovation engine of the semiconductor for its own product innovation: Cars are safer and more economic, medical diagnostics are performing to a significantly higher level, and energy efficiency from the generation to the consumer. We need to rethink the connected world around us to truly assess the new processing paradigms for the car itself. On the other hand the vehicle itself significantly expands its sensor and processing capabilities by the use of radar, video, ultrasound sensors and usage of state of the art CPU and GPU processor architectures. In our talk we will address both developments and outline foreseen future applications as future driving assistant and infotainment systems as well as highly automated driving. We will discuss major requirements for the future electrical architectures and implications for future automotive chips.
Executive Sessions

**Organiser:** Yervant Zorian, Synopsys, US

DATE 2014 will again feature an Executive Track of presentations by leading companies executives representing a range of semiconductor manufacturers, EDA vendors, fabless houses and IP providers. This one-day program will be held on Tuesday 26 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks.

### EXECUTIVE SESSION: How to Handle Today’s Design Complexity

**Organiser:** Yervant Zorian, Synopsys, US  
**Executives:** Sanjive Agarwala, Texas Instruments, US  
Paul Lo, Synopsys, US  
Rainer Kress, Infineon, DE  
Leon Strock, IBM, US  
Sanjiv Taneja, Cadence, US

The widening gap between growing SOC complexity and designer productivity limits traditional chip design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of complex SOC design. Executives in this session will discuss the impact of complexity and the new opportunities it may bring in designing today’s SOC.

### EXECUTIVE SESSION: Advanced Technology Challenges & Opportunities

**Organiser:** Yervant Zorian, Synopsys, US  
**Executives:** Giorgio Cesana, STMicroelectronics, FR  
Joachim Kunkel, Synopsys, US  
Rudy Lauwereins, IMEC, BE  
Maria Merced, TSMC  
Gerd Töpke, GLOBALFOUNDRIES, DE

The continuous technology scaling and their new applications are dramatically impacting the semiconductor industry. This may also significantly affect the dependency between eco-system players necessitating smooth interdependency between them. The executives in this session will discuss upcoming innovations in the semiconductor industry and their impact on the solutions offered by the eco system players.

### EXECUTIVE SESSION: Addressing Challenges of Reliable Chips

**Organiser:** Yervant Zorian, Synopsys, US  
**Executive:** Dan Alexandrescu, iROC Technologies, FR  
Robert Altkén, ARM, US  
Robert Hum, Mentor Graphics, US  
Ronald Martino, Freescale, US

While today’s SOCs systematically use semiconductor production quality assurance and optimization solutions, meeting end-product requirements for reliability and availability augments the need to prepare the SOC design in advance to address such requirements. The speakers in this executive session will address the current trends and challenges in the semiconductor reliability and discuss the level of readiness needed in a chip to meet today’s SOC requirements.

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**Special Day: System-Level Design**

**Organisers and Co-Chairs:** Jürgen Teich, University of Erlangen-Nuremberg, DE  
Johannes Stahl, Synopsys, US

The special day System-Level Design will reflect current industrial practices as well as present recent advances in this research area. A particular emphasis will be on ultra-low power design and modeling at multiple abstraction levels, virtual platforms for software development and architecture design of MPSoCs. We will also take a look at high-level synthesis from different input languages as well as software code generation techniques. Important topics also include multicore enablement for safety-critical and real-time embedded systems as well as accelerator-rich design for the fight against dark silicon.

### HOT TOPIC: Predictable Multi-Core Computing

**Organiser:** Jürgen Teich, University of Erlangen-Nuremberg, DE  
**Chair:** Petru Eles, Linkoping University, SE  
**Co-Chair:** Jürgen Teich, University of Erlangen-Nuremberg, DE

The requirement of high performance computing at low power can be met by the parallel execution of an application on a possibly large number of programmable cores. However, the lack of accurate timing properties may prevent parallel execution from being applicable to time-critical applications. This session treats this important problem of time predictability of applications on multi-core platforms by presenting results of the impact of resource sharing on performance, an architecture that has been designed to meet predictability requirements as well as new results on scheduling mixed critical applications on multi-core platforms.

### HOT TOPIC: The fight against Dark Silicon

**Organiser:** Jörg Henkel, Karlsruhe Institute of Technology, DE  
**Chair:** Jörg Henkel, Karlsruhe Institute of Technology, DE  
**Co-Chair:** Jürgen Teich, University of Erlangen-Nuremberg, DE

Dark Silicon is predicted to dominate the chip footage of upcoming-micro-systems within a decade since Dennard Scaling fails mainly due to the voltage-scaling problem that results in higher power densities. It would deem upcoming technologies nodes inefficient since a majority of cores would lie fallow. Significant research efforts have started within the last couple of years to investigate and mitigate Dark Silicon effects to ensure an effective use of available chip footage.

This special session gives a snapshot of current research activities of this grand challenge. In particular, the three talks present the newest trends and developments starting with the problem of Dennard Scaling and how it mandates new design constraints followed by the problem of power delivery and cooling, and concluding with the newest directions in efficient resource management for many-core systems.

### The connected car and its implication to the automotive chip roadmap

**Organiser:** Johannes Stahl, Synopsys, US  
**Chair:** Iris Stroh, Robert Bosch GmbH, DE

The connected car and its implication to the automotive chip roadmap is the topic of this special session. It will be divided into three parts: hardware, software, and verification.

### PANEL: HW/SW Co-Development – The Industrial Workflow

**Organiser:** Johannes Stahl, Synopsys, US  
**Chair:** Iris Stroh, Robert Bosch GmbH, DE

This panel brings together the entire supply chain for the use of virtual prototyping starting with the end users at an automotive Tier1, a semiconductor supplier, IP providers and the virtual prototyping and software development tool providers. The panelists will discuss what are the benefits and challenges of accelerating software development using virtual prototyping for deployment in industrial projects.

### System Simulation and Virtual Prototyping

**Organiser:** Johannes Stahl, Synopsys, US  
**Chair:** Johannes Stahl, Synopsys, US

In this session we will review several practical applications of virtual prototyping for architecture design work and software development across different markets such as mobile, industrial and automotive. The authors will share their practical experiences in using the virtual prototyping methodology and current commercial tools.
**Special Day: Advancing Electronics beyond CMOS**

Organisers and Co-Chairs: Ian O’Connor, Lyon Institute of Nanotechnology, FR
Thomas Mikolajick, NamLab gGmbH, DE

As the issues associated with CMOS scaling become harder and more costly to solve, the special day Advancing Electronics beyond CMOS will cover the latest trends towards alternative memory and processing technologies for computing and data acquisition and transport. Important topics include nanoscale switching devices and computing nanofabrics, trends in memory technologies in hybrid 3D integration, flexible and organic electronics, new state variable vectors (spintronic, photonic) and interfaces to the natural world (sensor networks, data analysis, displays, MEMS).

**HOT TOPIC: CMOS scaling - from evolutionary to revolutionary computing**

Organisers: Thomas Mikolajick, NamLab gGmbH, DE, Ian O’Connor, Lyon Institute of Nanotechnology, FR
Co-Chair: Thomas Mikolajick, NamLab gGmbH, DE

Transistors as switches have now scaled down to a point where the classical bulk structure is no longer tenable and it is necessary to change the nature of the channel structure. In this session, the three principal contenders for following on from conventional devices will be examined. The first paper looks at the use of III-V nanowires, with expected benefits in terms of speed and energy, as well as integration challenges. The second paper looks at how the use of switches with controllable polarity, such as in silicon nanowire devices, can improve the energy efficiency of systems on chip. The devices themselves are explored in detail in the third paper, with the concept of fine-grain reconfigurability at the forefront. The fourth and final paper gives a reality check on carbon electronics and the most promising devices in this class.

**State-of-the-art in verification: European tertulia IC design – enabling AMR Structured System integration - the Bridge between more than Moore and more Moore**

Organisers: Gooran Jerke, Robert Bosch GmbH, DE
Oliver Bringmann, University of Tuebingen, DE
Co-Chair: Gooran Jerke, Robert Bosch GmbH, DE

In order to benefit from modern automotive semiconductor technologies, application robustness must now be considered as a design target. This includes the subsequent consideration of environmental stress conditions and functional loads, which are formalized in so-called “mission profiles”. We introduce the motivation to use mission profiles from an OEM and Tier perspective. Additionally, we introduce the mission profile aware flow and present several application scenarios.

**EXHIBITION THEATRE**

**Special Session**

**Special Session**

**State-of-the-art in Verification: European Tertulia IC Design – Enabling AMS Structured Verification / Verification in FPGA & IP design flows**

Details to be announced.

**EXHIBITION THEATRE**

**Special Session**

**System Integration - The Bridge between More than Moore and More Moore**

Organiser: Manfred Dietrich, Fraunhofer IIS/EAS Dresden, DE
Chair:  
Kai Hahn, University Siegen, DE
Co-Chair:  
Kai Hahn, University Siegen, DE

System Integration using 3D technology is a very promising way to cope with current and future requirements for electronic systems. Since the pure shrinking of devices (known as “More Moore”) will come to an end due to physical and economic restrictions, the integration of systems (e.g. by stacking dies or by adding sensor functions) shows a way to maintain the growth in complexity as well as in diversity which is necessary for future applications. This so-called “More than Moore” approach complements the conventional SoC product engineering. This session gives insights in System Integration design challenges from different perspectives, ranging from design technology over MEMS product engineering and 3D interconnect to automotive cyber physical systems.
EXHIBITION THEATRE SESSION
First Time Right in Analog Design Enabling New Business Cases
Wednesday, March 26, 2014, 1100 – 1230
Details to be announced.

EXHIBITION THEATRE SESSION
FD-SOI – the Enabling European Technology for Energy Efficient Solutions – Creating a Solution Hive & Design Hub as Eco-System for Future Success
Wednesday, March 26, 2014, 1430 – 1600
Details to be announced.

SPECIAL SESSION
Hot Topic: Beyond CMOS Ultra-low-power Computing
Wednesday, March 26, 2014, 1700 – 1830
Organiser: Saibal Mukhopadhyay, Georgia Institute of Technology, US
Chair: Arijit Raychowdhury, Georgia Institute of Technology, US
Co-Chair: Saibal Mukhopadhyay, Georgia Institute of Technology, US
With conventional CMOS scaling becoming increasingly challenging, the designers wonder what opportunities and challenges exist beyond-CMOS for both Boolean and non-Boolean computing. This session will discuss three very different and promising emerging technologies – Tunneling Field-Effect Transistor, Spintrons, and nano-electro-mechanical switches (NEMS) – for low-power electronics. The talks will discuss the need for innovating and evaluating new circuit and system design methodologies as new device technologies emerge.

SPECIAL SESSION
Embedded Tutorial: Memcomputing: the Cape of Good Hope
Thursday, March 27, 0830 – 1000
Organisers: Yiyu Shi, Missouri University of Science & Technology, US
Hsing-Ming Chen, National Chiao Tung University, TW
Chair: Tsung-Yi Ho, CSIE, NCKU, TW
Co-Chair: Hsing-Ming Chen, National Chiao Tung University, TW
Energy efficiency has emerged as a major barrier to performance scalability for modern processors. On the other hand, significant breakthroughs have been achieved in memory technologies recently. As such, the fascinating idea of memcomputing (i.e., use memory for computation purposes) has drawn wide attention from both academia and industry as an effective remedy. Compared with conventional logic computing, memory array provides large set of parallel resources with high bandwidth, which can configured to perform computing in spatial/temporal manner leading to dramatic reduction in processor-memory traffic. Moreover, memory computing brings the computing engine close to the data, thus drastically minimizing the von Neumann bottleneck. Finally, it exploits the advances in memory technologies and integration approaches (e.g., 3D integration) to achieve better technology scalability. This special session offers a broad-spectrum retreat (devices, processes and systems) on this hot topic to the general CAD community, hoping to inspire more contributions from the design automation perspective.

EXHIBITION THEATRE PANEL
EDA+3D+MEMS Innovation Agenda 2020 Fueling the Innovation Chain of Electronics
Thursday, March 27, 2014, 1100 – 1230
Organiser: Jürgen Haase, edacentrum, DE
Moderator: Ahmed Jerraya, CEA-LETI, FR
Panelists: Gabriel Klietzer, X-FAB, DE
Brandon Wang, Cadence, US
Brent Gregory, Synopsys, US
Horst Symanzik, Bosch-Sensortec GmbH, DE
Gerd Teepe, GLOBALFOUNDRIES, DE

EXHIBITION THEATRE PANEL
Beyond-CMOS for both Boolean and non-Boolean computing, the designers wonder what opportunities and challenges exist beyond-CMOS. This session will discuss three very different and promising emerging technologies – Tunneling Field-Effect Transistor, Spintrons, and nano-electro-mechanical switches (NEMS) – for low-power electronics. The talks will discuss the need for innovating and evaluating new circuit and system design methodologies as new device technologies emerge.

SPECIAL SESSION
Embedded Tutorial: GPGPUs: how to combine high computational power with high reliability
Thursday, March 27, 1400 – 1530
Organiser: Matteo Sonza Reorda, Politecnico di Torino, IT
Chair: Dimitris Gizopoulos, University of Athens, GR
Co-Chair: Rob Aitken, ARM, US
The embedded tutorial aims at providing with an updated view on what GPGPUs can provide not only in terms of performance and power, but also in terms of reliability, and how the latter can be evaluated and possibly improved.

SPECIAL SESSION
Panel: Future SoC Verification methodology: UVM evolution or revolution?
Thursday, March 27, 1600 – 1730
Organiser: Alex Goryachev, IBM Research, Haifa, IL
Chair: Rolf Drechsler, University of Bremen/DPKI, DE
It is a recent trend that SoCs are becoming more similar to servers. Many SoCs today are no longer tied to a single application and look more like general purpose PCs and high-end servers. Smartphones are the most notable example of this, but we are also seeing this with TV chips, in-car controllers, network routers, and more. This trend is occurring in parallel to the constantly growing complexity of SoCs, which support diverse IO interfaces and devices, and have complex architectures including multiple heterogeneous cores, multi-level caches, and multiple IO bridges.

In this panel leading experts from industry (both users and vendors) and academia will discuss the future of SoC verification methodology. Is the gap in today’s SoC verification methodology significant? Is it growing? Or perhaps it does not exist? What is the right way to close the gap, if one exists? Is it sufficient to extend UVM capabilities (e.g., SystemC, TLM) or are dedicated tools and methodology needed? Are formal methods ready to play a significant role in SoC-level verification? In general, we would like to determine the importance of system-level verification and its unique needs—whether generators, checking, coverage, or teams.
The DATE 2014 Programme Committee has again put emphasis on providing plenty of opportunities for conference delegates to visit the exhibition, get in touch with colleagues and attend the sessions in the exhibition theatre.

A number of specialist interest groups will be holding their meetings at DATE 2014. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage www.date-conference.com.

### Coffee & Lunch Breaks

The exhibition area on the Terrace Level of the International Congress Centre also hosts the coffee and lunch break area. During the below-mentioned times, coffee and tea will be served during the coffee breaks as well as light snacks during the lunch breaks (for full conference delegates only). Furthermore, there is a cash bar on the Terrace Level for visitors and exhibitors.

#### Tuesday, March 25, 2014

- **Coffee Break:** 1030 – 1130
- **Lunch Break:** 1200 – 1300
- **Coffee Break:** 1600 – 1700

#### Wednesday, March 26, 2014

- **Coffee Break:** 1000 – 1100
- **Lunch Break:** 1230 – 1400
- **Coffee Break:** 1600 – 1700

#### Thursday, March 27, 2014

- **Coffee Break:** 1000 – 1100
- **Lunch Break:** 1230 – 1400
- **Coffee Break:** 1530 – 1600

### Exhibition Reception, Tuesday, March 25, 2014

The Exhibition Reception will take place on Tuesday, March 25, 2014, from 1830 – 1930 in the exhibition area (Terrace Level), where free drinks and snacks for all conference delegates and exhibition visitors will be offered.

### DATE Party, Wednesday, March 26, 2014

The DATE Party is again scheduled on the second conference day, Wednesday, March 26, 2014, starting from 1930. This year, it will take place in one of Dresden’s most exciting and modern buildings, the “Gläserne Manufaktur” of the car manufacturer Volkswagen AG (www.glaesernemanufaktur.de/en/). The party will feature a flying buffet style dinner with various catering points and accompanying drinks. Light background music and the possibility of guided visits through the extraordinary premises will round off the evening. It provides a perfect opportunity to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities.

Please kindly note that it is no seated dinner.

All delegates, exhibitors and their guests are encouraged to attend the party. Please be aware that entrance is only possible with a party ticket. Each full conference registration includes a ticket for the DATE Party. Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets). Ticket price for the full Evening Social Programme: 75 € per person.

DATE Party Shuttle: There will be an organised shuttle by tram to the DATE Party venue and back for all conference delegates having a Party Ticket.

Meeting point: 1845 in front of the main entrance of the International Congress Center Dresden (ICCD). The trams then start at 1900 from the tram station “Kongresszentrum”.

The DATE Party is co-sponsored by the City of Dresden.

### Interactive Presentations

Interactive presentations will take place from Tuesday, March 25, 2014 until Thursday, March 27, 2014 on the Conference Level, Foyer. → See page 8
### Conference Level

- Seminar rooms downstairs
- Conference rooms & Press Lounge upstairs
- Exhibition Theatre
- A/V Office (Konferenz 7+8)
- IP Sessions
- Technology Plaza
- University Booth
- Terrace Level

### Terrace Level

- Catering
- Press Lounge
- IP Sessions
- University Booth
- Conference Theatre
- A/V Office
- Technology Plaza
- Educational Level

### Company Booth

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First launched in 2009, 3D InCites is a community platform that is the only online resource devoted exclusively to 2.5D and 3D integration technologies. 3D InCites is a resource for industry news, technology innovation, market analysis and opinion. As such, it provides a place to learn, share, engage and collaborate innovation, market analysis and opinion. As such, it provides a place to learn, share, engage and collaborate.

Product Finder
Embedded Software Development: Compilers

Blue Pearl Software
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Email: murielle@bluepearlsoftware.com
Website: www.bluepearlsoftware.com

Blue Pearl Software automates IP and FPGA verification before debug. From an HDL description, designers run FPGA-centric structural checks for Xilinx and Altera. Blue Pearl’s unique clock domain crossing analysis includes checks through CORE Generator™ and MegaCore™ functions using Blue Pearl’s Grey Cell™ methodology. Blue Pearl automatically generates SDC timing constraints for downstream tools from Altera, Cadence, Mentor, Synopsys and Xilinx.

Network Thinking – Microelectronics in Dresden - Competencies: Research & Development, IC Design, Photomasks, Chip Manufacturing, Packaging, Equipment, Software - The Economic Development Office of the City of Dresden is your contact and partner as entrepreneur or investor. Our service ensures that your investment in Dresden can be realised without delay.
Welcome to Dresden!
information and communication technology and must be
guaranteed without penalizing or slowing down the
characteristics of the final products.
CLERECO research project (http://www.clereco.eu), a
FP7 Collaboration Project involving Politecnico di
Torino (Italy), National and Kapodistriou University of
Athens (Greece), LIUMM (France), Intel Corporation
Iberia S.A. (Spain), Thales SA (France), Yogitech spa
(Italy) and ABB AS (Norway), recognizes early accurate
reliability evaluation as one of the most important and
challenging tasks toward this goal. Being able to
precisely and early evaluate the reliability of a system
means being able to carefully plan for specific
countermeasures rather than resorting to worst-case
approaches.
The proposed CLERECO framework for efficient reliability
evaluation and therefore effective exploitation of
reliability oriented design approaches starting from
early phases of the design process will enable circuit
integration to continue at exponential rates and enable
the design and manufacture of future systems for the
computing continuum at a minimum cost contrary to
existing worst-case-design solutions for reliability. The
applications of such chips will play a major role in several
fields ranging from avionics, automobile, smartphones,
mobile systems, and future servers utilized in the
settings of several types of HPC systems.

**PRODUCT FINDER**

**ASIC and SOC Design:**
MEMS Design

**Services:**
Prototyping
Foundry & Manufacturing

**Codasip**

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**Fax:** +420541 211 479

**Email:** info@codasip.com
**Website:** www.codasip.com

Codasip delivers leading-edge IP and EDA tools to enable
adoption of Application Specific Instruction Set
Processors (ASIP’s). ASIP’s utilize dedicated instructions
to accelerate software and are at the heart of applications
such as software defined radio and computer vision - delivering very high performance with
low power. Codasip’s unique technology makes ASIP
design as simple and easy as standard embedded
processor cores.
The Codasip® Framework provides an all-in-one
development environment for ASIP design, verification,
programming and debug. Codasip® Framework
shortens development time substantially when
compared to competing ASIP design platforms
automating many of the otherwise time consuming
and error prone tasks, while at the same time delivering
higher performance ASIPs. Leveraging open technologies
and standards throughout ensures integration with any
design and programming environment - these
technologies cover synthesizable RTL, UVM and
tLM-based verification and UVM-based programming tool-
chains for the target processor. A wide variety of
processor verification models are automatically
generated supporting virtual prototyping, system
simulation and detailed debug. The Codasip® Framework
also includes support for multi-processor profiling,
verification, programming, and debug.
Codix IP Cores provide a proven extensible processing
platform that can be adapted to a customer’s needs.
These cores are an ideal starting point for customers new
to ASIC design allowing for rapid integration while still
delivering a great deal of flexibility. A variety of Codix
Cores are available covering DSP, RISC, and VLIW

**PRODUCT FINDER**

**ASIC and SOC Design:**
Verification
System-Level Design:
Hardware/Software Co-Design

**Services:**
Prototyping
Embedded Software Development:
Compilers
Debuggers

**Semiconductor IP:**

**Cores**

**Processors**

**System Platforms**

**Application-Specific IP:**

Digital Signal Processing
Multimedia Graphics

**CONTEX**

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Germany

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**Website:** contrex.offis.de

CONTEX (Design of embedded mixed-criticality CONTRol
systems under consideration of EXtra-functional
properties) will enable energy-efficient and cost aware
design through analysis and optimization of real-time,
power, temperature and reliability with regard to
application demands at different criticality levels.

**Concept Engineering GmbH**

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Germany

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**Email:** info@concept.de
**Website:** www.concept.de

Concept Engineering develops and markets innovative
visualization and debugging technology for commercial
EDA vendors, in-house CAD tool developers, FPGA and IC
designers.
Nview WidgetsTM – a family of schematic generation and
visualization engines (Tcl/Tk, MFC, Qt, Java, Perl/
Tk, wxWidgets) that can be easily integrated into EDA
tools.
PRODUCT FINDER
ASIC and SOC Design:
Analogue and Mixed-Signal Design
RF Design
Test:
Test Automation (ATPG, BIST)
Mixed-Signal Test
Services:
Design Consultancy
Prototyping
Semicorndonor IP:
Analogue & Mixed Signal IP
CPUs & Controllers
Encryption IP
Application-Specific IP:
Analogue & Mixed Signal IP

CREATIVE CHIPS GmbH

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Website: www.creativechips.com

CREATIVE CHIPS offers the complete service of a Fabless Semiconductor Vendor. From specification, complete IC development, sample production, qualification for series production and the documentation up to mass production and volume deliveries of ASICs and ASSPs, tested in our in-house test department. The company’s headquarter is located in Bingen /Rhein in Germany with design center in Dresden and an Asia sales office located in Israel. As an automotive supplier in Germany with design center in Dresden and an Asia sales office located in Israel, as an automotive supplier in Germany, the company is certified according to the quality standard ISO/TS 16949. CREATIVE CHIPS offers the following services:

- Turn-key circuit design, sample production, evaluation and qualification for mass production of a custom specific mixed-signal ASIC or pure analog but also complex digital integrated circuits – ASSICS and standard ICs
- Test and delivery of bulk production IC volumes to our customers regarding flexible and defined quality and logistic demands with backend services as tape & reel, dry packing or long time storage of parts
- complete supply chain management for IC production
- FPGA / ASIC conversion
ASICs from CREATIVE CHIPS are used in various applications like:

- Automotive electronics (e.g. robust sensor and control circuits for car environment)
- Automation industry (e.g. optical transimpedance amplifiers with integrated sensors, bus interface ICs, smart power supply circuits)
- Multimedia (e.g. broadband optical data transmission systems, RF data transmission in 433/868 MHz band, buck-boost converters)
- Consumer electronics and white goods (e.g. motor drivers, battery charging circuits).

PRODUCT FINDER
ASIC and SOC Design:
Analogue and Mixed-Signal Design
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Mixed-Signal Test
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Design Consultancy
Prototyping
Semicorndonor IP:
Analogue & Mixed Signal IP
CPUs & Controllers
Encryption IP
Application-Specific IP:
Analogue & Mixed Signal IP

Dream Chip Technologies GmbH

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Website: www.dreamchip.de

Dream Chip Technologies (DCT) - located in Garbsen near Hanover - is an independent fabless microelectronic engineering company with a long history in development of embedded Software and PCBs and in FPGAs and ASICs for highly complex System-on-Chips (SoCs). Next to pure development, DCT offers also the delivery of the developed products. Founded as SICAN more than 20 years ago and belonging as SCI-WORX to Infineon for several years, DCT comes today with outstanding know-how in the development of challenging microelectronics especially for video and imaging applications. DCT focuses on microelectronic manufacturers for the industrial and the consumer market who want to offer market-driven products in an optimum time frame, without permanently being able to provide the required capacity for development. Our customers are mainly product makers in the automotive, industrial and medical area, for professional video applications and for consumer electronics.

Next to the design service for customers, DCT develops and delivers also own technologies and products. As well as technologies for 2D and 3D image processing pipelines and for video compression functionality this also includes a Super Slow Motion module which extends the operational area of simple industrial cameras without integrated image processing capability and which is used in professional slow motion systems. Founded at the beginning of 2010, DCT today employs 35 development engineers; the yearly turnover is around EUR 4 million.

PRODUCT FINDER
ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Thermal, Signal) Verification
System-Level Design:
Enhancement & Emulation
Hardware/Software Co-Design
PCB & McM Design
Test:
Design for Test
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
System Test
Services:
Design Consultancy
Prototyping
Training
Embedded Software Development:
Real Time Operating Systems
Software/Modelling
Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Semicorndonor IP:
Configurable Logic Embed
Embedded FPGA
Embedded Software IP
Encrytion IP
On-Chip Bus Interconnect
On-Chip Debug
Processor Platforms
Synthesizable Libraries
Application-Specific IP:
Data Communication
Digital Signal Processing
Multimedia Graphics

DREAMS

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Website: www.dreams-project.eu

DREAMS (Distributed Real-time Architecture for Mixed criticality Systems) will develop a cross-domain architecture and design tools for networked complex systems where application subsystems of different criticality, executing on networked multi-core chips, are supported.

EDA Confidential

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EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation Industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes “Recipes”, Freddy Santamaría’s “Gourmet Corner”, as well as “Voices” of other contributing authors, “Off the Record” op-ed pieces, and “Conference” coverage.

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CREATIVE CHIPS GmbH

booth TP 2
Dream Chip Technologies GmbH

booth EP 1
DREAMS

booth K 3
EDA Confidential
EDA Solutions LTD
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For over 10 years EDA Solutions have provided cost effective and highly productive IC Design software and manufacturing services to European industry. Visit us at our stand to find out more about the digital synthesis tools from Incentia, the analog/mixed signal design, layout and verification tools from Tanner EDA and the tools from Incentia, the analog/mixed signal design, layout and verification tools from Tanner EDA and the tools from Incentia.

Elektronik i Norden
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Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed.

ECS draws its strength from highly qualified engineers with Ph.D. in computer architecture for embedded systems. Our expertise is based on nearly ten years of track records in advanced R&D projects and product development. Our strong scientific background allows us to quickly find the best solutions for your project challenges.

Elkefischer – COMPUTER SCIENCE
Elsevier is a leading international publisher of Computer Science journals, books and electronic products. By delivering first class information and innovative tools, we continue to refine our portfolio to serve the research need of Industry professionals, researchers and students worldwide.

We are proud to play an integral part within the computer science community and to participate in the advancement of this field. All our journals are available online via ScienceDirect (www.sciencedirect.com) the essential information resource for over 14 million scientists worldwide.

Visit our booth to meet publishers and editors and view the latest journal information on microelectronics and electronic system design. We will be introducing our new editor for Microelectronics Journal and celebrating the 30th Anniversary of Microelectronic Engineering Journal with various activities.

We look forward to meeting you!

Electronic Services
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Embedded Computing Specialists
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Phone: +32 498/105 795
Email: contact@ecspec.com
Website: www.ecspec.com

Embedded Computing Specialists provides engineering services and solutions for embedded computing. We specialize in R&D projects where you are looking for technology leap or performance breakthrough.

European Project Cluster on Mixed-Criticality Systems (DREAMS, PROXIMA, CONTREX, MultiPARTES)
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R&D Division Transportation
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Email: kim.gruettner@offis.de
Website: www.offis.de

The European Project Cluster on Mixed-Criticality Systems has been started in October 2013 and consists of the following European projects, attacking several challenges and aspects of Mixed-Criticality Systems:

DREAMS, PROXIMA, CONTREX and MultiPARTES. For a detailed description on the individual projects, please have a look at the exhibitor list.

EUROPRACTICE
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IMEC vzw
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Belgium
Phone: +32 16 28 12 48
Email: Carl.Das@imec.be
Website: www.imec.be

The EUROPRACTICE Service offers CAD tools for education, low cost and easy access to ASIC prototype and small volume fabrication. The service is offered by IMEC (B), STFC (UK) and Fraunhofer IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW runs whereby many designs are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemiconductor, austriamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on
Furthermore, Eurotraining establishes the training requirements of EU companies with production or development in Far East and develops dedicated webinars which will be available on www.eurotraining.net.

**PRODUCT FINDER**

Test:
- Design for Test
- Design for Manufacture and Yield
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Prototyping
- Semiconductor IP:
  - Analogue & Mixed Signal IP
- Physical Libraries

**EuroTraining – Training in Nanoelectronics**

**Contact**: Annette Locher
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Email: locher@fsrm.ch
Website: www.eurotraining.net

EuroTraining develops and runs the website www.eurotraining.net offering access to hundreds of courses, summer schools, lecturing material and on-line tutorials in the field of nanoelectronics and micro-nano systems.

The service addresses industry and universities which are also encouraged to share the basic development of courses, text books and training material on the EuroTraining website.

Course providers, universities or European project can announce their training offer on eurotraining.net for free. The events can also be included in the monthly newsletter to over 10'000 addresses. Contact: <mailto:eurotraining polito [dot] it> eurotraining polito [dot] it.

A major challenge in computing is to leverage multi-core technology to develop energy-efficient high performance systems. This is critical for embedded systems with a very limited energy budget as well as for supercomputers in terms of sustainability. Moreover, the efficient programming of multi-core architectures, as we move towards manycores with more than a thousand cores predicted by 2020, remains an unresolved issue. The FlexTiles project will define and develop an energy-efficient yet programmable heterogeneous manycore platform with self-adaptive capabilities. The manycore will be associated with an innovative virtualization layer and a dedicated tool-flow to improve programming efficiency, reduce the impact on time to market and reduce the development cost by 20 to 50%. FlexTiles will raise the accessibility of the manycore technology to industry – from small SMEs to large companies – thanks to its programming efficiency and its ability to adapt to the targeted domain using embedded reconfigurable technologies. Contract number: 288248

**PRODUCT FINDER**

**ASIC and SOC Design**:
- Design Entry
- Behavioural Modelling & Simulation
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design
- System-Level Design:
  - Behavioural Modelling & Analysis
  - Physical Analysis
  - PCB & MCM Design

**Test**:
- Test Automation (ATPG, BIST)
- Silicon Validation
- Mixed-Signal Test
- System Test

**Services**:
- Design Consultancy
- Prototyping

**FlexTiles Consortium**

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**Fraunhofer EMFT**

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Fraunhofer EMFT conducts cutting-edge applied research into sensors and actuators for man and the environment. The core competences of the research departments in Munich and Regensburg with hundred employees include: silicon technology, flexible electronics, chemical sensor materials and the capability of system integration. Each of these core competences in its own right allows new kinds of sensors and actuators to be created. But the real strength of Fraunhofer EMFT lies in the interaction between these areas: after all, innovations often emerge where technologies reach their limits and begin to cross-fertilize. This enables the creation of innovative solutions for various business and application areas. The business area “Design and Test” offers customized services from development of integrated circuits to integrated components as well as complete systems and equipment. The services portfolio also includes multiparametric characterization and reliability prognoses for the planned application.

The Fraunhofer Institute for Integrated Circuits IIS is one of Germany’s most important research facilities for the development of microelectronic systems. The scientists in the Design Automation Division EAS in Dresden work on new methods of modeling, simulation and optimization of systems as well as debugging, analysis and formal verification. These methods ensure that developed complex electronic and mechatronic systems meet the required specifications at every design stage and errors are identified before components are built.

By applying knowledge and innovative solutions, the division aims at achieving a faster, more efficient and last but not least a more cost saving design of products. One goal of particular importance is a high design quality despite ever more complex systems. Thus, our scientists take account of the growing requirements concerning reliability and robustness of systems. The EAS Division is involved in national and international networks in research and numerous standardization activities. Its results of work and developments are applied in microelectronics and its domains, such as communication technology, automotive industry or automation.
PRODUCT FINDER
ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Physical Analysis (Timing, Thermal, Signal)
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design
System-Level Design:
- Behavioural Modelling & Analysis
- Physical Analysis
- Hardware/Software Co-Design
- Package Design
- PCB & MCM Design
Test:
- Design for Test
- Design for Manufacture and Yield
- Test Automation (ATPG, BIST)
- Mixed-Signal Test
- System Test
Embedded Software Development:
- Real Time Operating Systems
- Software/Modelling
Semiconductor IP:
- Analogue & Mixed Signal IP
Application-Specific IP:
- Networking
- Wireless Communication

Incentia

Contact: Lynne Wright

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Incentia Design Systems, Inc. is a leading provider of advanced Timing and Signal Integrity Analysis, Design Closure, and Logic Synthesis software for multi-million-gate nanometre designs. Incentia patented technologies provide the fastest Static Timing Analysis (STA) tool in the market today. Incentia’s products are in use at leading semiconductor, fabless IC design, systems, and design service companies worldwide and have produced numerous customer tape-outs, including those using advanced 40nm technologies and designs over 50 million gates. Incentia is represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to our stand or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER
ASIC and SOC Design:
- Synthesis
- Power & Optimisation
- Physical Analysis (Timing, Thermal, Signal)
Test:
- Design for Test
- Logic Analysis
- Test Automation (ATPG, BIST)
- Boundary Scan

Micronews Media, powered by Yole Développement

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Yole Développement
Le Quartz, 75 Cours Emile Zola
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Phone: +33 472 83 01 01
Email: veyrier@yole.fr
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Founded in 1998, Yole Développement has grown to become a group of companies providing marketing, technology and strategy consulting, media in addition to corporate finance services. With a strong focus on emerging applications using silicon and/or micro manufacturing, Yole Développement group has expanded to include more than 50 associates worldwide covering MEMS, Compound Semiconductors, LED, Image Sensors, Optoelectronics, Multi/fluids & Medical, Photoelectrics, Advanced Packaging, Manufacturing, Ok Nanomaterials and Power Electronics. The group supports industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

MEDIA & EVENTS ACTIVITY:
- i-Micronews.com, online disruptive technologies website
- Weekly WebTalk
- @Micronews, weekly e-newsletter
- Technology Magazines dedicated to MEMS, Advanced Packaging, LED and Power Electronics

PRODUCT FINDER
ASIC and SOC Design:
- Design Entry
- Analogue and Mixed-Signal Design
Services:
- Data Management and Collaboration
- IP e-commerce & Exchange

MOSIS

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Segensworth Road, Fareham, Hants PO15 5RQ
United Kingdom
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Website: www.eda-solutions.com

MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions around the world. Programs offered include SOS, SOI, CMOS and SiGe BICMOS, in geometries from 0.7um to 32nm, from the foundries IBM, TSMC, ON Semiconductor, australian systems, Globalfoundries, and eagne. MOSIS are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to our stand or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER
ASIC and SOC Design:
- Design Entry
- Analogue and Mixed-Signal Design
Services:
- Data Management and Collaboration
**MunEDA GmbH**

*Contact:* Jin Qiu

**OneSpin Solutions GmbH**

*Contact:* Oliver Habeck

**ProPlus Design Solutions, Inc.**

*Contact:* Amit Nanda

**RacyICs GmbH**

*Contact:* Holger Eisenreich

**now publishers inc.**

*Contact:* James Finlay

**PRODUCT FINDER**

**ASIC and SOC Design:**

Behavioural Modelling & Simulation

Power & Optimisation

Physical Analysis (Timing, Thermal, Signal)

Verification

Analogue and Mixed-Signal Design

RF Design

Test:

Design for Manufacture and Yield

---

**MULTIPARTES**

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**OneSpin Solutions GmbH**

*Contact:* Oliver Habeck

**ProPlus Design Solutions, Inc.**

*Contact:* Amit Nanda

**RacyICs GmbH**

*Contact:* Holger Eisenreich

**now publishers inc.**

*Contact:* James Finlay

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RF Design

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**OneSpin Solutions GmbH**

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**ProPlus Design Solutions, Inc.**

*Contact:* Amit Nanda

**RacyICs GmbH**

*Contact:* Holger Eisenreich

**now publishers inc.**

*Contact:* James Finlay

**PRODUCT FINDER**

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**RacyICs GmbH**

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**now publishers inc.**

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RF Design

Test:

Design for Manufacture and Yield
Synflow SAS is an EDA start-up company that helps hardware designers increase their productivity by making design and verification easier. For this purpose, we develop and market EDA software based on a disruptive technology for IP and SoC design combining a new language called C+/C flow and an Eclipse-based IDE that verifies C+/C designs and translates them (on-the-fly) into Verilog and VHDL. We also provide support for our software to help designers learning the C+/C-language faster and master the IDE, as well as advice and tips to write better C+/C code to design IP cores and SoCs with the highest performance possible. We chose to create a new language to provide designers with a modern, hardware-oriented language that is more adapted to their needs.

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**About Synflow**

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allowing any kind of design to be created with ease and efficiency. We also made the choice of generating vendor-neutral, clean, readable Verilog and VHDL that respects the coding rules imposed or recommended by synthesizers and lint tools. Our users have succeeded in designing applications with a mix of control and dataflow up to 10x faster than using RTL with equivalent synthesis results.

The Synflex SAS company was founded by Nicolas Siret and Matthieu Wipliez, two PhDs specialized in hardware engineering and software engineering, who worked on models and code compilation with other researchers in the EU.

**PRODUCT FINDER**

**ASIC and SOC Design:**
Design Entry
Behavioural Modelling & Simulation
Verification

**System-Level Design:**
Behavioural Modelling & Analysis

**Services:**
Prototyping
Encryption IP
Synthesizable Libraries

**Application-Specific IP:**
Telecommunication

**exhibitor company profiles**

**Tanner EDA**

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Tanner EDA provides a complete line of software solutions that cater to design innovation for the market, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. Tanner is represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to our stand or visit the EDA Solutions website www.eda-solutions.com for more details.

**PRODUCT FINDER**

**ASIC and SOC Design:**
Design Entry
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design

**Test:**
Silicon Validation
Mixed-Signal Test

**TOSHIBA**

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In 1987, Toshiba invented NAND Flash technology. Today, Toshiba offers one of the industry's broadest line-ups of NAND Flash-based storage solutions—enabling a wide range of applications in the consumer, mobile, industrial, and enterprise markets. Extending its industry leadership in memory storage solutions, Toshiba offers an innovative new SDHC memory card, "FlashAir", which is the first to support the new Wireless LAN SD standard, SDIO. "FlashAir" is an SD memory card with embedded wireless LAN functionality. It has a built-in web server function and a wireless LAN access point. If power is supplied to the card, FlashAir can work as a server. Files stored in FlashAir are accessible from smartphones, tablets or PCs through Wi-Fi. Ad-hoc local networks between FlashAir and mobile devices are established, so that Internet access or Wi-Fi access points are not needed. The API of FlashAir is disclosed on our TOSHIBA booth to see some demos.

**PRODUCT FINDER**

**Application-Specific IP:**
Wireless Communication

**booth 16**

**University Booth 3**

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The University Booth is part of the DATE 2014 exhibition programme and is sponsored by the DATE Sponsor Committee. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are presenting innovative hardware and software demonstrations. All demonstrations will take place during the exhibition within a dedicated time slot. The University Booth is organized by Jens Lienig (TU Dresden) and Andreas Vörg (edacentrum).

**PRODUCT FINDER**

**ASIC and SOC Design:**
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Thermal, Signal)
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design

on-site download service. Furthermore, FlashAir allows you both peer-to-peer transfers and uploads to and downloads from servers if the device supports SDIO.

FlashAir opens up many new possibilities. Please stop by our TOSHIBA booth to see some demos.
WIRBRATE - Wireless, Self-Powered Vibration Monitoring and Control for Complex Industrial Systems

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WIRBRATE’s key innovation lies in the development of a self-powered, vibration monitoring and control platform. Unlike existing vibration monitoring devices available in the market that operate as individual entities, WIRBRATE’s unique approach is based on individual intelligent sensor-actuator nodes that communicate wirelessly to collaboratively predict impending failures, perform fault diagnosis or provide real-time feedback. This feedback can then be used to further minimise vibration levels using distributed and autonomous micro-actuators that are capable of carrying our robust, distributed control. The use of robust wireless communication strategies ensures that the system is highly flexible and allows for a new class of monitoring and control applications that are not possible using traditional wired systems. Apart from measuring and controlling vibration levels, WIRBRATE’s platform also harnesses the vibration itself thus resulting in a system that is both maintenance free and environment friendly.

PRODUCT FINDER
ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
RF Design
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Hardware/Software Co-Design
PCB & MCM Design
Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Embedded Software Development:
Compilers
Real Time Operating Systems
Debuggers
Software/Modelling
Hardware:
FPGA & Reconfigurable Platforms
Development Boards

Wirtschaftsförderung Sachsen GmbH (WFS)

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We build bridges: Between Saxon companies and cooperation partners from abroad, between potential investors and Saxony’s regions and communes, between research and practice, between business ideas and economic success.

X-FAB Group

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X-FAB is the leading analog/mixed-signal foundry group manufacturing silicon wafers for analog-digital integrated circuits (mixed-signal ICs). As a specialty foundry for so-called “More than Moore” technologies, X-FAB creates a clear alternative to typical foundry services by combining solid, specialized expertise in advanced analog and mixed-signal process technologies with excellent service, a high level of responsiveness and first-class technical support. It manufactures wafers for automotive, industrial, consumer, medical, and other applications on advanced modular CMOS and BiCMOS processes with technologies ranging from 1.0 to 0.13 µm, and special BCD, SOI and MEMS long-lifetime processes. These technologies are not intended for digital applications with the smallest possible structure sizes, but rather are targeted for analog applications that can be integrated with additional functions such as high voltage, non-volatile memory or sensors. Xi with five manufacturing sites in Germany, the U.S. and Malaysia, the company’s combined manufacturing capacity is approximately 62,000 8-inch equivalent wafer starts per month. X-FAB customers benefit from high-performance technologies, excellent technical design and prototyping services; and fast, easy and flexible foundry access worldwide. The company has approximately 2,400 employees worldwide. For more information, please visit www.xfab.com

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Zentrum Mikroelektronik Dresden AG (ZMDI) is a global, innovation-driven, customer-focused enterprise delivering high-performance analog and mixed signal semiconductor solutions for over 50 years. The ZMDI difference is that we partner fully throughout the development of innovative analog and digital power and sensing technologies, expertly exploring your unique system requirements, solving design challenges and then collaboratively designing and delivering subsystem and/or architectural solutions. ZMDI’s solutions enable our customers to create the most energy-efficient products for sensors, power management, and lighting.
Scope of the Event
The 18th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event
The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest
Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical and Healthcare Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems
- Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles
- Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers
All papers have to be submitted electronically by Sunday, September 14, 2014 via: www.date-conference.com
Papers can be submitted either for standard oral presentation or for interactive presentation.
The Programme Committee also encourages proposal submissions for Special Sessions, Tutorials and Friday Workshops as well as submissions for the Special Days on “Designing Electronics for the Internet of Things” and “Designing Electronics for Medical Applications”

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