Workshop

W2 1st RIIF Workshop - Towards Standards for Specifying and Modeling the Reliability of Complex Electronic Systems

Workshop

Agenda

Agenda

Time	Label	Session
08:30	W2.1	**Session 1 : Opening**
08:30	W2.1.1	**Introduction to the RIIF Initiative** Adrian Evans, iROC Technologies, FR
08:50	W2.2	**Session 2 : Processor Reliability**
08:50	W2.2.1	**Improving Server Reliability - A Front-End Design Engineering Perspective** Burcin Aktan, Intel, US
09:25	W2.2.2	**Reliability Availability Serviceability (RAS) of IBM POWER & Mainframe (z) Servers** Michael Müller, IBM, DE
10:00	W2.2.3	**Reliability Modeling Challenges - An IP Provider's Perspective** Peter Harrod, ARM, UK
10:30	W2	**Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
11:00	W2.3	**Session 3 : Reliability in Automotive Applications**
11:00	W2.3.1	**Reliability Modeling for Automotive Semiconductors** Göran Jerke, Bosch, DE
11:20	W2.3.2	**Embedded Tutorial : Using RIIF to Model a Complex Automotive System** Viacheslav Izosimov, Semcon, SE
11:40	W2.3.3	**Robustness Metrics for Automotive Power Microelectronics** Thomas Nirmaier, Infineon, DE
12:00	W2	**Lunch Break** Buffet meal
13:00	W2.4	**Session 4 : Modeling and Dependability**
13:00	W2.4.1	**From Component Reliability to System Dependability: A Modeling and Assessment Perspective** Jean Arlat, LAAS/CNRS, FR
13:25	W2.5	**Session 5 : Panel Discussion** **Panelists:** **Authors**: David Appello[1], Jean Arlat[2], Michael Müller[3], Michael Nicolaidis[4], Göran Jerke[5] and Ulf Schlichtmann[6] [1]ST, FR; [2]LAAS/CNRS, FR; [3]IBM, DE; [4]TIMA Laboratory, FR; [5]Bosch, DE; [6]Technische Universität München, DE
14:25	W2.6	**Session 6 : Poster Session / Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
14:45	W2.7	**Session 7 : Reliability Analysis and Optimization**
14:45	W2.7.1	**Towards Near Zero Cost of Fault Tolerance for Reliable Low Power Designs** Saquib Khursheed, University of Southampton, UK
15:05	W2.7.2	**System-Level Reliability Modeling for MPSoCs** Thidapat Chantem, Utah State University, US
15:20	W2.8	**Session 8 : Next Steps for RIIF**
15:20	W2.8.1	**IEEE Standardization, Case Studies, Working Protocols**

15:50	W2.9	**Closing Remarks** **Moderator:** Oliver Bringmann, FZI / University of Tuebingen, DE

Further information is available at the workshop website.

W4 Platform 2012 / STHORM embedded many-core acceleration

Workshop

Preliminary program

Agenda

Time	Label	Session
08:30	W4.1	**Session 1**
08:30		**Opening of the workshop** Diego Melpignano, STMicroelectronics, IT
08:50		**ST perspectives on programmable accelerators for embedded vision** Éric Flamand, STMicroelectronics, FR
09:20		**CEA vision on multicores architecture evolution** Thierry Collette, CEA, FR
09:50	W4	**Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
10:20	W4.2	**Session 2**
10:20		**Implementation of an Accurate Canny Edge Detector on Platform 2012** Gabriela Nicolescu et al., École Polytechnique de Montréal, CA
10:40		**An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to P2012** Vittorio Zaccaria et al., Politecnico di Milano, IT
11:00		**Complex Embedded Vision Application** Regis Vinciguerra, CEA-LIST, FR
11:20		**FPGA mapping of STHORM, an experimental testbed for the research community** Yassine Hariri and Peter Stokes, CMC Microsystems, CA
11:40		**Leveraging HW IPs in shared memory STHORM clusters** Andrea Marongiu, University of Bologna, IT
12:00	W4	**Lunch Break + demonstrations + posters** Buffet meal
13:00	W4.3	**Session 3**
13:00		**Evaluating Software Managed Memory with MapReduce** Alexandra Fedorova et al., Simon Fraser University, CA
13:20		**Porting Applications to Multicore Platforms: Results from the BIP & MCAPI Tool Chain for STHORM** Julien Mottin[1] and Marius Bozga et al. [2] [1]CEA, FR; [2]VERIMAG, FR
13:40		**Thermal Modeling of Deep Nano-Meter Heterogeneous Many-Core Platforms** David Atienza, EPFL, CH
14:00		**STHORM demos: Object Recognition and Face detection**
14:30	W4	**Coffee Break and Posters Session** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
15:00	W4.4	**Session 4**
15:00		**Run-Time Resource Management on Many-Core STHORM Platform** Patrick Bellasi, Politecnico di Milano, IT
15:20		**Dynamic Voltage and Frequency Management under Thermal Constraints in SoC: Towards an Event-Based Approach** Suzanne Lesecq et al., CEA, FR
15:40		**Supporting dataflow CAL language on STHORM** Marco Mattavelli, EPFL, CH

16:00		**Kernel Genius: a novel approach to vision code generation** Thierry Lepley, STMicroelectronics, FR
16:20	W4.5	**Conclusions of the workshop**

W9 International Workshop on Software Approaches to Resilient System Design

Workshop

Agenda

Agenda

Time	Label	Session
08:30	W9.1	**SESSION 1: OPENING**
08:30	W9.1.1	**Welcome Address** Mehdi Tahoori, Karlsruhe Institute of Technology, DE
08:45	W9.1.2	**Morning Keynote Address: "Who Cares About Reliability?"** Rob Aitken, ARM, US
09:30	W9.2	**SESSION 2: VARIABILITY**
09:30	W9.2.1	**Sensing and Emulating Variability** Puneet Gupta, University of California, Los Angeles, US
10:00	W9.2.2	**Variability Induced Compiler Directed Strategies** Rajesh Gupta, University of California, San Diego, US
10:30	W9	**Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
11:00	W9.3	**SESSION 3: THERMAL AND AGING EFFECTS**
11:00	W9.3.1	**Reliability of On-Chip Systems from a Thermal Perspective** Jörg Henkel, Karlsruhe Institute of Technology, DE
11:30	W9.3.2	**Software Approaches for Aging Modeling and Mitigation** Mehdi Tahoori, Karlsruhe Institute of Technology, DE
12:00	W9	**Lunch Break** Buffet meal
13:00	W9.4	**SESSION 4: CROSS-LAYER RESILIENCE**
13:00	W9.4.1	**Cross Layer Error resilience in MIMO Systems** Norbert Wehn, University of Kaiserslautern, DE
13:30	W9.4.2	**Variability-Aware Memory Management in the Operating System** Alex Nicolau, University of California, Irvine, US
14:00	W9.4.3	**Cross-layer Design of Distributed Embedded Controllers** Dip Goswami, Technische Universität München, DE
14:30	W9	**Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
15:00	W9.5	**SESSION 5: SYSTEM DEPENDABILITY**
15:00	W9.5.1	**Exploiting Variability in Flash Memories Through Non-binary Error Correction Coding** Lara Dolecek, University of California, Los Angeles, US
15:30	W9.5.2	**Brainstorming and discussion for future collaboration** Medhi Tahoori[1] and Puneet Gupta[2] [1]Karlsruhe Institute of Technology, DE; [2]University of California, Los Angeles, US
16:15	W9.6	**Concluding Remarks**

W5 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test

Workshop

Workshop Description

3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. To produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges.

The last four editions of this workshop took place in conjunction with DATE 2009 to DATE 2012.

- DATE 2009, Nice, France (https://www.date-conference.com/date09/conference/workshop-W5),
- DATE 2010, Dresden, Germany (https://www.date-conference.com/date10/conference/workshop-W5),
- DATE 2011, Grenoble, France (https://www.date-conference.com/date11/conference/workshop-W5).
- DATE 2012, Dresden, Germany (https://www.date-conference.com/date12/conference/session/W5).

The call for papers (CFP) for the upcoming workshop to be held in conjunction with DATE 2013 is available **here.**

Topic Areas

You are invited to participate and submit your contributions to the DATE 2013 Friday Workshop on 3D Integration. The areas of interest include (but are not limited to) the following topics:

- *3D technologies: chip-on-chip, micro-bumping, contactless, and through-silicon-vias interconnect*
- *TSV formation, perm./temp. wafer (de-)bonding*
- *3D architectures and design space exploration*
- *3D combinations of logic, memory, analog, RF*
- *Application, product, or test chip case studies*
- *3D design methods and EDA tools*
- *Signal and power integrity, and ESD in 3D*
- *Thermo(-mechanical) analysis and -aware design*
- *Chip-package co-design for 3D*
- *Test, design-for-test, and debug techniques for 3D*
- *Wafer test access, KGD test, thin-wafer handling*
- *Economic benefit/cost trade-off studies*
- *Standardization initiatives*

Submission Instructions

Submissions are invited in the form of (extended) abstracts not exceeding two pages. Submissions must be sent in as PDF file via the Welcome paper submission system: http://welcome.molesystems.com/DATE13-3D-WS/2013/. All submissions will be evaluated for selection with respect to their suitability for the workshop, originality, and technical soundness. Selected submissions can be accepted for regular or poster presentation. At the workshop, an Electronic Workshop Digest will be made available to all workshop participants, which will include all material that authors are willing to provide: abstract, paper, slides, poster, etc.

Paper Submission deadline	**November 25, 2012**
Notification of Acceptance	**December 10, 2012**
Camera-Ready Material due date	**February 22, 2013**

The workshop program contains the following elements.

- One invited keynote address
- Two invited talk
- Two sessions with in total eight regular presentations
- Two poster sessions
- One panel session

Agenda

Agenda

Time	Label	Session
08:30	W5.1	**Session 1: Opening** **Moderator:** Bjørn B. Larsen, NTNU, NO
08:30	W5.1.1	**Welcome Address** Qiang Xu, The Chinese University of Hong Kong, HK
08:40	W5.1.2	**Keynote Address: 3D IC Design and CAD Research: Challenges and Opportunities** Sung Kyu Lim, Georgia Tech, US
09:25	W5.1.3	**Invited Talk: 3D IC Test Challenges and Solutions** Erik Jan Marinissen, IMEC, BE
10:00	W5.2	**Session 2: Posters** Posters - coffee + tea break
10:00		**A NOVEL ON-CHIP TSV-BASED BANDPASS FILTER DESIGN** Khaled MOHAMED, Mentor Graphics, EG
10:00		**EXPLICIT AND UNCONDITIONALLY STABLE METHOD FOR THE FAST 3-D SIMULATION OF STAKED CHIP POWER DISTRIBUTION NETWORKS CONNECTED BY THROUGH SILICON VIA ARRAYS** Tadatoshi SEKINE and Hideki ASAI, Shizuoka University, JP
10:00		**LAYOUT-TECHNOLOGY INTERACTIONS AND OPTIMIZATION OF INTERPOSER BASED DESIGNS** Andy HEINIG and Uwe KNOECHEL, Fraunhofer IIS/EAS, DE
10:00		**PHYSICALLY BASED APPROACH OF SIMPLE COMPACT MODELING FOR 3D INTERCONNECT IN RF CIRCUITS** Fengyuan SUN[1], Jean-Etienne LORIVAL[1], Francis CALMON[1] and christian GONTRAND[2] [1]INL, FR; [2]INSA/INL, FR

10:00 **MODELING OF 3D-IC FABRICATION STEP SEQUENCES**
Armin GRUENEWALD, Kai HAHN and Rainer BRüCK, University of Siegen, DE

10:00 **TSV INTERPOSER FOR 3D WAFER LEVEL SYSTEM IN PACKAGES**
M. Jürgen WOLF, Fraunhofer IZM, DE

10:00 **A NEW TSV TEST METHOD WITH BISECTION**
huiyun LI, Shenzhen Institutes of Advanced Technology, CN

10:00 **WIOMING, A LOW POWER WIDEIO COMPATIBLE 3D CIRCUIT**
Denis Dutoit, Pascal Vivet and Alexandre Valentian, CEA, FR

10:00 **ANALYZING 3D NOC OCCUPANCY AND LATENCY**
Yan GHIDINI, Matheus MOREIRA, Thais WEBBER, Ney CALAZANS and Cesar MARCON, PUCRS, BR

10:30 W5.3 **Session 3: Design, Manufacturing and Test of 3D-Ics**

Moderator:
Haykel Ben Jamaa, CEA-LETI, FR

10:30 W5.3.1 **Silicon Interposers with Through Silicon Vias - A Base Approach for 3D Wafer Level System Integration**
Kai Zoschke[1], Rene Puschmann[1], Oswin Ehrmann[2], Juergen Wolf[1] and Klaus-Dieter Lang[2]
[1]Fraunhofer IZM, DE; [2]Technical U of Berlin, DE

10:53 W5.3.2 **Thermal-aware Energy Efficient Run-Time Incremental Mapping for 3-D Networks-on-Chips**
Xiaohang Wang[1], Mei Yang[2], Yingtao Jiang[2], Maurizio Palesi[3] and Terrence Mak[4]
[1]Guangzhou Ins. of Adv. Tech., CN; [2]U of Nevada, US; [3]Kore U, IT; [4]The Chinese University of Hong Kong, HK

11:15 W5.3.3 **3D MPSoC Design Using 2D EDA tools: Analysis of Parameters**
Mohamad Jabbar[1], Abir M'Zah[2], Omar Hammami[2] and Dominique Houzet[3]
[1]GIPSA-Lab/ENSTA Paristech, FR; [2]ENSTA Paristech, FR; [3]GIPSA-Lab, FR

11:38 W5.3.4 **Pre-bond Test of TSVs in 3D SICs using Ring Oscillators**
Yassine Fkih[1], Pascal Vivet[2], Bruno Rouzeyre[3], Marie-lise Flottes[3] and Giorgio Di Natale[3]
[1]CEA-Leti / LIRMM U Montpellier II, FR; [2]CEA-Leti, FR; [3]LIRMM U Montpellier II, FR

12:00 W5 **Lunch Break**

Buffet meal

13:00 W5.4 **Session 4: Performance, Reliability and Cost Modelling of 3D Ics**

Moderator:
Rishad A. Shafik, University of Bristol, UK

13:00 W5.4.1 **MoNICA: A Performance- and Thermal-Aware Floorplan Tool for Heterogeneous 3D NoC-based MPSoCs**
Felipe Frantz[1], da Silva Matos[2], Lioua Labrak[1], Fabien Clermidy[3], Ian O'Connor[1], Luigi Carro[2] and Altamiro Susin[2]
[1]Lyon Institute of Nanotechnology, FR; [2]Federal U of Rio Grande do Sul, BR; [3]CEA-Leti, FR

13:23 W5.4.2 **Short-Circuit Current Free NEMFET Based Logic and NEMFET-MOS Hybrid 3D Memory**
Marius Enachescu, Mihai Lefter, George Razvan Voicu and Sorin D. Cotofana, Delft U of Tech., NL

13:45 W5.4.3 **3D-COSTAR: A Cost Model for 3D Stacked Ics**
Mottaqiallah Taouil[1], Said Hamdioui[1], Erik Jan Marinissen[2] and Sudipta Bhawmik[3]
[1]Delft U of Tech., NL; [2]IMEC, BE; [3]Qualcomm, US

14:08 W5.4.4 **WIOMING, a Low Power Wide IO compatible 3D circuit**
Denis Dutoit, Pascal Vivet and Alexandre Valentian, CEA, FR

14:30 W5.5 **Session 5: Posters**

Posters - coffee + tea break

14:30 **A NOVEL ON-CHIP TSV-BASED BANDPASS FILTER DESIGN**
Khaled MOHAMED, Mentor Graphics, EG

14:30 **EXPLICIT AND UNCONDITIONALLY STABLE METHOD FOR THE FAST 3-D SIMULATION OF STAKED CHIP POWER DISTRIBUTION NETWORKS CONNECTED BY THROUGH SILICON VIA ARRAYS**
Tadatoshi SEKINE and Hideki ASAI, Shizuoka University, JP

14:30 **LAYOUT-TECHNOLOGY INTERACTIONS AND OPTIMIZATION OF INTERPOSER BASED DESIGNS**
Andy HEINIG and Uwe KNOECHEL, Fraunhofer IIS/EAS, DE

14:30 **PHYSICALLY BASED APPROACH OF SIMPLE COMPACT MODELING FOR 3D INTERCONNECT IN RF CIRCUITS**
Fengyuan SUN[1], Jean-Etienne LORIVAL[1], Francis CALMON[1] and christian GONTRAND[2]
[1]INL, FR; [2]INSA/INL, FR

14:30 **MODELING OF 3D-IC FABRICATION STEP SEQUENCES**
Armin GRUENEWALD, Kai HAHN and Rainer BRüCK, University of Siegen, DE

14:30 **TSV INTERPOSER FOR 3D WAFER LEVEL SYSTEM IN PACKAGES**
M. Jürgen WOLF, Fraunhofer IZM, DE

14:30 **A NEW TSV TEST METHOD WITH BISECTION**
huiyun LI, Shenzhen Institutes of Advanced Technology, CN

14:30 **WIOMING, A LOW POWER WIDEIO COMPATIBLE 3D CIRCUIT**
Denis Dutoit, Pascal Vivet and Alexandre Valentian, CEA, FR

14:30 **ANALYZING 3D NOC OCCUPANCY AND LATENCY**
Yan GHIDINI, Matheus MOREIRA, Thais WEBBER, Ney CALAZANS and Cesar MARCON, PUCRS, BR

15:00 W5.6 **Session 6: Invited Talk**

Moderator:
Denis Dutoit, CEA-LETI, FR

15:00 W5.6.1 **Expanding the Design-Manufacturing Interface for 3D IC**
Juan Rey, Mentor Graphics, US

15:40 W5.7 **Session 7: Panel Discussion**

Moderator:
Pascal Vivet, CEA-Leti, FR

Panelists:
Panelists:
Paul Franzon[1], Georg Kimmich[2], Juan Rey[3], Ravi Varadarajan[4] and Milojevic Dragomir[5]
[1]University North Carolina, US; [2]STEricsson, FR; [3]Mentor Graphics, US; [4]Atrenta, FR; [5]IMEC, BE

16:40 W5.8 **Close**

W8 Workshop on Industry-Driven Approaches for Cost-effective Certification of Safety-Critical, Mixed-Criticality Systems (WICERT)

Workshop

Agenda

Agenda

Time	Label	Session
08:30	W8.0	**Workshop Introduction** **Speaker:** Huáscar Espinoza, TECNALIA, ES
08:45	W8.1	**KEYNOTE 1**
08:45	W8.1.1	**MULCORS - The Use of MULticore proCessORs in airborne Systems. Project EASA.2011.OP.30. (study done for EASA: European Aviation Safety Agency)** Marc Gatti and Guy-Andre Berthon, Thales Avionics, FR
09:20	W8.2	**Session 1: Mixed-criticality HW/SW platforms** **Chair:** Rolf Ernst, TU Braunschweig, DE
09:20	W8.2.1	**Isolation of Cores** Claus Stellwag[1], Swapnil Gandhi[2] and Thorsten Rosenthal[2] [1]Elektrobit, DE; [2]Delphi, DE
09:35	W8.2.2	**Open platform for mixed-criticality applications** Miguel Méndez[1], José Luis Gutiérrez Rivas[2], David Fernández García-Valdecasas[2] and Javier Díaz Alonso[2] [1]Seven Solutions, ES; [2]University of Granada, ES
10:00	W8.2.3	**Servosystem control for theatre stage equipment** Pavel Zemcik[1], Sevcovic Jiri[1], Pavol Korcek[2], Michal Kajan[1] and Josef Strnadel[1] [1]Faculty of Information Technology, CZ; [2]Camea, CZ
10:15	W8	**Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
10:45	W8.3	**Session 2: Certification on aerospace, automotive and automation industries with mixed-criticality** **Chair:** Uwe Kremer, TÜV, DE
10:45	W8.3.1	**Hardware and Software Support for Mixed-Criticality Multicore Systems** Glenn Farrall[1], Claus Stellwag[2], Jonas Diemer[3] and Rolf Ernst[3] [1]Infineon, UK; [2]Elektrobit, DE; [3]TU Braunschweig, DE

11:10 W8.3.2 **IFCIMA - Incremental Functional Certification on Integrated Modular Avionics (IMA)**
Franck Aimé, Thales Avionics, FR

11:35 W8.3.3 **Impact of multicore platforms in hardware and software certification**
Risto Nevalainen[1], Uwe Kremer[2], Oscar Slotosch[3], Dragos Truscan[4] and Vicky Wong[5]
[1]Spinet, FI; [2]TÜV, DE; [3]Validas, DE; [4]Åbo Akademi, FI; [5]SpaceSystems Finland, FI

12:00 W8 **Lunch Break**

Buffet meal

13:00 W8.4 **KEYNOTE 2**

13:00 W8.4.1 **Industrial practice on mixed-criticality engineering and certification in the aerospace industry**
Ondrej Kotaba, Honeywell, CZ

13:30 W8.5 **Session 3: Methods and tools for cost-effective certification of safety critical systems**

Chair:
Huáscar Espinoza, TECNALIA, ES

13:30 W8.5.1 **Methods and tools for reducing certification costs of mixed-criticality applications on multi-core platforms: the RECOMP approach**
Paul Pop[1], Leonidas Tsiopoulos[2], Sebastian Voss[3], Oscar Slotosch[4], Christoph Ficek[5], Ulrik Nyman[6] and Alejandra Ruiz Lopez[7]
[1]Technical University of Denmark, DK; [2]Åbo Akademi, FI; [3]fortiss, DE; [4]Validas, DE; [5]Symtavision, DE; [6]Aalborg University, DK; [7]TECNALIA, ES

13:55 W8.5.2 **Towards Model-Driven Engineering for Mixed-Criticality Systems: MultiPARTES Approach**
Alejandro Alonso[1], Christophe Jouvray[2], Salvador Trujillo[3], Miguel A. de Miguel[1], Cyril Grepet[2] and José Simó[4]
[1]Universidad Politécnica de Madrid, ES; [2]Trialog, FR; [3]Ikerlan-IK4, ES; [4]Universidad Politécnica de Valencia, ES

14:20 W8.5.3 **Multicore In Real-Time Systems - Temporal Isolation Challenges Due To Shared Resources**
Ondrej Kotaba[1], Michael Paulitsch[2], Stefan Petters[3], Henrik Theiling[4] and Jan Nowotsch[2]
[1]Honeywell, CZ; [2]EADS, DE; [3]ISEP, PT; [4]SYSGO, DE

14:45 W8 **Coffee Break**

Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.

15:00 W8.6 **Demonstrators and Poster session: Paralell demonstrators and posters**

Chair:
Simon Brewerton, Infineon Technologies, UK

15:00 W8.6.1 **Mixed-Critical Multi-Processor Motor Controller with Capabilities for Runtime Update of Software**
Simon Holmbacka[1], José Luis Gutiérrez Rivas[2] and Miguel Méndez[3]
[1]Åbo Akademi, FI; [2]University of Granada, ES; [3]Seven Solutions, ES

15:00 W8.6.2 **RECOMP Demonstration of Mixed-Criticality Approach**
Claus Stellwag[1], Natalia Willey[2], Swapnil Gandhi[3] and Thorsten Rosenthal[3]
[1]Elektrobit, DE; [2]Delphi, FR; [3]Delphi, DE

15:00 W8.6.3 **Emergency Shutdown System Demonstrator**
Anton Hattendorf and Sebastian Voss, fortiss, DE

15:00 W8.6.4 **Tools for Compliance Management and Compositional Safety Assurance**
Alejandra Ruiz and Huáscar Espinoza, TECNALIA, ES

16:15 W8.7 **Wrap Up**

Chair:
Javier Díaz Alonso, University of Granada, ES

Further information are available at the workshop website.

W7 Reconfigurable Computing V2.0: The Next Generation of Technology, Architectures and Design Tools

Workshop

Organisers

Dr.-Ing. Diana Göhringer

Dr.-Ing. Göhringer works since 2001 in the domain of reconfigurable hardware. She graduated from the University of Karlsruhe in 2006 and finished her PhD at the Karlsruhe Institute of Technology (KIT) in 2011 with "summa cum laude". Since 2012, she leads the Young Investigator Group "CADEMA" at the KIT, where she focuses specifically on reconfigurable computing and multicore architectures. Dr. Göhringer is main- and coauthor of more than 40 highly relevant scientific papers in conferences, journals and book chapters.

Prof. Dr.-Ing. habil. Michael Hübner

Prof. Hübner is the Chair of Embedded Systems in Information Technology at the Ruhr-University of Bochum. He graduated at the University of Karlsruhe in 2003 and received his PhD in 2007 from the same University. He finished his habilitation in "reconfigurable computing systems" in 2011 at the Karlsruhe Institute of Technology (KIT). Prof. Hübner works since more than a decade in the domain of reconfigurable computing and is main- and coauthor of more than 130 scientific publications in highly relevant conference proceedings, journals and book chapters.

Description

Reconfigurable computing gained interest in the scientific and industrial community many years ago. It targeted the substitution of application specific integrated circuits (ASICs) by offering additional benefits, such as flexibility at design- and runtime. Since this time, various trends were followed and led to different generalizations and specializations e.g. through the offer of specific chips with more digital signal processing units or more logic cells or even embedded processors such as the Power PC 405 in Xilinx Virtex II Pro Field Programmable Gate Array (FPGA). In the meanwhile, other technologies such as Graphic Processing Units (GPUs) entered the marked and established themselves in the domain of high performance computing and nowadays also in embedded computing. However, the vendors of FPGAs continued improving the architectures, and the technology of their devices as well as the design tools and programming environments. Novel high performance architectures such as the Xilinx Zynq or Microsemi Smart Fusion, tailored for the embedded market, are some examples that the FPGA market is still growing. Virtual development platforms such as provided e.g. from Cadence enable an efficient design of complex systems without building a prototype in early stages of the development phase. Especially, this example shows how former hurdles will be bridged by introducing novel development tools for the chips which could be programmed in former times only by specialists. The introduction of novel technologies like MRAM, FRAM and also MEMRISTOR will further revolutionize the FPGA hardware and lead to a new era of reconfigurable computing.

This workshop will enable participants to take part in the most novel technology, architecture and design tools provided by the key players, but also from small and medium enterprises and researchers working at the cutting edge of technology. The unique constellation of the speakers which have sufficient time to talk about the novel chips will enable a deep insight into a promising reconfigurable computing future.

Confirmed speakers

- Dr. Ivo Bolsens, CTO Xilinx Inc., San Jose, US
- Steven Perry, Software Tools Architect, Altera, High Wycombe, UK
- Dr. Laurent Rougé, CEO and founder of Menta, Montpellier, FR
- Prof. Ahmed Jerraya, CEA Leti, Grenoble, FR
- Dr. Hichem Belhadj, VP Sales at Microsemi, US

Agenda

Agenda

Time	Label	Session
08:30	W7.0	**Welcome Session** **Chairs:** Diana Göhringer, KIT, DE Michael Hübner, Ruhr-U Bochum, DE
09:00	W7.1	**Session 1: System-on-Chip FPGAs from Xilinx and Altera: Novel Architectures and Design Tools** **Chair:** Diana Göhringer, KIT, DE
09:00	W7.1.1	**FPGA's Entering the Era of All Programmable SoCs** Ivo Bolsens, Xilinx, US
09:45	W7.1.2	**The role of the ARM instruction set architecture in a world of heterogeneity** John Goodacre, ARM, UK
10:30	W7	**Coffee Break and Poster Session** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
11:00	W7.2	**Session 2: Flexibility with Embedded FPGAs** **Chair:** Michael Hübner, Ruhr-U Bochum, DE
11:00	W7.2.1	**High Level Design Convergence for SoC FPGAs** Steven Perry, Altera, UK
12:00	W7	**Lunch Break** Buffet meal
13:00	W7.3	**Session 3: Novel Architectures and Technologies** **Chair:** Diana Göhringer, KIT, DE
13:00	W7.3.1	**SmartFusion2 for industrial and harsh environment applications** Hichem Belhadj, Microsemi, US
13:45	W7.3.2	**FPGA goes 3D** Ahmed Jerraya, CEA-Leti, FR
14:30	W7	**Coffee Break and Poster Session** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
15:00	W7.4	**Interactive Panel** **Organiser:** Michael Hübner, Ruhr-U Bochum, DE **Panelists:** **Authors**: Ivo Bolsens[1], Steven Perry[2], Laurent Rougé[3], Ahmed Jerraya[4] and Hichem Belhadj[5] [1]Xilinx, US; [2]Altera, UK; [3]Menta, FR; [4]CEA-Leti, FR; [5]Microsemi, US

16:00	W7.5	**Closing Session** **Chairs:** Diana Göhringer, KIT, DE Michael Hübner, Ruhr-U Bochum, DE

Further infromation is availabel at the workshop website.

W6 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications

Workshop

Preliminary Programme

Agenda

Time	Label	Session
08:30	W6.1	**Opening Session** **General Co-Chairs:** João Cardoso, Universidade do Porto, PT Cristina Silvano, Politecnico Milano, IT Dimitrios Soudris, National Technical University of Athens, GR
08:45	W6.2	**Morning Session on Many-Core Architectures and Compilers**
08:45	W6.2.1	**Invited Talk: "Multiprocessor Systems for H.264/AVC video encoding: A platform approach"** Sri Parameswaran, University of New South Wales, AU
09:45	W6.2.2	**Invited Talk: "C Compilation in the Dark Age of Many-Core Programming"** Marcel Beemster, ACE Associated Compiler Experts, NL
10:30	W6.3	**Architectures - Posters Session - Coffee Break (Posters program will be posted online)** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
11:00	W6.4	**Embedding High Performance Computing: A supercomputer in your pocket or ultra low power exaflop design?** **Panel Organiser and Moderator:** Georgi Gaydadjiev, Chalmers University of Technology, SE **Panelists:** Todd Austin, The University of Michigan, US Patrick Blouet, ST Ericsson, FR John Goodacre, ARM, UK Andreas Moshovos, University of Toronto, CA Alex Ramirez, Barcelona Supercomputing Center, ES Eugenio Villar, University of Cantabria, ES Bringing together experts from embedded computing and high-performance computing, this panel is organized to open the discussion about the common research challenges and synergies in these two areas, which have been recently magnified by the increasing ubiquity of many-cores and heterogeneity across the whole computing spectrum.
12:00	W6	**Lunch Break** Buffet meal
13:00	W6.5	**Afternoon Session on Design Tools and Applications for Many-Core Architectures**
13:00	W6.5.1	**Invited Talk: "The role of runtime system management in dynamic execution environments", Dionisios Pnevmatikatos, Technical University of Crete, Greece.**
14:00	W6.5.2	**Panel on: "Lessons learnt from European Projects: 2PARMA, COMPLEX, DESYRE, ERA, FASTER, MADNESS, PARAPHRASE, REFLECT, SMECY and TERAFLUX "** William Fornaciari[1], Philipp A. Hartmann[2], Stephan Wong[3], Dionisios Pnevmatikatos[4], Luigi Raffo[5], Kevin Hammond[6], Zlatko Petrov[7], Francois Pacull[8] and Roberto Giorgi[9] [1]Politecnico di Milano, IT; [2]OFFIS, DE; [3]TU Delft, NL; [4]Technical University of Crete, GR; [5]Università di Cagliari, IT; [6]University of St. Andrews, UK; [7]Honeywell, CZ; [8]CEA, FR; [9]Università di Siena, IT Georgi Gaydadjiev, Chalmers University of Technology, SE This panel is organized to present and discuss final outcomes and lessons learnt from the following on-going EU funded projects: 2PARMA (PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures, www.2parma.eu/), COMPLEX (COdesign and power Management in PLatform-based design space Exploration, http://complex.offis.de/), DeSyRe (DeSyRe: on-Demand System Reliability http://www.desyre.eu/), ERA (Embedded Reconfigurable Architecture, www.era-project.eu/), FASTER (Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration www.fp7-faster.eu/), MADNESS (Methods for predictAble Design of heterogeneous Embedded Systems with adaptivity and reliability Support, www.madness project.org/), PARAPHRASE (Parallel Patterns for Adaptive Heterogeneous Multicore Systems, http://paraphrase-ict.eu/) REFLECT (Rendering FPGAs to Multi-Core Embedded Computing, www.reflect-project.eu/), SMECY (Smart Multicore Embedded Systems, www.smecy.eu and TERAFLUX (Exploiting Dataflow Parallelism in Teradevice Parallelism www.teraflux.eu).

15:00	W6.6	**European Projects Parallel Demos Session - (Demos program will be posted online) - Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
15:30	W6.7	**Design Tools and Application -- Posters Session (Posters program will be posted online)**
16:30	W6.8	**Final Wrap up**

W3 International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2013)

Workshop

Agenda

Agenda

Time	Label	Session
08:15	W3	**Welcome and introduction** **Organisers:** Nikil Dutt, University of California, US Philippe Coussy, Université de Bretagne-Sud, FR
08:30	W3.0	**Session 0**
08:30	W3.0.1	**Brain: principles & modeling abstractions** Jeff Krichmar, University of California, US
09:00	W3.1	**Session 1**
09:00	W3.1.1	**Simulating the brain without a computer - Achievements and Challenges of Brain Inspired Computing** Karlheinz Meier and Simon Friedman, Heidelberg University, DE
09:30	W3.1.2	**Neuromorphic Visual Systems on FPGAs** Vijaykrishnan Narayanan, Pennsylvania State University, US
10:00	W3	**Coffee Break & Poster/demo session 1** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
11:00	W3.2	**Session 2**
11:00	W3.2.1	**When neural networks meet error-correction coding: new perspectives in associative memories** Claude Berrou, Telecom Bretagne, FR
11:30	W3.2.2	**The emergent microconnectome of neocortical circuitry** Sean Hill, INCF, US
12:00	W3	**Lunch Break** Buffet meal
13:00	W3.3	**Session 3**
13:00	W3.3.1	**SpiNNaker: a Biologically-Inspired Massively-Parallel Architecture** Steve Furber and Alexander Rast, Manchester University, UK
13:30	W3.3.2	**Hierarchical event-based reconfigurable systems for cognitive neuromorphic engineering** Emre Neftci and Gert Cauwenberghs, University of California, San Diego, US
14:00	W3	**Coffee Break & Poster/demo session 2** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
15:00	W3.4	**Session 4**
15:00	W3.4.1	**UPSIDE - Unconventional Processing of Signals for Intelligent Data Exploitation** Dan Hammerstrom, DARPA, US
15:30	W3.4.2	**A Scalable Analog Neuromorphic Learning System** Narayan Srinivasa, HRL, US
16:00	W3.4.3	**A closed-loop neurobotic system for fine touch sensing** Angelo Arleo, Université Pierre et Marie Curie, FR
16:30	W3	**Wrap up and close** **Organisers:** Nikil Dutt, University of California, US Philippe Coussy, Université de Bretagne-Sud, FR

Poster session #1 and #2

On the computational role of astrocyte – neuron coupling in brain function

Liam McDaid and Jim Harkin (UniversityofUlster-UK)

Advances in Scalable Interconnect for Bio-Inspired Computational Platforms
Jim Harkin, Snaider Carrillo and Liam McDaid (University ofUlster -UK)

Experimental study of electrical Morris-Lecar neuron

Rachid Behdad[1], Stéphane Binczak[1], Vladimir I Nekorkin[2], Alexey S Dmitrichev[2] and Jean-Marie Bilbault[1] ([1]Université de Bourgogne – FR, [2]Institute of Applied Physics of RAS - RU)

Hardware architecture of Self-Organizing Maps
Laurent Rodriguez, Laurent Fiack and Benoît Miramond (ENSEA/ETIS - FR)

Validation of neural networks onto FPGA
Laurent Rodriguez[1], Laurent Fiack[1], Benoît Miramond[1] and Erik Hochapfel[2] ([1]ENSEA/ETIS, [2]Adacsys - FR)

A Neuromorphic VLSI Implementation of a Simplified Electrosensory System in a Weakly Electric Fish
Syed Ahmed Aamir, Jacob Engelmann, Leonel Gomez and Elisabetta Chicca (University ofBielefeld - DE)

Training Scheme Analysis for Memristor-Based Neuromorphic Design
Miao Hu[1], Hai Li[1], Qing Wu[2], Garrett S. Rose[2] and Yiran Chen[1] ([1]University of Pittsburgh, [2]Air Force Research Laboratory - US)

Bio-Inspired Artificial Olfactory System
Ping-Chen Huang and Jan Rabaey (UniversityofCaliforniaatBerkeley- US)

Event management for large scale event-driven digital hardware spiking neural networks
Louis-Charles Caron[1], Michiel D'Haene[2], Frédéric Mailhot[3], Benjamin Schrauwen[2] and Jean Rouat[3] ([1]ENSTA ParisTech - FR, [2]Universiteit Gent - BE, [3]Université de Sherbrooke - CA)

Embedded Hardware Spiking Neural Network for UWB Bladder Volume Classification
Finn Krewer[1], Fearghal Morgan[1], Sandeep Pande[1], Martin O'halloran[1], Brian Mc Ginley[1], Seamus Cawley[1], Jim Harkin[2] and Liam Mc Daid[2] ([1]National University of Ireland – IR, [2]University of Ulster - UK)

Towards Formalization of Embedded Brain Reading
Elsa Andrea Kirchner and Rolf Drechsler (UniversityofBremen- DE)

Learning visual stimuli in neuromorphic VLSI
Federico Corradi[1], Massimiliano Giulioni[2], Vittorio Dante[2] and Paolo Del Giudice[2] ([1]Institute of neuroinformatics - CH, [2]Italian National Institute of Health - IT)

Design Exploration of EMBRACE Hardware Spiking Neural Network Architecture
Sandeep Pande and Fearghal Morgan (NationalUniversity ofIreland - IR)

A VLSI chip with spike-based synaptic plasticity for online learning in real-time
Fabio Stefanini[1], Mattia Rigotti[2], Stefano Fusi[2] and Giacomo Indiveri[1] ([1]University of Zurich and ETHZ – CH, [2]ColumbiaUniversity -US)

Brain Inspired Information Association on Hardware
Khadeer Ahmed, Wei Liu and Qinru Qiu (SyracuseUniversity- US)

Learning visual stimuli in neuromorphic VLSI
Federico Corradi[1], Massimiliano Giulioni[2], Vittorio Dante[2] and Paolo Del Giudice[2] ([1]Institute of neuroinformatics - CH, [2]Italian National Institute of Health - IT)

W1 ESCUG 2013: ESL - Putting the Pieces Together: Integrating SystemC Design and Verification with AMS and Algorithm Design

Workshop

Agenda

Agenda

Time	Label	Session
08:30	W1.1	**Opening Session**
08:30		**Welcome and Opening** Laurent Maillet-Contoz, STMicroelectronics, FR
08:35	W1.2	**Keynote Session**
08:35		**Multi Physical Domain Applications Challenges: Design Flow integration** Serge Scotti, STMicroelectronics, FR
09:00	W1.3	**Design Methodology Session**
09:00		**Towards Co-Design of HW/SW/AMS System** Christoph Grimm, TU Kaiserslautern, DE
10:00	W1	**Coffee Break** Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.
10:30	W1.4	**Virtual Prototyping Session**
10:30		**Virtual Prototyping for High Performance Mixed Signal Products** Martin Barnasconi, NXP Semiconductors, NL
11:30	W1.5	**SystemC AMS Session 1**
11:30		**AMS IP Handling and Simulation** Karsten Einwich, Fraunhofer IIS, DE

12:00 W1 **Lunch Break**

Buffet meal

13:00 W1.5 **SystemC AMS Session 2**

13:00 **AMS IP Handling and Simulation**
Karsten Einwich, Fraunhofer IIS, DE

13:30 W1.6 **SystemC TLM Session**

13:30 **Improving Timing Accuracy for TLM-LT Models**
Simon Hufnagel, Bosch, DE

14:30 W1 **Coffee Break**

Monday and Friday morning and afternoon coffee breaks will be located in the Salle de Reception. On Tuesday-Thursday the breaks will be located in the Exhibition Hall. Morning and afternoon (with the exception of Thursday afternoon which is a 30 minute break) coffee breaks on Tuesday-Thursday are extended breaks and will run for 60 minutes (coffee points will be open for the first 30 minutes only) from the start time indicated in the programme.

15:00 W1.7 **Town Hall Meeting Session: Interactive Discussion on "ESL Integration Experience"**

Moderator:
Laurent Maillet-Contoz, STMicroelectronics, FR

16:20 **Wrap-Up & Closing**
Laurent Maillet-Contoz, STMicroelectronics, FR

16:50 W1 **Close**

Complementary Documentation

Will be provided before the event!
