advance programme

Design, Automation & Test in Europe

Grenoble, France
March 18 - 22, 2013

www.date-conference.com

WELCOME welcome to DATE 13

Dear Colleague,

We proudly present to you the Advance Programme of DATE 13. DATE combines the world's favourite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design. DATE 2013 received 1002 paper submissions; an all-time high for DATE and a 9% increase over DATE'12. 829 of those submissions were eligible for review. DATE being a European conference, the largest share (43%) of those submissions came from Europe. However, with 26% of submissions from North-America, 25% from Asia, and 6% from the rest of the world, DATE clearly demonstrates its global reach and impact.

For the 16th successive year DATE has prepared an exciting technical programme, with the help of the 332-members strong Technical Programme Committee, who dedicated their time to perform 3386 reviews (more than four per submission) and select 136 (=16.4%) "long", 70 (= 8.4%) "short", and 96 (= 11.6%) "interactive presentation" papers.

This year the conference will be held in France, at the Alpexpo in Grenoble and will span an entire working week starting on Monday March 18 with tutorials, and ending on Friday March 22 with workshops.

The **plenary keynote speakers** on Tuesday are Benedetto Vigna, Executive VP of ST Microelectronics to talk about 'Smart Systems for Internet of Things', and Massoud Pedram, Professor at the University of Southern California, to talk about 'Creating a Sustainable Information and Communication Infrastructure'. On the same day, the **Executive Track** offers a series of business panels discussing hot topics in design. To emphasise that DATE is the major event for the designers, DATE 13 features invited sessions where **Europe's famous consumer industry presents its best designs and design practices.**

The main conference programme from Tuesday to Thursday includes 77 technical sessions organised in parallel tracks from four areas:

D – Design Methods, Tools, Algorithms and Languages
A – Application Design
T – Test and Reliability
E – Embedded Software

Extra tracks are dedicated to the Executive Day on Tuesday and the two special days: **"High-Performance Low-Power Computing"** Day on Wednesday and **"Electronic Technologies for Smart Cities"** Day on Thursday.

There is a lunch-time Keynote on Wednesday by John Goodacre of ARM, who will talk on 'Energy-Efficient Computing'. A second Lunch-time Keynote on Thursday by Francesco Profumo, Italian Minister of Education, University, and Research, and Genevieve Fiorasa, French Minister for Higher Education and Research will be on "Smart Cities and Communities at the Regional, National, and European Levels". Additionally, there are 96 Interactive Presentations which are organised into five IP sessions.

Finally, DATE offers a comprehensive overview of commercial design and verification tools in its exhibition including vendor seminars and abundant networking possibilities with fringe meetings.

We wish you a productive and exciting DATE 13 and a memorable social party on Wednesday evening.

DATE 13 General Chair Enrico Macii, Politecnico di Torino, IT

DATE 13 Programme Chair Erik Jan Marinissen, IMEC, BE

plenary session

Tuesday, March 19, 2013, 0830 – 1030

Opening Address – Awards – Keynote Speakers

first keynote address

Smart systems for internet of things

Benedetto Vigna -
Executive VP of STMicroelectronics, IT

Sensors add intelligence to systems which represent a broad class of devices incorporating functionalities like sensing, actuation, and control. They are the core of smart components and subsystems; then, the challenge in the realization of such smart systems goes beyond the design of the individual components and subsystems and consists of accommodating a multitude of functionalities, technologies, and materials to play a key role to augment our daily life.

second keynote address

Creating a sustainable information and communication infrastructure

Massoud Pedram -
Professor at University of Southern California, US

Modern society's dependence on information and communication infrastructure (ICI) is so deeply entrenched that it should be treated on par with other critical lifelines of our existence, such as water and electricity. As is the case with any true lifeline, ICI must be reliable, affordable, and sustainable. Meeting these requirements (especially sustainability) is a continued critical challenge, which will be the focus of my talk. More precisely, I will provide an overview of information and communication technology trends in light of various societal and environmental mandates followed by a review of technologies, systems, and hardware/software solutions required to create a sustainable ICI.

wednesday lunchtime keynote

Wednesday March 20, 2013, Room Oisans 1330 – 1400

Energy efficient computing

John Goodacre, ARM, UK

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

thursday lunchtime keynote

Thursday March 21, 2013, Room Oisans 1330 – 1400

Smart Cities And Communities At The Regional, National And European Levels

Francesco Profumo,
Italian Minister of Education, University and Research

Genevieve Fioraso,
French Minister for Higher Education and Research

general information

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 13. Full General Information covering full technical programme details, conference registration costs and booking forms, hotel reservations and booking forms, travel to and in Grenoble, and social event details is available on the conference website - **www.date-conference.com**

interactive programme on web

A fully interactive DATE 13 programme is available on the web – **www.date-conference.com** - where you will be able to view the entire detail of the programme and plan your attendance in advance.

venue

The Conference will take place from 18-22 March 2013 and the Exhibition from 19-21 March 2013 in Alpexpo, Avenue d'Innsbruck, Grenoble, France - **www.alpexpo.com**

date party – wednesday

This year the DATE party will take place in the World Trade Center, Grenoble. The evening will feature a buffet style dinner with plenty of buffet points and drinks to accompany dinner. In an enjoyable atmosphere participants will have the opportunity to meet and mingle with their friends and colleagues. All conference attendees, users, vendors and their guests are encouraged to come to the party. Additional tickets for the full Evening Social Programme may be obtained for 75 Euros each (see website for booking forms). Entrance will be by ticket only, so please check that you receive the party ticket when you register.

interactive presentations

Chair: Oliver Bringmann, FZI Karlsruhe, DE

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area.

Interactive Sessions will be held in the Exhibition Hall area in 30-minute time slots during coffee and exhibition breaks. Coffee and water will be available during the sessions.

executive sessions – tuesday

Organiser:
Yervant Zorian, Synopsys, US

DATE 2013 will again feature an Executive Track of presentations by leading company executives representing a range of semiconductor manufacturers, EDA vendors, fables houses and IP providers. This one-day program will be held on Tuesday 19 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks.

All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view.

2.1 EXECUTIVE SESSION - Advanced Technology Nodes: Dependency on Collaboration

– see page 27

3.1 EXECUTIVE SESSION – The Role of Prototyping in Today's SOCs

– see page 33

4.1 EXECUTIVE SESSION - Is Reusing Off-the-Shelf Semiconductor IP Possible Today

– see page 40

Organiser:
Ahmed Jerraya, CEA-Leti, FR

High-Performance, Low-Power Computing

Energy-efficiency has played a key role in our lives thus allowing the emergence of new products such as mobile phones and digital TV and all other kinds of consumer products. The computing part determines the effectiveness of many, if not all, of these products. The main indicator of that effectiveness is energy-efficiency, i.e. having higher performance while lowering power consumption.

The environmental pressure is generating stringent constraints on computing systems where energy-efficiency needs to be improved by a factor 50 in the next five years. To reach this goal, system and architecture solutions need to be aligned with circuit and fabrication process solutions.

This special day brings together key actors from system, architecture, circuit and fabrication technologies to explore strategies for high-performance low-power computing.

Sessions listed at http://www.date-conference.com/conference/wednesday-special-day-sessions

5.1 **HOT TOPIC - System Approaches to Energy-Efficiency** - see page 47

6.1 **EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency** - see page 54

7.0 **LUNCH-TIME KEYNOTE: High-Performance Low-Power Computing** - see page 60

7.1 **HOT TOPIC - Many-Core SoC Approaches to Energy-Efficiency** - see page 60

8.1 **HOT TOPIC - Fabrication Technology Approaches to Energy-Efficiency** - see page 68

Organiser:
Enrico Macii, Politecnico di Torino, IT

Electronic Technologies for Smart Cities

Information and communication technologies, and in particular electronic technologies are the key enablers of the concept of smart city. Research and development activities on different components of a smart city are proliferating, and so are the funding initiatives at the national and international levels.

This Special Day features several technical sessions addressing different aspects of a smart city, ranging from Smart Grid and Buildings to Smart Data Centers, from Smart Health to Smart Mobility. The presentation of the most recent advances in the field of electronic solutions for smart cities is paired by a panel discussion on what are the implications in terms of research directions and policies that the broad theme of smart city can have on the electronic design community.

Sessions listed at http://www.date-conference.com/conference/thursday-special-day-sessions

9.1 **HOT TOPIC: Smart Grid and Buildings - see page 74**

10.1 **HOT TOPIC: Smart Data Centers Design and Optimisation - see page 82**

11.0 **LUNCH-TIME KEYNOTE: Electronic Technologies for Smart Cities - see page 88**

11.1 **HOT TOPIC: Smart Health - see page 88**

12.1 **SPECIAL DAY 2 - HOT TOPIC: Internet of Energy – Connecting Smart Mobility in the Cloud - see page 96**

Special Sessions Chair:
Nicola Nicolici, McMaster University, CA
Zebo Peng, Linköping University, SE

The following 15 Special Sessions have been organised, which should prove to be of great general interest. **Panel Sessions** provide a forum in which motivated opinions on a controversial issue are discussed. The 'trend setters' are given a time-slot to present their views, which are then subjected to critical appraisal from the audience. **Hot Topic** sessions give technical information about emerging new topics and provide a good overview and technical insight. Presenters are leading experts in the field. They present their view on the relevant issues and their importance for research and development. **Embedded Tutorials** give an insight of relevant topics usually starting from an introductory base.

2.6 HOT TOPIC: Reliability Challenges of Real-time Systems in Forthcoming Technology Nodes
Organisers: Said Hamdioui - Delft University of Technology, NL
Dimitris Gizopoulos - University of Athens, GR

2.8 HOT TOPIC: IP Subsystems: The next productivity wave?
Organisers: Wido Kruijtzer - Synopsys, NL
Luciano Lavagno - Politecnico di Torino, IT

3.2 PANEL: The Heritage of Mead & Conway: What Has Remained the Same, What Was Missed, What Has Changed, What Lies Ahead
Organiser: Marco Casale-Rossi - Synopsys, US

3.8 HOT TOPIC: Design for Variability, Manufacturability, Reliability, and Debug: Many Faces of the Same Coin?
Organiser: Vikas Chandra - ARM, US

4.3 EMBEDDED TUTORIAL: Reliability Analysis Reloaded: How Will We Survive?
Organisers: Goerschwin Fey - University of Bremen, DE
Matteo Sonza Reorda - Politecnico di Torino, IT

4.7 HOT TOPIC: Security Challenges in Automotive Hardware/Software Architecture Design
Organiser: Samarjit Chakraborty - TU Munich, DE

5.2 PANEL: Can Energy Harvesting Deliver Enough Power for Automotive Electronics?
Organisers: Tom Kazmierski - University of Southampton, UK
Christoph Grimm - TU Kaiserslautern, DE

6.2 HOT TOPIC: Emerging Nanoscale Devices: A Booster for High Performance Computing
Organisers: Pierre-Emmanuel Gaillardon - EPFL, CH
Giovanni De Micheli - EPFL, CH

6.6 HOT TOPIC: Energy-Efficient Design and Test Techniques for Future Multi-Core Systems
Organiser: Krishnendu Chakrabarty - Duke University, US

7.7 EMBEDDED TUTORIAL: From multi-core SoC to scale-out processors
Organiser: Marcello Coppola – ST Microelectronics, FR

8.8 HOT TOPIC: Countering Counterfeit Attacks on Micro-Electronics
Organisers: Erik Jan Marinissen - IMEC, BE
Ingrid Verbauwhede - KU Leuven, BE

10.2 EMBEDDED TUTORIAL: On the use of GP-GPUs for accelerating computing intensive EDA applications
Organiser: Franco Fummi - University of Verona, IT

10.8 PANEL: Will 3D-IC Remain a Technology of the Future... Even in the Future?
Organiser: Marco Casale-Rossi - Synopsys, US

11.8 EMBEDDED TUTORIAL: Advances in Asynchronous logic: from principles to GALS & NoC, recent industry applications, and commercial CAD tools
Organiser: Pascal Vivet - CEA-LETI, FR

12.8 EMBEDDED TUTORIAL: Closed-Loop Control for Power and Thermal Management in Multi-core Processors: Formal Methods and Industrial Practice
Organiser: Ibrahim Elfadel - Masdar Institute of Science and Technology, AE

MONDAY

Educational Tutorials
Welcome Reception

TUESDAY

Technical Conference and Exhibition Day 1
Vendor Exhibition
Exhibition Theatre
Opening Plenary, Awards and Keynote Addresses
Executive Sessions
Evening Reception sponsored by the City of Grenoble

WEDNESDAY

Technical Conference and Exhibition Day 2
Vendor Exhibition
Exhibition Theatre
Special Day 1: High-Performance Low-Power Computing
DATE Party

THURSDAY

Technical Conference and Exhibition Day 3
Vendor Exhibition
Exhibition Theatre
Special Day 2: Electronic Technologies for Smart Cities

FRIDAY

Special Interest Workshops

CONTACTS

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Exhibitor and Exhibition Enquiries
Email: exhibition-management@date-conference.com

0730	TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS				
BREAKS	1100-1130 Morning, 1300-1430 Lunch, 1600-1630 Afternoon.				
0930 to 1800	A (Room - Belle-Etoile)	B (Room – Les Bans)	C (Room – Chartreuse)	F (Room – Stendhal)	G (Room – Bayard)
	Design Automation Of Electronic Systems: Past Accomplishments And Challenges Ahead - A Tribute To Robert Brayton	Advanced Techniques For Power-Aware System-Level Prototyping	E-Health: Systems, Components, Technologies	Post-Silicon Validation: Old Challenges and New Solutions	Design Methodologies For Adaptive Circuits And Systems
0930 to 1300	D1 (Room – Meije 2)	E1 (Room – Meije 3)	H1 (Room – 7 Laux 4)		
	Digital Microfluidic Biochips: Towards Hardware/Software Co-Design And Cyberphysical System Integration	Assertion Based Verification: A Common Verification Infrastructure For Soc And Embedded Software	Mixed-Signal Dft & Bist: Trends, Principles, And Solutions		
1430 to 1800	D2 (Room – Meije 2)	E2 (Room – Meije 3)	H2 (Room – 7 Laux 4)		
	Hardware Security And Trust	Design And Verification Of Embedded Systems From Natural Language Descriptions	Beyond Dft: The Convergence Of Dfm, Variability, Yield, Diagnosis And Reliability		
1800	Welcome Reception				

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1030-1130 Exhibition Break, 1300-1430 Lunch, 1600-1700 Exhibition Break (1600-1630 IP1)
0830	1.1 PLENARY: OPENING, AWARDS PRESENTATION AND KEYNOTE ADDRESSES, Auditorium Dauphine		

	SPECIAL TRACK	DESIGN	DESIGN	DESIGN	APPLICATIONS	TEST & RELIABILITY	EMBEDDED SOFTWARE	EXHIBITION THEATRE
1130 to 1300	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdiguieres
	2.1 EXECUTIVE SESSION - Advanced Technology Nodes: Dependency on Collaboration	2.2 Acceleration and Verification of ESL and Analog Systems	2.3 Energy Optimization in Multi-core Systems	2.4 Memory and Cache Architectures	2.5 Communications, Multimedia, and Consumer Electronics	2.6 HOT TOPIC: Reliability Challenges of Real-time Systems in Forthcoming Technology Nodes	2.7 Safety Critical Real-Time Systems	2.8 HOT TOPIC: IP Subsystems: The next productivity wave?
1300	1300-1400, Auditorium Dauphine: 3.0 Special Lunch-Time Session: Grenoble Ecosystem to Provide Semiconductor Alternative Process for Advanced CMOS							
1430 to 1600	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdiguieres
	3.1 EXECUTIVE SESSION - The Role of Prototyping in Today's SOCs	3.2 PANEL: The Heritage of Mead & Conway	3.3 Addressing Process and Delay Variation in High-Level Synthesis	3.4 Microarchitectural Techniques for Reliability	3.5 Energy Efficient Mobile and Cloud Computing Systems	3.6 Dealing with Timing Variation in Advanced Technologies	3.7 Timing Analysis	3.8 HOT TOPIC: Design for Variability, Manufacturability, Reliability, and Debug
1700 to 1830	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdiguieres
	4.1 EXECUTIVE SESSION - Is reusing off-the-shelf Semiconductor IP possible today?	4.2 The Quest for Better NoCs	4.3 EMBEDDED TUTORIAL: Reliability Analysis Reloaded: How Will We Survive?	4.4 Emerging Solutions to Manage Energy/Performance Trad-Offs Along the Memory Hierarchy	4.5 Device Identification and Protection	4.6 New Techniques for Test Pattern Generation	4.7 HOT TOPIC: Security Challenges in Automotive Hardware/Software Architecture Design	4.8 EXHIBITION THEATRE: Testimonials
1830	Evening Reception sponsored by the IEEE Council on EDA							

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP2), 1230-1340 Lunch, 1600-1700 Exhibition Break (1600-1630 IP3)					
	SPECIAL TRACK	DESIGN	DESIGN	DESIGN	APPLICATIONS	TEST & RELIABILITY	EMBEDDED SOFTWARE	EXHIBITION THEATRE
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigieres
0830 to 1000	5.1 SPECIAL DAY 1 HOT TOPIC - System Approaches to Energy-Efficiency	5.2 PANEL - Can Energy Harvesting Deliver Enough Power for Automotive Electronics?	5.3 Post-Silicon Debug Techniques	5.4 Novel Approaches for Real-Time Architectures	5.5 Error-Aware Adaptive Modern Computing Architectures	5.6 Advances in Mixed-Signal, RF, and MEMS testing	5.7 Compilers and Software Synthesis for Embedded Systems	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigieres
1100 to 1230	6.1 SPECIAL DAY 1 - EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency	6.2 HOT TOPIC - Emerging Nanoscale Devices: A Booster for High Performance Computing	6.3 Verification and Simulation Support for Architecture	6.4 Design Space Exploration for Application Specific Architectures	6.5 Reliable Multi-Processor Computing Systems Design	6.6 HOT TOPIC - Energy-Efficient Design and Test Techniques for Future Multi-Core Systems	6.7 Model-Based Design and Verification for Embedded Systems	6. 8 EXHIBITION THEATRE: Silicon Europe – Leading European Regions Join Forces
1300	1330-1400, Room Oisans: 7.0 Special Day 1 Lunch-Time Keynote: Energy-Efficient Computing							
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigieres
1430 to 1600	7.1 SPECIAL DAY 1 HOT TOPIC - Many-Core SoC Approaches to Energy-Efficiency	7.2 Formal Verification Algorithms and Models	7.3 Dynamic Reconfiguration	7.4 Emerging Memory	7.5 Energy-efficient architectures and software design for power-constrained systems	7.6 On-Line Approaches Towards Processor Resilience	7.7 SPECIAL SESSION EMBEDDED TUTORIAL: From multi-core SoC to scale-out processors	
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigieres
1700 to 1830	8.1 SPECIAL DAY 1 HOT TOPIC - Fabrication Technology Approaches to Energy-Efficiency	8.2 Scheduling for Real-Time Embedded Systems	8.3 Logic Synthesis Techniques	8.4 High-Speed Robust NoCs	8.5 Industrial Experiences with Embedded System Design	8.6 DfT Methods	8.7 Monitoring and Control of Cyber Physical Systems	8.8 HOT TOPIC: Countering Counterfeit Attacks on Micro-Electronics

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP4), 1230-1400 Lunch, 1530-1600 Break (1530-1600 IP5)					
	SPECIAL TRACK	DESIGN	DESIGN	DESIGN	DESIGN	TEST & RELIABILITY	EMBEDDED SOFTWARE	EXHIBITION THEATRE
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
0830 to 1000	9.1 SPECIAL DAY 2 - HOT TOPIC: Smart Grid and Buildings	9.2 System-Level Analysis and Simulation	9.3 Thermal/Power Management Techniques for Energy-Efficient Systems	9.4 Emerging Architectures	9.5 Manufacturing and Design Security	9.6 Improving IC Quality and Lifetime Though Advanced Characterisation	9.7 Design and Scheduling	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1100 to 1230	10.1 SPECIAL DAY 2 - HOT TOPIC: Smart Data Centers Design and Optimisation	10.2 EMBEDDED TUTORIAL: On the use of GP-GPUs for accelerating computing intensive EDA applications	10.3 Thermal Analysis and Power Optimisation Techniques	10.4 Abstraction Techniques and SAT/SMT-Based Optimisations	10.5 Design and Verification of Mixed-Signal Circuits	10.6 On-Line Testing Techniques	10.7 Embedded Software for Many-Core Architectures	10.8 PANEL: Will 3D-IC Remain a Technology of the Future... Even in the Future?
1330	1330-1400, Room Oisans: 11.0 Special Day 2 Lunch-Time Keynote: SMART CITIES AND COMMUNITIES AT THE REGIONAL, NATIONAL AND EUROPEAN LEVELS							
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1400 to 1530	11.1 SPECIAL DAY 2 - HOT TOPIC: Smart Health	11.2 High-Level Synthesis and Coarse-Grained Reconfigurable Architectures	11.3 Efficient NoC Routing Mechanisms	11.4 System-Level Modelling for Physical Properties	11.5 Energy Challenges for Multi-Core and NoC Architectures	11.6 Modelling and Design for Signal and Power Integrity	11.7 Powerful Aging	11.8 EMBEDDED TUTORIAL: Advances in Asynchronous logic
	Room – Oisans	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room - Meije	Room – Bayard	Room – Les Bans	Room - Lesdigiueres
1600 to 1730	12.1 SPECIAL DAY 2 - HOT TOPIC: Internet of Energy – Connecting Smart Mobility in the Cloud	12.2 Methodologies to Improve Yield, Reliability and Security in Embedded Systems	12.3 NoC Mapping and Synthesis	12.4 Emerging Logic	12.5 Emerging Technology Architectures for Energy-Efficient Memories	12.6 Clock Distribution and Analogue Circuit Synthesis	12.7 Physical Design	12.8 EMBEDDED TUTORIAL: Closed-Loop Control for Power and Thermal Management

0730	WORKSHOP REGISTRATION & WELCOME REFRESHMENTS
BREAKS	Please see individual workshop programmes for lunch and break times

0830 TO 1700	Room – Meije 2	Room – Stendhal	Room – Oisans	Room – Chartreuse	Room – Bayard
	W1 ESCUG 2013: ESL - Putting the Pieces Together: Integrating SystemC Design and Verification with AMS and Algorithm Design	W2 1st RIIF Workshop - Towards Standards for Specifying and Modeling the Reliability of Complex Electronic Systems	W3 International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2013)	W4 Platform 2012 / STHORM embedded many-core acceleration	W5 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test

0830 TO 1700	Room – Berlioz	Room – Les Bans	Room – Belle-Etoile	Room – Meije 3	
	W6 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications	W7 Reconfigurable Computing V2.0: The Next Generation of Technology, Architectures and Design Tools	W8 Workshop on Industry-Driven Approaches for Cost-effective Certification of Safety-Critical, Mixed-Criticality Systems (WICERT)	W9 International Workshop on Software Approaches to Resilient System Design	

Organiser: Franco Fummi, Verona U, IT

Eleven pre-conference tutorials will be given on Monday. Five are full-day tutorials (A, B, C, F and G). Six are half-day tutorials, three to be given in the morning (D1, E1, and H1) and three in the afternoon (D2, E2, and H2). A participant should enroll for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.

The titles, organisers, speakers, and abstracts of the tutorials are given below:

0930 **FULL-DAY TUTORIALS – A, B, C, F and G**

A **(Room - Belle-Etoile)**

DESIGN AUTOMATION OF ELECTRONIC SYSTEMS: PAST ACCOMPLISHMENTS AND CHALLENGES AHEAD - A TRIBUTE TO ROBERT BRAYTON

Organiser: **Tiziano Villa,** Università di Verona, IT

Speakers:
Jacob White, MIT, US
Jaijeet Roychowdhury, University of California at Berkeley, US
Masahiro Fujita, University of Tokyo, JP
Jordi Cortadella, Universitat Politecnica de Catalunya, ES
Victor Kravets, IBM, US
Rajeev Murgai, Synopsys, IN
Igor Markov, University of Michigan, US
Ken McMillan, Microsoft, US
Sanjit Seshia, University of California at Berkeley, US
Giovanni De Micheli, Ecole Polyt. de Lausanne, CH
Douglas Densmore, Boston University, US
Rupak Majumdar, University of California at LA, US
Alexandre Petrenko, CRIM, CA
Luca Carloni, Columbia University, US
Alberto Sangiovanni-Vincentelli, University of California at Berkeley, US
Robert Brayton, University of California at Berkeley, US

This tutorial brings together world-wide experts in Computer-Aided Design of Electronics Systems to assess past successes and present challenges in electronic design automation (EDA). This event will celebrate the scientific contributions of Prof. Robert Brayton who has been since many decades a major driving force for all fields of EDA in industrial and academic research. Prof. Brayton, who is still an active researcher at UC Berkeley, will turn eighty in 2013. The tutorial will be a unique opportunity for the EDA community to get a perspective on the major directions of development, past and future.

B **(Room - Les Bans)**

ADVANCED TECHNIQUES FOR POWER-AWARE SYSTEM-LEVEL PROTOTYPING

Organiser: **Frank Oppenheimer,** OFFIS, DE
Eugenio Villar, Universidad de Cantabria, ES
Adam Morawiec, ECSI, FR
Philipp A. Hartmann, OFFIS, DE

Speakers: **Eugenio Villar,** Universidad de Cantabria, ES
Davide Quaglia, EDALab, IT
Emmanuel Vaumorin, Magillem, FR
Francisco Ferrero, GMV AD, ES
Carlo Brandolese, Politecnico di Milano, IT
Philipp A. Hartmann, OFFIS, DE
Sara Bocchio, STMicroelectronics, IT

In the design of embedded systems extra-functional properties like timing and power need to be considered during the entire design process. Often these properties can only be estimated after manually implementing a design for a certain target platform and using component-level timing and power analysis tools. At the same time, exploration, analysis, and optimization of embedded applications running on today's platforms require fast and early virtual system models enabling the consideration of extra-functional properties under real-world application scenarios.

With a group of experts from industry and academia, the tutorial discusses the major challenges and presents novel and innovative research results including tool support to create timing and power-aware Virtual Platforms. In this context, the following key aspects are covered:

- Model-driven design and automatic platform performance and power model synthesis, enabling early design space exploration,
- efficient application mapping onto resource-constrained platform models,
- early and automatic timing and power estimation for embedded software and custom hardware components, suitable for integration into Virtual Platform models,
- RTL-to-TLM re-synthesis and abstraction of timing and power properties, suitable for integration into Virtual Platform models

The presentations will be accompanied by concrete tool introductions and demonstrations, showing how the presented concepts support improvement of today's state-of-the-art system-level design flows.

C **(Room - Chartreuse)**

E-HEALTH: SYSTEMS, COMPONENTS, TECHNOLOGIES

Organiser: **Giovanni De Micheli,**
EPFL, CH

Speakers:
Rudy Lauwereins, IMEC, BE
Giovanni De Micheli, EPFL, CH
Carlotta Guiducci, EPFL, CH
Benedetto Vigna, STMicroelectronics, IT
Sven Ingebrandt, University of Kaiserslautern, DE
Wayne Burleson, University of Massachusetts, US

There is a rapid growth of the electro-medical sector and a shortage of engineers and designers who can seize this opportunity. As mass production of standard electronic components is shifting to Asia, it is important for the European Industries and Universities to explore alternative use of silicon. Indeed, the use of silicon interfaces to living matter opens unforeseeable horizons and markets. New electronic systems for diagnostics and care are changing the practice of health management, opening the door to personalized medicine as well as to support for remote care of chronic patients.

This tutorial starts with a survey of the field and the motivations to develop biomedical electronic system. It will be followed by a survey of biosensing methods, for both diagnostics and implants in humans. Whereas the first two presentations will cover system and methodological aspects, the following two will focus on technology, and in particular on silicon technologies for sensing and on biosensor design. The final presentation will return to system aspects with a presentation of security features as a key design problem.

F **(Room - Stendhal)**

POST-SILICON VALIDATION: OLD CHALLENGES AND NEW SOLUTIONS

Organisers: **Valeria Bertacco,** University of Michigan, US
Amir Nahir, IBM, IL

Speakers: **Rand Gray,** Intel Corp, US
Valeria Bertacco, University of Michigan, US
Sharad Malik, Princeton University, US
Wisam Kadry, IBM, IL

Taking complex designs, such as microprocessors, from design to manufacturing requires both pre-silicon and post-silicon validation efforts. Because modern designs are extremely complex, pre-silicon verification methods are no longer sufficient to guarantee a correct design. Therefore, a growing portion of the verification effort is shifting to the post-silicon phase, after the first few silicon prototypes become available. While post-silicon validation benefits from extremely high execution performance compared to pre-silicon simulation, major challenges are posed by the limited controllability and observability of internal circuit nodes, as well as the very long error traces generated. Increasing amounts of functionality and IP components integrated into a single chip exacerbate these issues significantly.

Compounding these issues are the ever-increasing speeds of high speed system level signaling schemes, which, in turn, drive up analog circuit complexity in silicon. Moreover, memory subsystem architecture continues to increase in complexity to keep up with power and performance targets.

This tutorial will provide an overview of the validation challenges that are specific to the post-silicon domain. It will then discuss strategies and methods used in the industry to expose, locate and debug the different classes of silicon bugs (functional, electrical and manufacturing errors). The discussion will also reference specific experiences and design case studies to which the techniques presented have been applied. We will also provide a forward-looking perspective regarding emerging solutions in silicon debug, based on recent academic research. The discussion will focus primarily on the post-silicon validation of complex processors, since this is a market segment where post-silicon validation is widely deployed; however, many of the solutions are suitable for digital designs in general.

G **(Room - Bayard)**

DESIGN METHODOLOGIES FOR ADAPTIVE CIRCUITS AND SYSTEMS

Organiser: **Saibal Mukhopadhyay,**
Georgia Institute of Technology, US

Speakers:
Saibal Mukhopadhyay, Georgia Institute of Technology, US
Abhijit Chatterjee, Georgia Institute of Technology, US
Sudhakar Yalamanchili, Georgia Institute of Technology, US
Arijit Raychowdhury, Georgia Institute of Technology, US

CMOS technology scaling along with the resulting large variability of circuit performance metrics in the presence of manufacturing process variations has made post-silicon and dynamic adaptation/tuning almost a necessity for nanometer scale silicon technologies. Currently, circuits and systems are designed to tolerate worst-case process corners and worst case operating conditions (e.g. worst case voltage and temperature conditions). The traditional design approach of excessively guard-banding the products results in unacceptable power-performance-yield tradeoffs as technology moves to 10nm nodes. The preceding challenge has led to significant research and development in designing circuits that are "self-aware" and can adapt to process (static) and environmental (dynamic) variations to minimize guard-banding and hence reduce power while maintaining desired yield and reliability. Such self-awareness involves incorporation of on-chip and on-line characterization static/dynamic variations using sensors and/or built-in test/diagnosis and performing on-line tuning/adaptation. The adaptation methodologies are different at the circuit and system levels. Likewise the digital and mixed-signal systems have different challenges for adaptation. This tutorial will provide a broad perspective of the emerging trend of adaptive circuits and systems for next generation electronics; summarize recent results obtained in this area; and points to directions for future work. First, the tutorial will discuss the circuit level techniques for adaptations including on-chip sensors. The advancements in the adaptive logic and memory circuits will be presented. Next, the tutorial will discuss the challenges in designing adaptive digital systems focusing on the architecture level adaptation. Special emphasis will be given in illustrating the need for innovative modeling and simulation methodologies required to design adaptive architectures. Finally, the tutorial will summarize recent results obtained in the design of self-aware wireless communications systems to illustrate the challenges and methodologies for adaptive mixed-signal systems.

A full-day tutorial is proposed to cover the different aspects of adaptive systems spanning different levels of design abstractions – from circuits to micro-architecture, and different types of circuits – logic, memory, and RF subsystems. The coverage of all these various aspects in a single tutorial will provide the audience a broad perspectives of the very important topic of adaptive systems.

0930 HALF-DAY TUTORIALS – D1, E1, H1

D1 (Room - Meije 2)

DIGITAL MICROFLUIDIC BIOCHIPS: TOWARDS HARDWARE/SOFTWARE CO-DESIGN AND CYBERPHYSICAL SYSTEM INTEGRATION

Organiser: **Krishnendu Chakrabarty,** Duke University, US

Speakers: **Tsung-Yi Ho,** National Cheng Kung Univ., TW
Krishnendu Chakrabarty, Duke University, US

This tutorial will first provide an overview of typical biomolecular applications (market drivers) such as immunoassays, DNA sequencing, clinical chemistry, etc. Next, microarrays and various microfluidic platforms will be discussed.

The second part of the tutorial will focus on electrowetting-based digital microfludic biochips. The key idea here is to manipulate liquids as discrete droplets. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial. Basic concepts in microfabrication techniques will also be discussed.

Attendees will next learn about CAD, design-for-testability, and reconfiguration aspects of digital microfluidic biochips. Synthesis tools will be described to map assay protocols from the lab bench to a droplet-based microfluidic platform and generate an optimized schedule of bioassay operations, the binding of assay operations to functional units, and the layout and droplet-flow paths for the biochip. The role of the digital microfluidic platform as a "programmable and reconfigurable processor" for biochemical applications will be highlighted. Sensor integration, and cyberphysical integration using low-cost sensors and adaptive control software will be highlighted. Reconfiguration techniques will be presented to easily bypass faults once they are detected. The problem of mapping a small number of chip pins to a large number of array electrodes will also be covered. With the availability of these tools, chip users and chip designers will be able to concentrate on the development and chip-level adaptation of nano-scale bioassays (higher productivity), leaving implementation details to CAD tools.

Earlier offerings of this (and similar) tutorials covered technology aspects, initial work on CAD algorithms and test solutions. This tutorial will, for the first time, include sensor integration, cyberphysical adaptation and hardware/software co-design for biochemistry-on-a-chip, error recovery, and dynamic reconfiguration.

E1 (Room - Meije 3)

ASSERTION BASED VERIFICATION: A COMMON VERIFICATION INFRASTRUCTURE FOR SOC AND EMBEDDED SOFTWARE

Organiser: **Masahiro Fujita,** University of Tokyo, JP
Graziano Pravadelli, Università di Verona, IT

Speakers: **Giuseppe Di Guglielmo,** Columbia University, US
Masahiro Fujita, University of Tokyo, JP
Cristina Marconcini, STM Product, IT
Graziano Pravadelli, Università di Verona, IT

Model driven design and virtual prototyping are pushing more and more towards the convergence between HW design and embedded SW development. However, the adoption of HW/SW unrelated verification approaches tends to increase both the verification time and the risk of bug escaping at the HW/SW frontier. In this context, assertion-based verification (ABV) is a promising approach for SoC as well as of embedded software. However, some practical aspects still prevent industries from definitely including ABV in their design process. Among the most relevant issues we can cite: (i) the difficulty of writing a complete and signification set of assertions, which really reflects the intent described in the test plan, and (ii) the lack of a design methodology for embedded SW development and FPGA prototyping, which easily enables dynamic ABV. For these reasons someone thinks ABV requires a too strong formal background to writing assertions, while others believe ABV mandatory needs the use of formal tools that cannot easily handle neither large SoC descriptions, nor complex embedded SW implementations. This half-day tutorial is intended to controvert such beliefs.

The first part introduces ABV and, particularly, the Property Specification Language for assertion definition.

The second part deals with basic and advanced ABV methods based on static and dynamic analysis targeting HW designs including SoC. This covers automatic generation of assertions from simulation results, as it is crucial to have sufficient sets of assertions for more complete verification. Automatic generation can provide assertions escaping manual definition. Both algorithmic as well as empirical results are shown. This part also discusses how to check the completeness of the assertions prepared for a particular design.

The third part describes dynamic ABV methods for embedded SW. Although both static and dynamic ABV methods are widely adopted for HW, software parts are traditionally verified by means of static ABV. This is because dynamic approaches need simulation assumptions that could not be true during execution of general embedded software and also cannot be controlled by the assertion language. Here, dynamic ABV methods, which exploit model-driven designs for guaranteeing such simulation assumptions, are introduced. These techniques can also be applied to post-silicon verification and debugging for SoC.

Finally, the tutorial will be concluded by showing how ABV-based tools can be profitably used to accomplish verification process requirements, like, for example, those described in the IEC 60730 safety standard for automatic electronic controls used in household appliances.

H1 **(Room - 7 Laux 4)**

MIXED-SIGNAL DFT & BIST: TRENDS, PRINCIPLES, AND SOLUTIONS

Organisers: **Yiorgos Makris,** University of Texas at Dallas, US
Dimitris Gizopoulos, University of Athens, GR

Speaker: **Stephen Sunter,** Mentor Graphics, US

We start by briefly looking at trends in process, design, and analogue/mixed-signal testing, then in more detail at trends in ad hoc design-for-test (DfT) and analogue defect simulation. We then review standardized DFT suitable for mixed-signal circuits, including IEEE 1149.1, .4, .6, .8, and 1687. The trend analysis concludes with an analysis of BIST techniques, especially for ADC/DAC, but also for

PLL, SerDes, DDR, and miscellaneous analogue. Next, seven essential principles of practical analogue BIST are discussed, ranging from testing the BIST itself, and adding for precision, to subtracting for accuracy, and generating a digital result. Lastly, we discuss the most practical techniques to use in new DfT and BIST circuitry, ranging from the classic analogue test bus, to mostly-digital oversampling and undersampling circuits that improve measurement range, resolution, and reusability, to ultimately optimize quality and cost of test.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2013

1430 **HALF-DAY TUTORIALS – D2, E2, H2**

D2 **(Room - Meije 2)**

HARDWARE SECURITY AND TRUST

Organiser: **Ramesh Karri,** New York University, US

Speakers:
Ramesh Karri, New York University, US
Miodrag Potkonjak, University of California at LA, US
Ozgur Sinanoglu, New York University, US

Hardware security and trust is an important design objective similar to power, performance, reliability and testability. We will highlight why hardware security and trust are important objectives from the economics, security, and safety perspectives. We will highlight various attacks and countermeasure, hardware based security primitives, security vs reliability vs quality trade-offs.

Globalization of Integrated Circuit (IC) design is making designers and users of IC and Intellectual Property (IP) re-assess their trust in hardware. As the IC design flow spans the globe -driven by cost-conscious consumer electronics- hardware is increasingly prone to side channel analysis, reverse engineering, IP piracy and malicious modifications (i.e. hardware trojans). An attacker, anywhere within the global, horizontal design flow, can reverse engineer the functionality of an IC/IP, steal and claim ownership of the IP or introduce counterfeits into the supply chain. Moreover, an untrusted IC fab may overbuild ICs and sell them illegally. Finally, rogue elements in the fabs may insert hardware trojans into the design without the knowledge of the designer or the end-user of the IC; this additional functionality may subsequently be exploited to introduce errors in the results, steal sensitive information or incapacitate a fielded system. The semiconductor industry routinely loses over $4 billion annually due to these attacks. In this tutorial we will introduce this important, emerging area of Design, Test and EDA.

E2 **(Room - Meije 3)**

DESIGN AND VERIFICATION OF EMBEDDED SYSTEMS FROM NATURAL LANGUAGE DESCRIPTIONS

Organiser: **Robert Wille,** University of Bremen, DE

Speakers: **Rolf Drechsler,** DFKI GmbH, DE
Wolfgang Ecker, Infineon Technologies, DE
Rainer Findenig, Intel Mobile Communications, AT
Ian G. Harris, University of California Irvine, US
Robert Wille, University of Bremen, DE

At the same time, designers are constantly striving for higher levels of abstraction. After the gate level, the Register Transfer Level (ESL), and the Electronic System Level (ESL), researchers are increasingly considering the formal specification level. Modeling languages such as the Unified Modeling Language (UML) or the System Modeling Language (SysML) provide proper syntax and semantic for this purpose. They allow for a formal specification of the structure and the behavior of a system while, at the same time, hiding precise implementation details. Using these formal descriptions, crucial design flaws can already be detected at the specification level and, thus, before any line of code is written. Besides that, they provide a formal input for automatic code generation techniques.

Both developments build the basis to narrow the gap between the (natural language) specification as well as its actual implementation and, at the same time, allow for a verification-driven design flow. This tutorial will provide an overview on this progress and outline the challenges and opportunities resulting from these developments. We show how NLP and modeling languages build the basis for a new design flow, which incorporates automation from the beginning to the initial code generation.

H2 **(Room - 7 Laux 4)**

BEYOND DFT: THE CONVERGENCE OF DFM, VARIABILITY, YIELD, DIAGNOSIS AND RELIABILITY

Organiser: **Yiorgos Makris,** University of Texas at Dallas, US
Dimitris Gizopoulos, University of Athens, GR

Speaker: **Rob Aitken,** ARM, US

The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. As feature sizes reduced to 90 nm and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of test-limited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2013

Tutorials

MONDAY 18 MARCH, 2013

0730 **TUTORIAL REGISTRATION**

0800 **Tutorial Welcome Refreshments**

0930-1800

A	(Room – Belle-Etoile)	**Design Automation Of Electronic Systems: Past Accomplishments And Challenges Ahead - A Tribute To Robert Brayton**
B	(Room – Les Bans)	**Advanced Techniques For Power-Aware System-Level Prototyping**
C	(Room – Chartreuse)	**E-Health: Systems, Components, Technologies**
F	(Room – Stendhal)	**Post-Silicon Validation: Old Challenges And New Solutions**
G	(Room – Bayard)	**Design Methodologies For Adaptive Circuits And Systems**

0930

D1	(Room – Meije 2)	**Digital Microfluidic Biochips: Towards Hardware/ Software Co-Design And Cyberphysical System Integration**
E1	(Room – Meije 3)	**Assertion Based Verification: A Common Verification Infrastructure For Soc And Embedded Software**
H1	(Room – 7 Laux 4)	**Mixed-Signal DfT & BIST: Trends, Principles, And Solutions**

1430

D2	(Room – Meije 2)	**Hardware Security And Trust**
E2	(Room – Meije 3)	**Design And Verification Of Embedded Systems From Natural Language Descriptions**
H2	(Room – 7 Laux 4)	**Beyond Dft: The Convergence Of Dfm, Variability, Yield, Diagnosis And Reliability**

Tutorial attendees should choose in advance one tutorial from D1, E1, or H1, which take place in the morning, and/or one tutorial from D2, E2, or H2, which take place in the afternoon. Those wishing to attend one of the full-day tutorials should choose in advance one of A, B, C, F or G. A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.

All tutorials run in parallel in accordance with the timetable below.

Rooms will be signposted.

0730 - 0930	**Registration and Tutorial Welcome Refreshments** (Main Foyer)
0930 – 1100	**Tutorials**
1100 – 1130	**Break**
1130 – 1300	**Tutorials**
1300 – 1430	**Lunch Break**
1330	**CONFERENCE REGISTRATION BEGINS**
1430 – 1600	**Tutorials**
1600 – 1630	**Break**
1630 – 1800	**Tutorials**
1800 – 1930	**WELCOME RECEPTION** (Main Foyer)
1900 – 2100	**FRINGE TECHNICAL MEETINGS**

technical programme

TUESDAY 19 MARCH, 2013

0730 REGISTRATION and SPEAKERS' BREAKFAST

1.1 Plenary: Opening and Keynote

Room - Auditorium Dauphine 0830-1030

Organiser: Enrico Macii - Politecnico di Torino, IT

0830 OPENING REMARKS

Enrico Macii - Politecnico di Torino, IT
Erik Jan Marinissen - IMEC, BE

0900 DATE 2012 BEST PAPER AWARD
Zebo Peng - Linköping University, SE

The DATE 2012 Best Paper Award is given for "Compositional System-Level Design Exploration with Planning of High-Level Synthesis", by Hung-Yi Liu, Michele Petracca, and Luca P. Carloni, Columbia University, US

0902 DATE 2013 BEST PAPER AWARD
Giovanni De Micheli - EPFL, CH

0912 PRESENTATION OF DISTINGUISHED AWARDS

0920 SMART SYSTEMS FOR INTERNET OF THINGS
Benedetto Vigna - STMicroelectronics, IT

Sensors add intelligence to systems which represent a broad class of devices incorporating functionalities like sensing, actuation, and control. They are the core of smart components and subsystems; then, the challenge in the realization of such smart systems goes beyond the design of the individual components and subsystems and consists of accommodating a multitude of functionalities, technologies, and materials to play a key role to augment our daily life.

0955 CREATING A SUSTAINABLE INFORMATION AND COMMUNICATION INFRASTRUCTURE
Massoud Pedram - University of Southern California, US

Modern society's dependence on information and communication infrastructure (ICI) is so deeply entrenched that it should be treated on par with other critical lifelines of our existence, such as water and electricity. As is the case with any true lifeline, ICI must be reliable, affordable, and sustainable. Meeting these requirements (especially sustainability) is a continued critical challenge, which will be the focus of my talk. More precisely, I will provide an overview of information and communication technology trends in light of various societal and environmental mandates followed by a review of technologies, systems, and hardware/software solutions required to create a sustainable ICI.

1030 EXHIBITION BREAK

SESSIONS technical sessions

2.1 EXECUTIVE SESSION - Advanced Technology Nodes: Dependency on Collaboration

Room - Oisans 1130-1300

Organiser: **Yervant Zorian,** Synopsys, US

Chair: **Yervant Zorian,** Synopsys, US

Executives:
Maria Marced, President, TSMC Europe, NL
Navid Shervani, President, CoFounder & CEO - Open Silicon, US
Juan Rey, Senior Director, Mentor Graphics, US
Raj Yavatkar, Fellow, Intel, US

Abstract: The continuous technology scaling and new multi-die solutions are dramatically impacting the business performance of semiconductor industry. This may also significantly affect the dependency between eco-system players necessitating stronger collaboration and interdependency between them. The executives in this session will discuss upcoming changes in the semiconductor industry and their impact on collaboration between the foundries, design service and IP providers, EDA companies, and the rest of the value chain.

2.2 Acceleration and Verification of ESL and Analog Systems

Room - Belle-Etoile 1130-1300

Chair: **Alper Sen,** Bogazici University, TR
Co-Chair: **Daniel Grosse,** University of Bremen, DE

The session is centered around parallelization and verification of electronic designs during simulation. The first paper introduces an optimization technique for out-of-order parallel discrete event simulation of ESL designs using static analysis of potential hazards at compile time. The second paper describes a new way of parallelizing loosely-timed SystemC models using primitives that can explicitly capture durations for tasks. The third paper presents trade-offs estimation of fixed-point errors on linear time-invariant systems by combining advantages of statistical and analytical techniques. The final paper proposes a run-time algorithm to verify design properties of non-linear analogue circuits using efficient data structures.

1130 **OPTIMIZED OUT-OF-ORDER PARALLEL DISCRETE EVENT SIMULATION USING PREDICTIONS**
Weiwei Chen and Rainer Doemer
University of California, Irvine, US

1200 **PARALLEL PROGRAMMING WITH SYSTEMC FOR LOOSELY TIMED MODELS: A NON-INTRUSIVE APPROACH SYSTEM-ON-CHIP MULTIPROCESSING**
Matthieu Moy
Grenoble University, FR

1230 **ACCURACY VS SPEED TRADEOFFS IN THE ESTIMATION OF FIXED-POINT ERRORS ON LINEAR TIME-INVARIANT SYSTEMS**
David Novo[1], Sara El Alaoui[2], Paolo Ienne[1]
[1]EPFL, CH, [2]Al Akhawayn University, MA

1245 **RUNTIME VERIFICATION OF NONLINEAR ANALOG CIRCUITS USING INCREMENTAL TIME-AUGMENTED RRT ALGORITHM**
Seyed Nematollah Ahmadyan, Jayanand Asok Kumar and Shobha Vasudevan
University of Illinois at Urbana-Champaign, US

IPs **IP1-1, IP1-2, IP1-3**

1300 **LUNCH BREAK**

2.3 Energy Optimization in Multi-core Systems

Room - Stendhal 1130-1300

Chair: Thidapat Chantem, Utah State University, US
Co-Chair: William Fornaciari, Politecnico di Milano, IT

This session features papers addressing various issues arising in the design of multi-core systems, including process variability, real-time responsiveness, and dynamic user adaptation.

1130 **CHERRY-PICKING: EXPLOITING PROCESS VARIATIONS IN DARK-SILICON HOMOGENEOUS CHIP MULTI-PROCESSORS**
Yatish Turakhia[1], Bharathwaj Raghunathan[2], Siddharth Garg[2], Diana Marculescu[3]
[1]Indian Institute of Technology Bombay, IN
[2]University of Waterloo, CA
[3]Carnegie Mellon University,, CA

1200 **ENERGY OPTIMIZATION WITH WORST-CASE DEADLINE GUARANTEE FOR PIPELINED MULTIPROCESSOR SYSTEMS**
Gang Chen[1], Kai Huang[1], Christian Buckl[2], Alios Knoll[1]
[1]Technical University Munich, DE [2]ForTISS, DE

1230 **SELF-ADAPTIVE HYBRID DYNAMIC POWER MANAGEMENT FOR MANY-CORE SYSTEMS**
Muhammad Shafique, Benjamin Vogel and Jörg Henkel
Karlsruhe Institute of Technology, DE

IPs **IP1-4, IP1-5**

1300 **LUNCH BREAK**

2.4 Memory and Cache Architectures

Room - Chartreuse 1130-1300

Chair: Georgi Gaydadjiev, Chalmers University of Technology, SE
Co-Chair: Todd Austin, Michigan University Ann Arbor, US

This session covers memory architectures to improve energy efficiency, reliability, performance, and access patterns in caches. The first paper proposes a mechanism to overcome sensitivity to access-time variations in L1 cache. The second paper introduces a new memory-addressing method and corresponding coherency protocol to handle two-dimensional memory access patterns. The third paper suggests a hybrid cache architecture composed of a hybrid SRAM and DRAM caches instead of two separate cache levels to reduce inter-core DRAM interferences. The last paper in the session uses a combination of SRAM and eDRAM to build energy-efficient L1 data caches that are resilient to errors when operating at near-threshold voltages.

1130 **AVICA: AN ACCESS-TIME VARIATION INSENSITIVE L1 CACHE ARCHITECTURE**
Seokin Hong and Soontea Kim
Korea Advanced Institute of Science and Technology, KR

1200 **DUAL-ADDRESSING MEMORY ARCHITECTURE FOR TWO-DIMENSIONAL MEMORY ACCESS PATTERNS**
Yen-Hao Chen and Yi-Yu Liu
Yuan Ze University, TW

1230 **ADAPTIVE CACHE MANAGEMENT FOR A COMBINED SRAM AND DRAM CACHE HIERARCHY FOR MULTI-CORES**
Fazal Hameed, Lars Bauer and Jörg Henkel
Karlsruhe Institute of Technology, DE

1245 **COMBINING RAM TECHNOLOGIES FOR HARD-ERROR RECOVERY IN L1 DATA CACHES WORKING AT VERYLOW POWER MODES**
Vicente Lorente[1], Alejandro Valero[1], Julio Sahuquillo[1], Salvador Petit[1], Ramón Canal[2], Pedro López[1], José Duato[1]
[1]Universitat Politècnica de València, ES
[2]Universitat Politècnica de Catalunya, ES

IPs **IP1-6, IP1-7**

1300 **LUNCH BREAK**

2.5 Communications, Multimedia, and Consumer Electronics

Room - Meije 1130-1300

Chair: Theocharis Theocharides, University of Cyprus, CY
Co-Chair: Amer Baghdadi, Telecom Bretagne, FR

This session presents new architectures for digital communications as well as multi-media systems. The session consists of four papers.

The first paper presents a low-complexity QR decomposition architecture, while the second paper presents a new methodology for managing SRAM memories for video applications. The third paper presents a parameterized flexible turbo decoder, and lastly, the fourth paper presents an H.264 intra-video encoder architecture.

1130 **LOW COMPLEXITY QR-DECOMPOSITION ARCHITECTURE USING THE LOGARITHMIC NUMBER SYSTEM**
Jochen Rust, Frank Ludwig and Steffen Paul University of Bremen, DE

1200 **PERCEPTUAL QUALITY PRESERVING SRAM ARCHITECTURE FOR COLOR MOTION PICTURES**
Wen Yueh, Minki Cho and Saibal Mukhopadhyay Georgia Institute of Technology, US

1230 **PARAMETERIZED AREA-EFFICIENT MULTI-STANDARD TURBO DECODER**
Purushotham Murugappa, Amer Baghdadi and Michel Jezequel Telecom Bretagne, FR

1245 **AN H.264 QUAD-FULLHD LOW-LATENCY INTRA VIDEO ENCODER**
Muhammad Usman Karim Khan, Jan-Micha Borrmann, Lars Bauer, Muhammad Shafique and Jörg Henkel Karlsruhe Institute of Technology, DE

IPs **IP1-8, IP1-9**

1300 **LUNCH BREAK**

2.6 HOT TOPIC: Reliability Challenges of Real-time Systems in Forthcoming Technology Nodes

Room - Bayard 1130-1300

Organisers: **Said Hamdioui,** Delft University of Technology, NL
Dimitris Gizopoulos, University of Athens, GR

Chair: **Said Hamdioui,** Delft University of Technology, NL
Co-Chair: **Dimitris Gizopoulos,** University of Athens, GR

Three leading researchers in various layers of system design and integration (technology, circuit, system, application) will present recent innovations in addressing emerging questions about reliability of the electronics of today's and tomorrow's real-time systems. Speakers will address the challenges from technology perspective, from circuit/IP perspective and from architectural and hardware/software integration perspective.

1130 **CHALLENGES IN ASSESSING AND ASSURING RELIABILITY OF NANO-SCALED CMOS TECHNOLOGIES**
Guido Groeseneken IMEC, BE

1200 **ADDA: ADAPTIVE DOUBLE-SAMPLING ARCHITECTURE FOR HIGHLY FLEXIBLE ROBUST DESIGN**
Michael Nicolaidis TIMA, FR

1230 **RELIABILITY CHALLENGES IN THE DESIGN OF CRITICAL EMBEDDED SYSTEMS**
Arnaud Grasset and Philippe Bonnot Thales, FR

1300 **LUNCH BREAK**

2.7 Safety Critical Real-Time Systems

Room - Les Bans 1130-1300

Chair: Michael Paulitsch, EADS, DE
Co-Chair: Giuseppe Lipari, ENS – Cachan, FR

This session presents novel methodologies for the design and analysis of safety critical real-time systems. The first paper concerns sensitivity analysis, which characterizes bounds on admissible system parameters. The contribution concerns the bounds on admissible activation pattern of the recurrent real-time tasks. The last two papers concern mixed-criticality scheduling, an effective approach to address diverse certification requirements of safety-critical systems that integrate multiple subsystems with different levels of criticality. The contribution of the first one includes schedulability analysis algorithms to enable integration of preemption threshold (technique which controls the degree of preemption) in order to reduce scheduler overhead and improve system predictability. The second one proposes an Early-Release EDF scheduling algorithm, which can judiciously manage the early release of low-criticality tasks without affecting the timeliness of high-criticality tasks.

1130 **SENSITIVITY ANALYSIS FOR ARBITRARY ACTIVATION PATTERNS IN REAL-TIME SYSTEMS**
Moritz Neukirchner, Sophie Quinton, Tobias Michaels, Philip Axer and Rolf Ernst TU Braunschweig, DE

1200 **PT-AMC: INTEGRATING PREEMPTION THRESHOLDS INTO MIXED-CRITICALITY SCHEDULING**
Qingling Zhao[1], Zonghua Gu[1], Haibo Zeng[2]
[1]Zhejiang University, CN, [2]McGill University, CA

1230 **AN ELASTIC MIXED-CRITICALITY TASK MODEL AND ITS SCHEDULING ALGORITHM**
Hang Su and Dakai Zhu
The University of Texas at San Antonio, US

IPs **IP1-10**

1300 **LUNCH BREAK**

2.8 HOT TOPIC: IP Subsystems: The next productivity wave?

Room - Lesdigueres (Exhibition Theatre) 1130-1300

Organisers: Wido Kruijtzer, Synopsys, NL
Luciano Lavagno, Politecnico di Torino, IT

Chair: Wido Kruijtzer, Synopsys, NL
Co-Chair: Luciano Lavagno, Politecnico di Torino, IT

System-on-Chip (SoC) integrators have to deal with more and more complexity during integration of their architectures. For cost and time-to-market reasons, SoCs tend to be architected as a set of coarse-grain subsystems for recognized system functions like audio, video, connectivity, modem, etc. Such subsystem solutions consist of multiple integrated hardware IP blocks together with associated software. Till recently IP subsystems were mostly adopted internally within SoC integrators and were not yet available from traditional IP companies. However, in 2012 multiple companies announced the availably of IP subsystem solutions. This special session will provide an update on the state-of-the art with regards to IP subsystems and review if IP subsystems indeed will be the way forward to boost productivity of SoC design.

1130 **MODULAR SOC INTEGRATION WITH SUBSYSTEMS: THE AUDIO SUBSYSTEM CASE**
Pieter van der Wolf and Ruud Derwig Synopsys, NL

1200 **CONFIGURABILITY IN IP SUBSYSTEMS: BASEBAND EXAMPLES**
Pierre-Xavier Thomas, Grant Martin, David Heine, Dennis Moolenaar and James Kim
Tensilica, US

1230 **CONFIGURABLE IO INTEGRATION TO REDUCE SYSTEM-ON-CHIP TIME TO MARKET: DDR, PCIE EXAMPLES**
Frank Martin and Peter Bennett Cadence, UK

1245 **HIGH-PERFORMANCE IMAGING SUBSYSTEMS AND THEIR INTEGRATION IN MOBILE DEVICES**
Menno Lindwer and Mark Ruvald Pedersen Intel, DK

1300 **LUNCH BREAK**

3.0 Special Lunch-Time Session: Grenoble ecosystem to provide semiconductor alternative process for advanced CMOS

Room - Auditorium Dauphine 1300-1400

Organiser: **Bernard Courtois,** CMP, FR

Chair: **Enrico Macii,** Politecnico di Torino, IT

The session presents the Ultra-Thin Body and Box (UTBB) Fully Depleted SOI (FDSOI) process and shows that it meets requirements for high-performance at low-power and high energy efficiency: the 28nm FDSOI, 14nm FDSOI, and 10nm FDSOI nodes, offer a practical and cost-effective roadmap to shrink features and enable a significant boost for "green" products. With unmatched access resistance and electrostatic characteristics, planar SOI is superior to other technologies based on bulk CMOS technology or FinFET architecture. Product silicon demonstrates outstanding performances for low-power applications in consumer electronics, including tablets and mobile phones. The session will address manufacturing capabilities, design infrastructure and future R&D roadmaps.

1300 **FDSOI: FROM SUCCESSFUL COLLABORATIVE R&D TO SUCCESSFUL SILICON RESULTS**
Philippe Magarshack - STMicroelectronics, FR

1320 **DESIGN INFRASTRUCTURE TO SUPPORT ADVANCED FDSOI BELOW 20NM**
Jean-Marc Talbot - Mentor Graphics, FR

1340 **ROADMAP TOWARDS 10NM FDSOI NODE**
Laurent Malier - CEA-LETI, FR

1400 **EXHIBITION BREAK**

3.1 EXECUTIVE SESSION – The Role of Prototyping in Today's SOCs

Room - Oisans 1430-1600

Organiser: Yervant Zorian, Synopsys, US

Chair: Gary Smith, Gary Smith EDA, US

Executives:
Ivo Bolsens, Senior Vice President & CTO, Xilinx, US
Joachim Kunkel, Senior Vice President & GM, Synopsys, US
Bipin Nair, General Manager, Infotech, DE
Sanjiv Taneja, VP, Cadence Design Systems, US

Abstract: The widening gap between growing SOC complexity and designer productivity limits traditional system design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of complex SOC design, such as early investing in prototyping solutions. Executives in this session will discuss the role of prototyping and the new opportunities it may bring in designing today's complex chips..

1600 **EXHIBITION BREAK/IP1**

3.2 PANEL: The Heritage of Mead & Conway: What Has Remained the Same, What Was Missed, What Has Changed, What Lies Ahead

Room - Belle-Etoile 1430-1600

Organiser: Marco Casale-Rossi, Synopsys, US

Chair: Alberto Sangiovanni-Vincentelli, UCB, US
Co-Chair: Marco Casale-Rossi, Synopsys, US

Panelists:
Luca Carloni Columbia University, US
Bernard Courtois CMP, FR
Hugo De Man K.U. Leuven & IMEC, BE
Antun Domic Synopsys, US
Jan Rabaey UCB, US

About 30 years ago, Electronics Magazine awarded two electrical engineers and computer scientists, Carver Mead and Lynn Conway for their contribution to VLSI chips design; in 1982, the so called Mead & Conway methods, taught at 100+ universities all over the world, "not only have helped spawn a common design culture so necessary in the VLSI era, but have greatly increased interaction between university and industry so as to stimulate research by both"; concepts such as separation of design from manufacturing, design rules, silicon foundries, addressing complexity through design methodology, new, electronic representations of design data, have enabled tens of thousands of chip designers, and tens of thousands of chip designs. Today, as Moore's Law – a term coined by Carver Mead – has brought as from 10 microns to 10 nanometers, what is the heritage of Mead & Conway?

UCB Professor Alberto Sangiovanni-Vincentelli will moderate an industry and research panel, to discuss what has remained the same, what was missed, what has changed, and what lies ahead.

1600 **EXHIBITION BREAK/IP1**

3.3 Addressing Process and Delay Variation in High-Level Synthesis

Room - Stendhal 1430-1600

Chair: Lars Bauer, Karlsruhe Institute of Technology, DE
Co-Chair: Hiroyuki Tomiyama, Ritsumeikan University, JP

The first two papers target the problem of process variation and aging issues for high-level and instruction-set synthesis. The last paper incorporates delay variations arising from speculative adder structures in high-level synthesis.

1430 **PROFIT MAXIMIZATION THROUGH PROCESS VARIATION AWARE HIGH LEVEL SYNTHESIS WITH SPEED BINNING**
Zhao Mengying[1], Alex Orailoglu[2], Xue Chun Jason[1]
[1]City University of Hong Kong, HK,
[2]University of California, US

1500 **INSTRUCTION-SET EXTENSION UNDER PROCESS VARIATION AND AGING EFFECTS**
Yuko Hara-Azumi[1], Farshad Firouzi[2], Saman Kiamehr[2], Mehdi Tahoori[2]
[1]Nara Institute of Science and Technology, JP
[2]Karlsruhe Institute of Technology, DE

1530 **MULTISPECULATIVE ADDITIVE TREES IN HIGH-LEVEL SYNTHESIS**
Alberto A. Del Barrio[1], Román Hermida[1], Seda O. Memik[2], José M. Mendías[1], María C. Molina[1]
[1]Complutense University of Madrid, ES
[2]Northwestern University, US

IPs **IP1-11. IP1-12**

1600 **EXHIBITION BREAK/IP1**

3.4 Microarchitectural Techniques for Reliability

Room - Chartreuse 1430-1600

Chair: Todd Austin, Michigan University Ann Arbor, US
Co-Chair: Mladen Berekovic, Technical University of Braunschweig, DE

This session introduces a variety of papers regarding reliability issues, which are managed by fault tolerance, fault avoidance, and error correction techniques. The first paper proposes to aggressively utilize computation results from error-prone processors. The second one tries to avoid voltage drops in multi-core processors by focusing on the inter-core power interactions. The third and fourth papers propose error detection and correction techniques; the former one is for memories and the latter one for logic circuits.

1430 **EXTRACTING USEFUL COMPUTATION FROM ERROR-PRONE PROCESSORS FOR STREAMING APPLICATIONS**
Yavuz Yetim, Margaret Martonosi and Sharad Malik
Princeton University, US

1500 **ORCHESTRATOR: A LOW-COST SOLUTION TO REDUCE VOLTAGE EMERGENCIES FOR MULTI-THREADED APPLICATIONS**
Xing Hu, Guihai Yan, Yu Hu and Xiaowei Li
Chinese Academy of Sciences, CN

1530 **MEMORY ARRAY PROTECTION: CHECK ON READ OR CHECK ON WRITE?**
Panagiota Nikolaou[1], Yanos Sazeides[1], Lorena Ndreou[1], Emre Ozer[2], Sachin Idgunji[3]
[1]University of Cyprus, CY, [2]ARM, UK, [3]ARM, UK,

1545 **FAULTM: ERROR DETECTION AND RECOVERY USING HARDWARE TRANSACTIONAL MEMORY**
Gulay Yalcin, Osman Unsal and Adrian Cristal
Barcelona Supercomputing Center, ES

IPs **IP1-13**

1600 **EXHIBITION BREAK/IP1**

3.5 Energy Efficient Mobile and Cloud Computing Systems

Room - Meije 1430-1600

Chair: Tajana Rosing, University of California San Diego, US
Co-Chair: Theocharis Theocharides, University of Cyprus, CY

The session focuses on modelling, model-driven optimization, and low-energy architectures for energy-efficient computing in mobile devices and cloud computing systems. The first paper explores new computationally inexpensive detection methods of thermal behavior on multi-core architectures.

The second paper presents a novel way of computing by using energy-efficient 3D wide memory interfaces. Finally, the third paper presents a low-power FFT implementation for multiple applications.

1430 **SCC THERMAL MODEL IDENTIFICATION VIA ADVANCED BIAS-COMPENSATED LEAST-SQUARES**
Roberto Diversi, Andrea Bartolini, Andrea Tilli, Francesco Beneventi and Luca Benini
University of Bologna, IT

1500 **SYSTEM AND CIRCUIT LEVEL POWER MODELING OF ENERGY-EFFICIENT 3D-STACKED WIDE I/O DRAMs**
Karthik Chandrasekar[1], Christian Weis[2], Benny Akesson[3], Norbert Wehn[2], Kees Goossens[4]
[1]Delft University of Technology, NL
[2]University of Kaiserslautern, DE
[3]Polytechnic Institute of Porto, PT
[4]Eindhoven University of Technology, NL

1515 **DESIGN OF LOW POWER, HIGH PERFORMANCE SYNCHRONOUS AND ASYNCHRONOUS 64-POINT FFT**
William Lee[1], Vikas Vij[1], Kenneth Stevens[1], Anthony Thatcher[2]
[1]University of Utah, US, [2]Intel, US

1530 **A MULTI-LEVEL MONTE CARLO FPGA ACCELERATOR FOR OPTION PRICING IN THE HESTON MODEL**
Christian de Schryver, Pedro Torruella and Norbert Wehn
University of Kaiserslautern, DE

IPs **IP1-14, IP1-15, IP1-16, IP1-17**

1600 **EXHIBITION BREAK/IP1**

3.6 Dealing with Timing Variation in Advanced Technologies

Room - Bayard 1430-1600

Chair: Hans Manhaeve, Ridgetop Europe, BE
Co-Chair: Saqib Khursheed, University of Southampton, UK

To get the best performance one needs to minimize slack, however, this is getting challenging since one needs to take into account many aspects. The papers in this session present the benefits of taking aging into account during the design phase, how to measure in-situ the slack, and test pattern generation that takes into account statistical variation to improve coverage.

1430 **MTTF-BALANCED PIPELINE DESIGN**
Fabian Oboril and Mehdi Tahoori
Karlsruhe Institute of Technology, DE

1500 **EFFICIENT VARIATION-AWARE STATISTICAL DYNAMIC TIMING ANALYSIS FOR DELAY TEST APPLICATIONS**
Marcus Wagner and Hans-Joachim Wunderlich
University of Stuttgart, DE

1530 **SLACKPROBE: A LOW OVERHEAD IN SITU ON-LINE TIMING SLACK MONITORING METHODOLOGY**
Liangzhen Lai[1], Vikas Chandra[2], Robert Aitken[2], Puneet Gupta[1]
[1]UCLA, US, [2]ARM, US

IPs **IP1-18, IP1-19**

1600 **EXHIBITION BREAK/IP1**

3.7 Timing Analysis

Room - Les Bans 1430-1600

Chair: Stefan Petters, ISEP, PT
Co-Chair: Michael Paulitsch, EADS, DE

The session focuses on low-level timing analysis of real-time systems. The first paper presents a novel way of analysing the behaviour of FIFO caches, which is known to be a demanding challenge. The second paper introduces the timing analysis of multi-core processors in an automotive setting, when this is subject to mode changes. The last paper explores the analysis of contention on shared SDRAM memory under a credit-controlled static priority arbitration scheme.

1430 **FIFO CACHE ANALYSIS FOR WCET ESTIMATION: A QUANTITATIVE APPROACH**
Nan Guan[1], Xinping Yang[1], Mingsong Lv[2], Wang Yi[1]
[1]Uppsala University, SE, [2]Northeastern University, CN

1500 **TIMING ANALYSIS OF MULTI-MODE APPLICATIONS ON AUTOSAR CONFORM MULTI-CORE SYSTEMS**
Mircea Negrean, Sebastian Klawitter and Rolf Ernst
TU Braunschweig, DE

1530 **BOUNDING SDRAM INTERFERENCE: DETAILED ANALYSIS VS. LATENCY-RATE ANALYSIS**
Hardik Shah[1], Alois Knoll[2], Benny Akesson[3]
[1]ForTISS, DE, [2]Technical University Munich, DE
[3]Polytechnic Institute of Porto, PT

1600 **EXHIBITION BREAK/IP1**

3.8 HOT TOPIC: Design for Variability, Manufacturability, Reliability, and Debug: Many Faces of the Same Coin?

Room - Lesdigiueres (Exhibition Theatre) 1430-1600

Organiser: Vikas Chandra, ARM, US

Chair: Vikas Chandra, ARM, US
Co-Chair: Kartik Mohanram, University of Pittsburgh, US

Complex SoCs of the future are subject to various sources of variability, reliability failures and design errors (logical or electrical) due to sheer design complexity, and marginal behaviors induced by uncertainties in manufacturing processes, temporal variability and operating conditions. In this session, we will cover this entire spectrum ranging from state-of-the-art techniques for manufacturability, variability and aging mitigation to effective post-silicon debug methods and everything in between.

1430 **ROLE OF DESIGN IN MULTIPLE PATTERNING: TECHNOLOGY DEVELOPMENT, DESIGN ENABLEMENT AND PROCESS CONTROL**
Rani A. Ghaida[1] and Puneet Gupta[2]
[1]GlobalFoundries, US, [2]UCLA, US

1500 **OVERCOMING POST-SILICON VALIDATION CHALLENGES THROUGH QUICK ERROR DETECTION (QED)**
David Lin[1], Ted Hong[1], Yanjing Li[1], Farzan Fallah[1], Donald S. Gardner[2], Nagib Hakim[2], Subhasish Mitra[1]
[1]Stanford University, US, [2]Intel, US

1530 **STOCHASTIC DEGRADATION MODELING AND SIMULATION FOR ANALOG INTEGRATED CIRCUITS IN NANOMETER CMOS**
Georges Gielen and Elie Maricau KU Leuven, BE

1600 **EXHIBITION BREAK/IP1**

IP1 Interactive Presentations

Room - Salle de Reception 1600-1630

Interactive Presentations run simulatenously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP1-1 **AN AUTOMATED PARALLEL SIMULATION FLOW FOR HETEROGENEOUS EMBEDDED SYSTEMS**
Seyed Hosein Attarzadeh Niaki and Ingo Sander
KTH Royal Institute of Technology, SE

IP1-2 **MUTATION ANALYSIS WITH COVERAGE DISCOUNTING**
Peter Lisherness, Nicole Lesperance and Kwang-Ting Cheng UCSB, US

IP1-3 **SCALABLE FAULT LOCALIZATION FOR SYSTEMC TLM DESIGNS**
Hoang M. Le, Daniel Große and Rolf Drechsler
University of Bremen, DE

IP1-4 **SMARTCAP: USER EXPERIENCE-ORIENTED POWER ADAPTATION FOR SMARTPHONE'S APPLICATION PROCESSOR**
Xueliang Li, Guihai Yan, Yinhe Han and Xiaowei Li
Chinese Academy of Sciences, CN

IP1-5 **RUNTIME POWER ESTIMATION OF MOBILE AMOLED DISPLAYS**
Dongwon Kim, Wonwoo Jung and Hojung Cha
Yonsei University, KR

IP1-6 **A DUAL-GRAIN HIT/MISS DETECTOR FOR LARGE DIE-STACKED DRAM CACHES**
Michel El Nacouzi, Islam Atta, Myrto Papadopoulou, Jason Zebchuk, Natalie Enright Jerger and Andreas Moshovos
University of Toronto, CA

IP1-7 **REDUCING WRITES IN PHASE-CHANGE MEMORY ENVIRONMENTS BY USING EFFICIENT CACHE REPLACEMENT POLICIES**
Roberto Rodriguez, Fernando Castro, Daniel Chaver, Luis Pinuel and Francisco Tirado
Complutense University, ES

IP1-8 **A 100 GOPS ASP BASED BASEBAND PROCESSOR FOR WIRELESS COMMUNICATION**
Zhu Ziyuan, Tang Shan, Su Yongtao, Han Juan, Sun Gang and Shi Jinglin
Chinese Academy of Sciences, CN

IP1-9 **HARDWARE-SOFTWARE COLLABORATIVE COMPLEXITY REDUCTION SCHEME FOR THE EMERGING HEVC INTRA ENCODER**
Muhammad Usman Karim Khan, Muhammad Shafique, Mateus Grellert da Silva and Jörg Henkel
Karlsruhe Institute of Technology, DE

IP1-10 **AN OPEN PLATFORM FOR MIXED-CRITICALITY REAL-TIME ETHERNET**
Gonzalo Carvajal[1] and Sebastian Fischmeister[2]
[1]Universidad de Concepcion, CL,
[2]University of Waterloo, CA

IP1-11 **MULTI-PUMPING FOR RESOURCE REDUCTION IN FPGA HIGH-LEVEL SYNTHESIS**
Andrew Canis, Jason Anderson and Stephen Brown
University of Toronto, CA

IP1-12 **RESOURCE-CONSTRAINED HIGH-LEVEL DATAPATH OPTIMIZATION IN ASIP DESIGN**
Yuankai Chen and Hai Zhou Northwestern University, US

IP1-13 **PHOENIX: REVIVING MLC BLOCKS AS SLC TO EXTEND NAND FLASH DEVICES LIFETIME**
Xavier Jimenez, David Novo and Paolo Ienne
Ecole Polytechnique Fédérale de Lausanne, CH

IP1-14 **NON-SPECULATIVE DOUBLE-SAMPLING TECHNIQUE TO INCREASE ENERGY-EFFICIENCY IN A HIGH-PERFORMANCE PROCESSOR**
Junyoung Park, Ameya Chaudhari and Jacob Abraham
The University of Texas at Austin, US

IP1-15 **USER-AWARE ENERGY EFFICIENT STREAMING STRATEGY FOR SMARTPHONE BASED VIDEO PLAYBACK APPLICATIONS**
Hao Shen and Qinru Qiu Syracuse University, US

IP1-16 **UTILITY-AWARE DEFERRED LOAD BALANCING IN THE CLOUD DRIVEN BY DYNAMIC PRICING OF ELECTRICITY**
Muhammad Adnan and Rajesh Gupta
University of California San Diego, US

IP1-17 **LEAKAGE AND TEMPERATURE AWARE SERVER CONTROL FOR IMPROVING ENERGY EFFICIENCY IN DATA CENTERS**
Marina Zapater[1], José L. Ayala[1], José M. Moya[1], Kalyan Vaidyanathan[2], Kenny Gross[2], Ayse K. Coskun[3]
[1]Universidad Politécnica de Madrid, ES [2]UC San Diego, US
[3]Boston University, US

IP1-18 **CAPTURING POST-SILICON VARIATIONS BY LAYOUT-AWARE PATH-DELAY TESTING**
Xiaolin Zhang, Jing Ye, Yu Hu and Xiaowei Li
Chinese Academy of Sciences, CN

IP1-19 **ADAPTIVE REDUCTION OF THE FREQUENCY SEARCH SPACE FOR MULTI-VDD DIGITAL CIRCUITS**
Chandra Suresh[1], Ender Yilmaz[2], Ozgur Sinanoglu[1], Sule Ozev[3]
[1]NYU Abu Dhabi, AE, [2]Freescale, US,
[3]Arizona State University, US

4.1 EXECUTIVE SESSION: Is Reusing Off-the-Shelf Semiconductor IP Possible Today?

Room - Oisans 1700-1830

Organiser: **Yervant Zorian,** Synopsys, US

Chair: **Peggy Aycinena,** EDA Weekly, US

Executives:
Christoph Heer, Head Design System & IP,
Intel Mobile Communication, DE
Navraj Nandra, Senior Director, Synopsys, US
James McNiven, Vice President, ARM, UK

Abstract: While today's SOCs systematically use a range of IP blocks, meeting end product requirements, such as power, performance and area, remain an obstacle on reusing off-the-shelf IP blocks. The speakers in this executive session will address the current trends and challenges in the semiconductor IP industry and discuss the level of customization versus reuse needed to meet today's SOC requirements.

1830 **CLOSE**

EVENING RECEPTION
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4.2 The Quest for Better NoCs

Room - Belle-Etoile 1700-1830

Chair: Pascal Vivet, CEA-LETI, FR
Co-Chair: Riccardo Locatelli, ST Microelectronics, FR

This session focuses on the architectural side of NoC design, starting with an asynchronous switch architecture and related tool flow for implementation. The next paper proposes an efficient, single-cycle-propagation technique that reduces NoC traversal latencies. The last paper analyzes the trade-offs of port sharing in NoC routers.

1700 **A TRANSITION-SIGNALING BUNDLED DATA NOC SWITCH ARCHITECTURE FOR COST-EFFECTIVE GALS MULTICORE SYSTEMS**
Alberto Ghiribaldi[1], Davide Bertozzi[1], Steven M. Nowick[2]
[1]University of Ferrara, IT, [2]Columbia University, US

1730 **SMART: A SINGLE-CYCLE RECONFIGURABLE NoC FOR SoC APPLICATIONS**
Chia-Hsin Owen Chen, Sunghyun Park, Tushar Krishna, Suvinay Subramanian Li-Shiuan Peh and Anantha P. Chandrakasan
Massachusetts Institute of Technology, US

1800 **SWITCH FOLDING: NETWORK-ON-CHIP ROUTERS WITH TIME-MULTIPLEXED OUTPUT PORTS**
Giorgos Dimitrakopoulos[1], Nikodimos Georgiadis[2], Chrysostomos Nicopoulos[2], Emmanouil Kalligeros[3]
[1]Democritus University of Thrace, GR,
[2]University of Cyprus, CY, [3]University of the Aegean, GR

IPs **IP2-1, IP2-2**

1830 **CLOSE**

EVENING RECEPTION
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4.3 EMBEDDED TUTORIAL: Reliability Analysis Reloaded: How Will We Survive?

Room - Stendhal 1700-1830

Organisers: Goerschwin Fey, University of Bremen, DE
Matteo Sonza Reorda, Politecnico di Torino, IT

Chair: Bernd Becker, University of Freiburg, DE
Co-Chair: Xavier Vera, Intel, ES

Concepts for reliability analysis have been a hot topic in research and industry ever since the introduction of electronic systems over 40 years ago.

Reliability problems are expected to increase rapidly for future technology nodes, for many reasons. The sheer complexity of today's and future "more Moore" and "more than Moore" systems as well as the huge universe of potential faults requires reliability analysis to be revisited from this new perspective. This embedded tutorial will focus on reliability analysis from both an academic and an industrial perspective, including different layers of abstraction. The first talk will concentrate on the lowest layer from an industrial perspective, i.e. how we can find models for device-level reliability that may be used for determining the reliability of a system. The second talk will approach state-of-the-art techniques from an academic point of view to evaluate the reliability of complex systems, including virtualization environments. The tutorial will be completed with a talk that describes the development of safety critical systems in industrial automation, in particular pointing out how reliability evaluation is handled on the basis of current safety standards.

1700 **RELIABILITY EVALUATION AT THE DEVICE LEVEL AND ITS IMPACT ON DESIGN**
Rob Aitken ARM, US

1730 **RELIABILITY EVALUATION AT THE SYSTEM LEVEL**
Z. T. Kalbarczyk
University of Illinois at Urbana-Champaign, AE

1800 **ON EVALUATING THE RELIABILITY OF INDUSTRIAL PRODUCTS AND THE IMPACT OF SAFETY STANDARDS IN AUTOMATION INDUSTRY**
Frank Reichenbach
ABB Corporate Research, NO

1830 **CLOSE**

EVENING RECEPTION
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4.4 Emerging Solutions to Manage Energy/Performance Trade-Offs Along the Memory Hierarchy

Room - Chartreuse 1700-1830

Chair: Mladen Berekovic, Technical University of Braunschweig, DE
Co-Chair: Cristina Silvano, Politecnico di Milano, IT

The session discusses emerging solutions to efficiently manage energy/performance trade-offs along the memory hierarchy from caches to secondary storage solutions. The first paper proposes a multiple access cache interface to provide low energy. The second paper introduces an efficient RAM management technique for NAND flash-based storage systems, while the third paper describes a data protection technique for NAND flash storage systems. The fourth paper proposes how to exploit sub-arrays inside a bank to improve the performance of Phase Change Memory, a promising alternative or supplement to DRAM.

1700 **MALEC: A MULTIPLE ACCESS LOW ENERGY CACHE**
Matthias Boettcher[1], Giacomo Gabrielli[2], Bashir M. Al-Hashimi[1], Danny Kershaw[3]
[1]University of Southampton, UK, [2]ARM, UK, [3]NXP Semiconductors, AT

1730 **TREEFTL: EFFICIENT RAM MANAGEMENT FOR HIGH PERFORMANCE OF NAND FLASH-BASED STORAGE SYSTEMS**
Chundong Wang and Weng-Fai Wong
National University of Singapore, SG

1800 **DA-RAID-5: A DISTURB AWARE DATA PROTECTION TECHNIQUE FOR NAND FLASH STORAGE SYSTEMS**
Jie Guo[1], Wujie Wen[1], Yaojun Zhang[1], Sicheng Li[2], Hai Li[1], Yiran Chen[1]
[1]University of Pittsburgh, US,
[2]Polytechnic Institute of New York University, US

1815 **EXPLOITING SUBARRAYS INSIDE A BANK TO IMPROVE PHASE CHANGE MEMORY PERFORMANCE**
Jianhui Yue and Yifeng Zhu
University of Maine, US

IPs **IP2-3, IP2-4, IP2-5**

1830 **CLOSE**

EVENING RECEPTION
SPONSORED BY THE IEEE COUNCIL ON EDA

4.5 Device Identification and Protection

Room - Meije 1700-1830

Chair: Patrick Koeberl, Intel Labs, DE
Co-Chair: Roel Maes, Intrinsic-ID, NL

System designers need secure building blocks for robust protection against physical and network attacks. This session presents the novel construction and implementation of physically unclonable functions as well as recent trends on counter-measure evaluation and realization.

1700 **COMPREHENSIVE ANALYSIS OF SOFTWARE COUNTERMEASURES AGAINST FAULT ATTACKS**
Nikolaus Theißing[1], Dominik Merli[2], Michael Smola[3], Frederic Stumpf[2], Georg Sigl[4]
[1]Institute of Flight Systems, University of the Armed Forces, DE, [2]Fraunhofer - AISEC, DE,
[3]Infineon Technologies, DE
[4]Technische Universität München, DE

1730 **AN EDA-FRIENDLY PROTECTION SCHEME AGAINST SIDE-CHANNEL ATTACKS**
Ali Galip Bayrak[1], Nikola Velickovic[1], Francesco Regazzoni[2], David Novo Bruna[1], Philip Brisk[3], Paolo Ienne[1]
[1]EPFL, CH, [2]Alari, CH, [3]UC Riverside, US

1745 **DESIGN AND IMPLEMENTATION OF A GROUP-BASED RO PUF**
Chi-En Yin[1], Gang Qu[1], Qiang Zhou[2]
[1]Univ. of Maryland, College Park, US,
[2]Tsinghua University, CN

1800 **CLOCKPUF: PHYSICAL UNCLONABLE FUNCTIONS BASED ON CLOCK NETWORKS**
Yida Yao[1], Myungbo Kim[1], Jianmin Li[1],
Igor L. Markov[1], Farinaz Koushanfar[2]
[1]University of Michigan, US, [2]Rice University, US

IPs **IP2-6, IP2-7**

1830 **CLOSE**

EVENING RECEPTION
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4.6 New Techniques for Test Pattern Generation

Room - Bayard 1700-1830

Chair: Sudhakar Reddy, University of Iowa, US
Co-Chair: Matteo Sonza Reorda, Politecnico di Torino, US

The session presents new test pattern generation methods for low power memory cells as well as for dealing with unknown values and delay faults.

1700 **ACCURATE QBF-BASED TEST PATTERN GENERATION IN PRESENCE OF UNKNOWN VALUES**
Stefan Hillebrecht[1], Michael A. Kochte[2], Dominik Erb[1],
Hans-Joachim Wunderlich[2], Bernd Becker[1]
[1]University of Freiburg, DE, [2]University of Stuttgart, DE

1730 **TEST SOLUTION FOR DATA RETENTION FAULTS IN LOW-POWER SRAMS**
Leonardo Henrique Bonet Zordan[1], Alberto Bosio[1],
Patrick Girard[1], Luigi Dilillo[1], Aida Todri-Sanial[1],
Arnaud Virazel[1], Nabil Badereddine[2]
[1]LIRMM, FR, [2]Intel Mobile Communications, FR

1800 **EFFICIENT SAT-BASED DYNAMIC COMPACTION AND RELAXATION FOR LONGEST SENSITIZABLE PATHS**
Matthias Sauer[1], Sven Reimer[1], Tobias Schubert[1],
Ilia Polian[2], Bernd Becker[1]
[1]University of Freiburg, DE, [2]University of Passau, DE

IPs **IP2-8**

1830 **CLOSE**

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4.7 HOT TOPIC: Security Challenges in Automotive Hardware/ Software Architecture Design

Room - Les Bans 1700-1830

Organiser: Samarjit Chakraborty, TU Munich, DE

Chair: Jason Xue, City Univ. of Hong Kong, HK
Co-Chair: Dip Goswami, TU Munich, DE

In modern cars, innovations are mainly driven by electronics and software. As a result, top-of-the-range vehicles comprise up to 100 Electronic Control Units (ECUs) and multiple heterogeneous buses connected via gateways. Various wireless communication protocols, like keyless entry systems or WiFi, connect the car with its surroundings while functionality in upcoming cars will be even more based on software with strong wireless connectivity. Similar to the first computers connected to the Internet, current automotive architectures are not designed for security which makes them highly vulnerable to attacks infiltrating the system. This session will focus on discussing this problem and on potential solutions from an embedded systems design perspective.

1700 **SECURITY CHALLENGES IN AUTOMOTIVE HARDWARE/SOFTWARE ARCHITECTURE DESIGN**
Florian Sagstetter, Martin Lukasiewycz, Sebastian Steinhorst, Marko Wolf, Alexandre Bouard, William R. Harris, Somesh Jha, Thomas Peyrin, Axel Poschmann and Samarjit Chakraborty - TUM-CREATE, SG

1730 **AUTOMOTIVE IP SECURITY: ENABLER FOR NEW CONNECTED FUNCTIONS IN CAR**
Alexandre Bouard - BMW, DE

1800 **HACKING CARS: TAKING A LOOK BACK, A LOOK AT AND A LOOK AHEAD ON AUTOMOTIV SECURITY**
Marko Wolf - Escrypt, DE

1830 **CLOSE**

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4.8 EXHIBITION THEATRE: Testimonials

Room - Lesdigiueres (Exhibition Theatre) 1700-1830

Organiser/Moderator: Jürgen Haase, edacentrum, DE

In this session industrial testimonials will offer engineers an insight into good working practices and state-of-the-art design methods of market leaders. This sessions features design centering of IO in 28nm FDSOI technology, SoC power integrity verification with focus on analogue/mixed signal macros, data management for future SoCs and evolutionary computation for validation, testing and design automation.

1700 **DESIGN CENTERING OF IO IN 28NM FDSOI TECHNOLOGY**
Hubert Degoirat - STMicroelectronics, FR

1720 **USING APACHE REDHAWK FOR SOC POWER INTEGRITY VERIFICATION WITH FOCUS ON ANALOGUE/MIXED SIGNAL MACROS**
Jack Kruppa - Infineon Technologies, DE

1740 **EVOLUTIONARY COMPUTATION FOR VALIDATION, TESTING AND DESIGN AUTOMATION**
Senad Durakovic and Aktan Burcin - Intel, US

1800 **DATA MANAGMENT IN FUTURE SOCS MADE EASY**
Axel Jantsch - ELSIP, SE

1830 **CLOSE**

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SPECIAL DAY

WEDNESDAY 20 MARCH, 2013

0730 **REGISTRATION and SPEAKERS' BREAKFAST**

5.1 SPECIAL DAY 1 HOT TOPIC - System Approaches to Energy-Efficiency

Room - Oisans 0830-1000

Organiser: Ahmed Jerraya, CEA-LETI-MINATEC, FR

Chair: Patrick Blouet, ST Ericsson, FR
Co-Chair: Ahmed Jerraya, CEA-LETI-MINATEC, FR

At system level, energy consumption optimisation may be the most rewarding. Different approaches may be applied to improve energy efficiency. This Hot-Topic Session explores both system architecture and applications to reach better energy efficiency.

0830 **EXPERIENCES WITH MOBILE PROCESSORS FOR ENERGY EFFICIENT HPC**
Alex Ramirez, Nikola Rajovic, Alejandro Rico, James Vipond, Isaac Gelado and Nikola Puzovic BSC, ES

0850 **WHAT DESIGNS FOR COMING SUPERCOMPUTERS?**
Xavier Vigouroux Bull, FR

0910 **ENERGY-EFFICIENT IN-MEMORY DATABASE COMPUTING**
Wolfgang Lehner TU Dresden, DE

0930 **PERFORMANCE ANALYSIS OF HPC APPLICATIONS ON LOW-POWER EMBEDDED PLATFORMS**
Luka Stanisic[1], Brice Videau[1], Johan Cronsioe[1], Augustin Degomme[1], Vania Marangozova-Martin[1], Arnaud Legrand[1], Jean-François Méhaut[1], Jean-François Méhaut[2]
[1]CNRS/LIG, FR, [2]UJF/LIG/CEA-Leti, FR

1000 **EXHIBITION BREAK/IP2**

5.2 PANEL: Can Energy Harvesting Deliver Enough Power for Automotive Electronics?

Room - Belle-Etoile 0830-1000

Organisers: Tom Kazmierski, University of Southampton, UK
Christoph Grimm, TU Kaiserslautern, DE

Chair: Jürgen Haase, Edacentrum, DE
Co-Chair: Norbert Wehn, TU Kaiserslautern, DE

Panellists:
Thomas Herndl - Infineon Technologies, AT
Robert Kappel - Graz University of Technology, AT
Paul Mitcheson - Imperial College, UK
Christoph Grimm - TU Kaiserslautern, DE
Tom J. Kazmierski - University of Southampton, UK

The panel will address upcoming technologies aimed at energy efficiency in energy harvester powered sensor networks for automotive applications. It will focus on the main challenge faced by the researchers working in this area: how to design efficiently analogue and digital automotive electronics powered by extremely low levels of harvested energy? The two industrial panelists will outline issues facing battery-less automotive sensor nodes powered by kinetic and thermal energy harvesters. The academic panelists will present currently being developed adaptive harvesters which can deliver maximum energy output in a changing environment, discuss techniques of virtual prototyping for ultra-low energy consumption and methods to analyse and optimise energy management and efficiency in automotive sensor nodes.

5.3 Post-Silicon Debug Techniques

Room - Stendhal 0830-1000

Chair: Jaan Raik, Tallinn University of Technology, EE
Co-Chair: Adrian Evans, iRoC Technologies, FR

It is becoming increasingly difficult to fully verify an SoC prior to tape-out resulting in more debug work occurring after first silicon. In the past, the techniques for post-silicon debug were largely ad-hoc. This session includes papers which highlight a new, emerging body of work which applies advanced algorithms to obtain optimized hardware for post-silicon debug. The first paper describes a new technique for selecting an optimal set of trace signals using a mixture of fast metrics and simulation profiling. In the second paper, the authors apply anomaly detection algorithms similar to those used for fraud detection to the automatic temporal and spatial localization of bugs. The third paper presents a low-area hardware block which can be used to reduce the volume of data that needs to be exported when dumping cache contents in the lab. The final paper tackles a slightly different, but very important aspect of silicon validation problem and proposes an innovative technique to perform BER estimation on high-speed links.

0830 **A HYBRID APPROACH FOR FAST AND ACCURATE TRACE SIGNAL SELECTION FOR POST-SILICON DEBUG**
Min Li and Azadeh Davoodi
University of Wisconsin - Madison, US

0900 **MACHINE LEARNING-BASED ANOMALY DETECTION FOR POST-SILICON BUG DIAGNOSIS**
Andrew DeOrio[1], Qingkun Li[2], Matthew Burgess[1], Valeria Bertacco[1]
[1]University of Michigan, US,
[2]University of Illinois at Urbana-Champaign, US

0915 **SPACE SENSITIVE CACHE DUMPING FOR POST-SILICON VALIDATION**
Sandeep Chandran, Smruti R. Sarangi and Preeti Ranjan Panda
Indian Institute of Technology Delhi, IN

0930 **FAST AND ACCURATE BER ESTIMATION METHODOLOGY FOR I/O LINKS BASED ON EXTREME VALUE THEORY**
Alessandro Cevrero[1], Nestor Evmorfopoulos[2], Charalampos Antoniadis[2], Paolo Ienne[1], Yusuf Leblebici[1], Andreas Burg[1], George Stamoulis[2]
[1]EPFL, CH, [2]University of Thessaly, GR

IPs **IP2-9**

1000 **EXHIBITION BREAK/IP2**

5.4 Novel Approaches for Real-Time Architectures

Room - Chartreuse 0830-1000

Chair: Cristina Silvano, Politecnico di Milano, IT
Co-Chair: Andreas Moshovos, University of Toronto, CA

This section focuses on new approaches for real-time architectures that go beyond classic static approaches. The first paper presents the first practical, effective, and efficient cache design that enables probabilistic worst-case execution time analysis. The second paper presents a novel architecture that enables fast and time-predictable computation for switched hybrid automata, a new modelling framework for power electronics applications. The third paper presents a conservative open-page memory controller policy that improves average-case performance without sacrificing worst-case time guarantees.

0830 **A CACHE DESIGN FOR PROBABILISTICLY ANALYSABLE REAL-TIME SYSTEMS**
Leonidas Kosmidis[1,2], Jaume Abella[2], Eduardo Quiñones[2], Francisco J. Cazorla[3,2]
[1]Universitat Politècnica de Catalunya, ES
[2]Barcelona Supercomputing Center, ES
[3]Spanish National Research Council, ES

0900 **MARTHA: ARCHITECTURE FOR CONTROL AND EMULATION OF POWER ELECTRONICS AND SMART GRID SYSTEMS**
Michel Kinsy[1], Omer Khan[2], Ivan Celanovic[1], Srinivas Devadas[1]
[1]MIT, US, [2]University of Connecticut, US

0930 **CONSERVATIVE OPEN-PAGE POLICY FOR MIXED TIMECRITICALITY MEMORY CONTROLLERS**
Sven Goossens[1], Benny Akesson[2], Kees Goossens[1]
[1]Eindhoven University of Technology, NL
[2]Polytechnic Institute of Porto, PT

IPs **IP2-10**

1000 **EXHIBITION BREAK/IP2**

5.5 Error-Aware Adaptive Modern Computing Architectures

Room - Meije 0830-1000

Chair: Marco Santambroglio, Politecnico di Milano, IT
Co-Chair: Marian Verhelst, Katholieke Universiteit Leuven, BE

This session covers the area of reliable and adaptive systems for practical computing applications. The scope of this session includes the development, optimization, and practical application mechanisms to compensate for aging and temperature, development of fault-tolerant systems, redundant designs and applications, reconfigurable systems and applications, static and dynamic reconfiguration techniques, context-aware applications, and self-adaptive architectures.

0830 **HOT-SWAPPING ARCHITECTURE WITH BACK-BIASED TESTING FOR MITIGATION OF PERMANENT FAULTS IN FUNCTIONAL UNIT ARRAY**
Zoltan E. Rakosi[1], Masayuki Hiromoto[1], Hiroshi Tsutsui[1], Takashi Sato[1], Yukihiro Nakamura[2], Hiroyuki Ochi[1]
[1]Kyoto University, JP, [2]Ritsumeikan University, JP

0900 **VARIATION-TOLERANT OPENMP TASKING ON TIGHTLY-COUPLED PROCESSOR CLUSTERS**
Abbas Rahimi[1], Andrea Marongiu[2], Paolo Burgio[2], Rajesh Gupta[1], Luca Benini[2]
[1]University of California, San Diego, US,
[2]University of Bologna, IT

0930 **ACCURATE AND EFFICIENT RELIABILITY ESTIMATION TECHNIQUES DURING ADL-DRIVEN EMBEDDED PROCESSOR DESIGN**
Zheng Wang, Kapil Singh, Chao Chen and Anupam Chattopadhyay RWTH Aachen, DE

1000 **EXHIBITION BREAK/IP2**

5.6 Advances in Mixed-Signal, RF, and MEMS testing

Room - Bayard 0830-1000

Chair: Salvador Mir, TIMA Laboratory, FR
Co-Chair: Adoración Rueda, University of Seville, ES

The first paper uses industrial data to demonstrate a technique for reducing the complexity of wafer-level testing of RF transceivers. The second paper presents the experimental validation of a defect detection and error-recovery technique for microfluidic bio-chips. The third paper shows defect-oriented testing in action for a large industrial mixed-signal circuit.

0830 **HANDLING DISCONTINUOUS EFFECTS IN MODELING SPATIAL CORRELATION OF WAFER-LEVEL ANALOG/RF TESTS**
Ke Huang[1], Nathan Kupp[2], John Carulli[3], Yiorgos Makris[1]
[1]UT Dallas, US, [2]Yale University, US, [3]Texas Instruments, US

0900 **FAULT DETECTION, REAL-TIME ERROR RECOVERY, AND EXPERIMENTAL DEMONSTRATION FOR DIGITAL MICROFLUIDIC BIOCHIPS**
Kai Hu, Bang-Ning Hsu, Andrew Madison, Krishnendu Chakrabarty and Richard Fair
Duke University, US

0930 **FAULT ANALYSIS AND SIMULATION OF LARGE SCALE INDUSTRIAL MIXED-SIGNAL CIRCUITS**
Ender Yilmaz[1], Geoff Shofner[1], LeRoy Winemberg[1], Sule Ozev[2]
[1]Freescale Semiconductor, US, [2]Arizona State University, US

IPs **IP2-11**

1000 **EXHIBITION BREAK/IP2**

5.7 Compilers and Software Synthesis for Embedded Systems

Room - Les Bans 0830-1000

Chair: Björn Franke, University of Edinburgh, UK
Co-Chair: Heiko Falk, Ulm University, DE

This session covers a broad spectrum of topics in compilers, software synthesis, validation, and transformation. The first paper addresses communication optimization for kernels offloaded to accelerators. It is followed by a paper focussing on concurrency in a synchronous model of computation. The third paper deals with source-level cache modelling. The fourth paper proposes the management of heap data of tasks which are executed on a multi-core architecture with limited local memory.

0830 **OPTIMIZING REMOTE ACCESSES FOR OFFLOADED KERNELS: APPLICATION TO HIGH-LEVEL SYNTHESIS FOR FPGA**
Christophe Alias[1], Alain Darte[2], Alexandru Plesco[1]
[1]INRIA, FR, [2]CNRS, FR

0900 **SEQUENTIALLY CONSTRUCTIVE CONCURRENCY - A CONSERVATIVE EXTENSION OF THE SYNCHRONOUS MODEL OF COMPUTATION**
Reinhard von Hanxleden[1], Michael Mendler[2], Joaquin Aguado[2], Björn Duderstadt[1], Insa Fuhrmann[1], Stephen Mercer[3], Christian Motika[1], Owen O'Brien[3]
[1]Kiel University, DE, [2]Bamberg University, DE, [3]National Instruments, US

0930 **FAST AND ACCURATE CACHE MODELING IN SOURCE-LEVEL SIMULATION OF EMBEDDED SOFTWARE**
Zhonglei Wang and Jörg Henkel
Karlsruhe Institute of Technology, DE

0945 **AUTOMATIC AND EFFICIENT HEAP DATA MANAGEMENT FOR LIMITED LOCAL MEMORY MULTICORE ARCHITECTURES**
Ke Bai and Aviral Shrivastava
Arizona State University, US

IPs **IP2-12, IP2-13**

1000 **EXHIBITION BREAK/IP2**

IP2 Interactive Presentations

Room – Salle de Reception 1000-1030

Interactive Presentations run simulatenously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP2-1 **AN EFFICIENT NETWORK-ON-CHIP ARCHITECTURE BASED ON ISOLATING LOCAL AND NON-LOCAL COMMUNICATIONS**
Vahideh Akhlaghi[1], Mehdi Kamal[1], Ali Afzali-Kusha[1], Massoud Pedram[2]
[1]University of Tehran, IR,
[2]University of Southern California, US

IP2-2 **SVR-NOC: A PERFORMANCE ANALYSIS TOOL FOR NETWORK-ON-CHIPS USING LEARNING-BASED SUPPORT VECTOR REGRESSION MODEL**
Zhiliang Qian[1], Da-Cheng Juan[2], Paul Bogdan[2], Chi-Ying Tsui[1], Diana Marculescu[2], Radu Marculescu[2]
[1]Hong Kong University of Science and Technology, HK,
[2]Carnegie Mellon University, US

IP2-3 **THE FUTURE OF GPGPU MICRO-ARCHITECTURAL PARAMETERS**
Cedric Nugteren, Gert-Jan van den Braak and Henk Corporaal
Eindhoven University of Technology, NL

IP2-4 **SYNCHRONIZING CODE EXECUTION ON ULTRA-LOWPOWER EMBEDDED MULTI-CHANNEL SIGNAL ANALYSIS PLATFORMS**
Ahmed Yasir Dogan, Jeremy Constantin, Ruben Braojos Lopez, Giovanni Ansaloni, Andreas Burg, David Atienza EPFL, CH

IP2-5 **USING SYNCHRONIZATION IN POWER-AWARE ACCELERATORS**
Ali Jooya and Amirali Baniasadi University of Victoria, CA

IP2-6 **MEMRISTOR PUFS: A NEW GENERATION OF MEMORY-BASED PHYSICALLY UNCLONABLE FUNCTIONS**
Unal Kocabas[1], Patrick Koeberl[2], Ahmad-Reza Sadeghi[3]
[1]Technische Universität Darmstadt, DE
[2]Intel, DE, [3]Technische Universität Darmstadt, DE and Fraunhofer SIT Darmstadt, DE

IP2-7 **WIRELESS SENSOR NETWORK SIMULATION FOR SECURITY AND PERFORMANCE ANALYSIS**
Álvaro Díaz[1], Pablo Sanchez[1], Juan Sancho[2], Juan Rico[2]
[1]University of Cantabria, ES, [2]TST Sistemas, ES

IP2-8 **PROCESS-VARIATION-AWARE IDDQ DIAGNOSIS FOR NANO-SCALE CMOS DESIGNS - THE FIRST STEP**
Chia-Ling (Lynn) Chang[1], Charles H.-P. Wen[1], Jayanta Bhadra[2]
[1]National Chiao Tung University, TW
[2]Freescale Semiconductor, US

IP2-9 **AUTOMATED DETERMINATION OF TOP LEVEL CONTROL SIGNALS**
Rohit Jain, Praveen Tiwari, Soumen Ghosh
Synopsys, IN

IP2-10 **AN EFFICIENT AND FLEXIBLE HARDWARE SUPPORT FOR ACCELERATING SYNCHRONIZATION OPERATIONS ON THE STHORM MANY-CORE ARCHITECTURE**
Farhat Thabet, Yves Lhuillier, Caaliph Andriamisaina, Jean-Marc Philippe and Raphael David CEA LIST, FR

IP2-11 **ELECTRICAL CALIBRATION OF SPRING-MASS MEMS CAPACITIVE ACCELEROMETERS**
Lingfei Deng[1], Vinay Kundur[1], Naveen Sai Jangala Naga[1], Muhlis Kenan Ozel[1], Ender Yilmaz[1], Sule Ozev[1], Bertan Bakkaloglu[1], Sayfe Kiaei[1], Divya Pratab[2], Tehmoor Dar[2]
[1]Arizona State University, US,
[2]Freescale Semiconductor, US

IP2-12 **SOFTWARE ENABLED WEAR-LEVELING FOR HYBRID PCM MAIN MEMORY ON EMBEDDED SYSTEMS**
Jingtong Hu[1], Qingfeng Zhuge[2], Chun Xue[3], Wei-Che Tseng[1], Edwin Sha[1]
[1]University of Texas at Dallas, US,
[2]Chongqing University, CN,
[3]City University of Hong Kong, HK

IP2-13 **PROBABILISTIC TIMING ANALYSIS ON CONVENTIONAL CACHE DESIGNS**
Leonidas Kosmidis[1], Charlie Curtsinger[2], Eduardo Quiñones[3], Jaume Abella[3], Emery Berger[2], Francisco Cazorla[4]
[1]Universitat Politècnica de Catalunya and Barcelona Supercomputing Center, ES,
[2]University of Massachusetts Amherst, US,
[3]Barcelona Supercomputing Center, ES
[4]Barcelona Supercomputing Center and and IIIA-CSIC, ES

6.1 SPECIAL DAY SESSION: EMBEDDED TUTORIAL - HW-SW Architecture Approaches to Energy-Efficiency

Room - Oisans 1100-1230

Organiser: Ahmed Jerraya - CEA-LETI-MINATEC, FR

Chair: Agnès Fritsch - Thales Group, FR
Co-Chair: Ahmed Jerraya - CEA-LETI-MINATEC, FR

Traditionally HW-SW interfaces are defined twice using two different models: one representing HW from a SW point of view, and one representing SW from a HW point of view. These separate views create a discontinuity in the design process and inevitably induces non-optimised designs from an energy-efficiency point of view. This embedded tutorial presents a HW view, a SW view, and an integrated HW-SW view to study the different approaches to energy efficiency

1100 **IC ARCHITECTURE APPROACHES TO ENERGY-EFFICIENCY**
Thomas Pflueger IBM, DE

1130 **SW ARCHITECTURE**
David Rusling Linaro, UK

1200 **HW-SW INTEGRATION FOR ENERGY-EFFICIENT/VARIABILITY-AWARE COMPUTING**
Gasser Ayad[1], Andrea Acquaviva[1], Enrico Macii[1], Brahim Sahbi[2] and Romain Lemaire[2]
[1]Politecnico di Torino, IT, [2]CEA-Leti, FR

1230 **LUNCH BREAK**

6.2 HOT TOPIC: Emerging Nanoscale Devices: A Booster for High Performance Computing

Room - Belle-Etoile 1100-1230

Organisers: Pierre-Emmanuel Gaillardon - EPFL, CH
Giovanni De Micheli - EPFL, CH

Chair: Giovanni De Micheli, EPFL, CH
Co-Chair: Ahmed Jerraya, CEA, LETI, Minatec, FR

As the semiconductor industry advances into the era of nanotechnology, the devices are expected to be scaled down to their physical and economic limits. These limitations require the industry to explore the use of novel materials and device structures able to replace the current CMOS transistors within the next few years. In this session, we elaborate on novel and emerging technologies, from advanced Silicon devices to carbon electronics, that can help pushing the Moore's Law beyond. We will detail the novel physical design techniques, architectural organizations and CAD tools identified to keep improving the performance of the computation structures, while maintaining an acceptable yield.

1100 **NEAR-THRESHOLD VOLTAGE DESIGN IN NANOSCALE CMOS**
Vivek De Intel, US

1122 **ULTRA-WIDE VOLTAGE RANGE DESIGNS IN FULLY-DEPLETED SILICON-ON-INSULATOR FET**
Edith Beigné[1], Philippe Flatresse[2], Bastien Giraud[1], Jean-Philippe Noel[2], Olivier Thomas[1], Anuj Grover[2], Thomas Benoist[1], Fady Abouzeid[2], Yvain Thonnart[1], Bertrand Pelloux-Prayer[2], Sébastien Bernard[1], Sylvain Clerc[2], Guillaume Moritz[1], Philippe Roche[2], Olivier Billoint[1], Julien Le Coz[2], Yves Maneglia[1], Sylvain Engels[2], Alexandre Valentian[1], Robin Wilson[2]
[1]CEA-LETI, Minatec, FR, [2]STMicroelectronics, FR

1145 **CARBON NANOTUBE CIRCUITS: OPPORTUNITIES AND CHALLENGES**
Hai Wei, Max Shulaker, Gage Hills, Hong-Yu Chen, Chi-Shuen Lee, Luckshitha Liyanage, Jie Jerry Zhang, H.-S. Philip Wong and Subhasish Mitra
Stanford University, US

1207 **VERTICALLY-STACKED DOUBLE-GATE NANOWIRE FETS WITH CONTROLLABLE POLARITY: FROM DEVICES TO REGULAR ASICS**
Pierre-Emmanuel Gaillardon, Luca Gaetano Amarù, Shashikanth Bobba, Michele De Marchi, Davide Sacchetto, Yusuf Leblebici and Giovanni De Micheli EPFL, CH

1230 **LUNCH BREAK**

6.3 Verification and Simulation Support for Architecture

Room - Stendhal 1100-1230

Chair: Valeria Bertacco, University of Michigan, US
Co-Chair: Elena Vatajelu, LIRMM, FR

With processor architectures becoming increasingly complex and concurrent, new verification ideas are needed to rescue them from being bug-ridden. This session addresses a number of key issues in this domain: simulation performance, correctness of concurrency, and of the models used to validate the software running on them. The session presents solutions to boost the performance of architectural simulators and cache simulation and to effectively verify memory transactions with respect to consistency.

1100 **ON-THE-FLY VERIFICATION OF MEMORY CONSISTENCY WITH CONCURRENT RELAXED SCOREBOARDS**
Leandro S. Freitas, Eberle A. Rambo and Luiz C. V. dos Santos
Federal University of Santa Catarina, BR

1130 **FAST CACHE SIMULATION FOR HOST-COMPILED SIMULATION OF EMBEDDED SOFTWARE**
Kun Lu, Daniel Mueller-Gritschneder and Ulf Schlichtmann
Technische Universitaet Muenchen, DE

1200 **A CRITICAL-SECTION-LEVEL TIMING SYNCHRONIZATION APPROACH FOR DETERMINISTIC MULTI-CORE INSTRUCTION-SET SIMULATIONS**
Fan-Wei Yu, Bo-Han Zeng, Yu-Hung Huang, Hsin-I Wu, Che-Rung Lee, Ren-Song Tsay
National Tsing Hua University, TW

1215 **MULTI-LEVEL PHASE ANALYSIS FOR SAMPLING SIMULATION**
Jiaxin Li[1], Weihua Zhang[1], Haibo Chen[2], Binyu Zang[1]
[1]Fudan University, CN,
[2]Shanghai Jiaotong University, CN

1230 **IP3-1**

1230 **LUNCH BREAK**

6.4 Design Space Exploration for Application Specific Architectures

Room - Chartreuse 1100-1230

Chair: Andreas Moshovos, University of Toronto, CA
Co-Chair Georgi Gaydadjiev, Chalmers University of Technology, SE

This session presents a collection of papers that advances design space exploration for application-specific customization. The first paper proposes an analytical meta-model for area and delay to predict the quality of the design points in co-processor synthesis leading to significant speed-up in the design space exploration process. The second paper designs an application-specific customization of memory hierarchy for multi-view video coding. The final paper in this session employs an analytical model to reduce the number of cycle-accurate simulations for exploration of many-core embedded platforms.

1100 **A META-MODEL ASSISTED COPROCESSOR SYNTHESIS FRAMEWORK FOR COMPILER/ARCHITECTURE PARAMETERS CUSTOMIZATION**
Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano
Politecnico Di Milano, IT

1130 **ENERGY-EFFICIENT MEMORY HIERARCHY FOR MOTION AND DISPARITY ESTIMATION IN MULTIVIEW VIDEO CODING**
Felipe Sampaio[1], Bruno Zatt[2], Muhammad Shafique[2], Luciano Agostini[3], Sergio Bampi[1], Jörg Henkel[2]
[1]Federal University of Rio Grande do Sul, BR
[2]Karlsruhe Institute of Technology, DE
[3]Federal University of Pelotas, BR

1200 **IMPROVING SIMULATION SPEED AND ACCURACY FOR MANY-CORE EMBEDDED PLATFORMS WITH ENSEMBLE MODELS**
Edoardo Paone[1], Nazanin Vahabi[1], Vittorio Zaccaria[1], Cristina Silvano[1], Diego Melpignano[2], Germain Haugou[2], Thierry Lepley[2]
[1]Politecnico di Milano, IT, [2]STMicroelectronics, FR

IPs **IP3-2, IP3-3, IP3-4**

1230 **LUNCH BREAK**

6.5 Reliable Multi-Processor Computing Systems Design

Room - Meije 1100-1230

Chair: Jose Ayala, Complutense University of Madrid, ES
Co-Chair Vincenzo Rana, EPFL, CH

This session tackles the problems of task mapping and allocation for latest multi-processor systems under possible error conditions. The first paper deals with task mapping to maximize the correct operation of multi-processor architectures under reliability constrained setups. The second paper proposes a new scheduling framework for processing systems that can adapt to different fault tolerance requirements. The third paper explores methods to use coarse-grained reconfigurable architectures in order to guarantee reliable system-level behavior, and the fourth paper explores the development of a configurable soft-error resilience approach to achieve reliable specific instruction-set processing architectures.

1100 **RELIABILITY-DRIVEN TASK MAPPING FOR LIFETIME EXTENSION OF NETWORKS-ON-CHIP BASED MULTIPROCESSOR SYSTEMS**
Anup Das, Akash Kumar and Bharadwaj Veeravalli
National University of Singapore, SG

1130 **A WORK-STEALING SCHEDULING FRAMEWORK SUPPORTING FAULT TOLERANCE**
Yizhuo Wang, Weixing Ji, Feng Shi and Qi Zuo
Beijing Institute of Technology, CN

1200 **A COST-EFFECTIVE SELECTIVE TMR FOR HETEROGENEOUS COARSE-GRAINED RECONFIGURABLE ARCHITECTURES BASED ON DFG-LEVEL VULNERABILITY ANALYSIS**
Takashi Imagawa, Hiroshi Tsutsui, Hiroyuki Ochi, and Takashi Sato
Kyoto University, JP

1215 **CSER: HW/SW CONFIGURABLE SOFT-ERROR RESILIENCY FOR APPLICATION SPECIFIC INSTRUCTION-SET PROCESSORS**
Tuo Li[1], Muhammad Shafique[2], Semeen Rehman[2], Swarnalatha Radhakrishnan[1], Roshan Ragel[1], Jude Angelo Ambrose[1], Jörg Henkel[2], Sri Parameswaran[1]
[1]University of New South Wales, AU
[2]Karlsruhe Institute of Technology, DE

IPs **IP3-5, IP3-6, IP3-7**

1230 **LUNCH BREAK**

6.6 HOT TOPIC: Energy-Efficient Design and Test Techniques for Future Multi-Core Systems

Room - Bayard 1100-1230

Organiser:
Krishnendu Chakrabarty - Duke University, US

Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE
Co-Chair: Paul Pop, Technical University of Denmark, DE

In this hot topic session, the speakers will describe new, far-reaching design methods and test techniques that achieve energy efficiency and low defect escapes in massively integrated single-chip computing platforms. By integrating design, design automation, and test content, this session will provide a holistic view of multi-core systems to DATE attendees.

1100 **ENERGY-EFFICIENT MULTICORE CHIP DESIGN THROUGH CROSS-LAYER APPROACH**
Paul Wettin[1], Jacob Murray[1], Partha Pratim Pande[1], Behrooz Shirazi[1], Amlan Ganguly[2]
[1]Washington State University, US
[2]Rochester Institute of Technology, US

1120 **BREAKING THE ENERGY BARRIER IN FAULT-TOLERANT CACHES FOR MULTICORE SYSTEMS**
Paul Ampadu[1], Meilin Zhang[1], Vladimir Stojanovic[2]
[1]University of Rochester, US
[2]Massachusetts Institute of Technology, US

1140 **TESTING FOR SOCS WITH ADVANCED STATIC AND DYNAMIC POWER-MANAGEMENT CAPABILITIES**
Chrysovalantis Kavousianos[1] and Krishnendu Chakrabarty[2]
[1]University of Ioannina, GR, [2]Duke University, US

1200 **TOWARDS ADAPTIVE TEST OF MULTI-CORE RF SOCS**
Rajesh Mittal, Lakshmanan Balasubramanian, Chethan Kumar Y. B., V. R Devanathan, Mudasir Kawoosa and Rubin A. Parekhji - Texas Instruments, IN

1230 **LUNCH BREAK**

6.7 Model-Based Design and Verification for Embedded Systems

Room - Les Bans 1100-1230

Chair: Wang Yi, Uppsala University, SE
Co-Chair: Saddek Bensalem, Verimag, FR

This session includes four papers. The first and the third papers present two different techniques to solve design optimization problems for systems with multiple conflicting constraints on timing, buffer, and energy.

The second and the last papers address issues on performance bottlenecks and weakly real-time guarantees in multi-core systems as well as real-time systems in the presents of sporadic workload bursts.

1100 **A SATISFIABILITY APPROACH TO SPEED ASSIGNMENT FOR DISTRIBUTED REAL-TIME SYSTEMS**
Pratyush Kumar, Devesh B. Chokshi and Lothar Thiele
ETH Zurich, CH

1130 **DATA MINING MPSOC SIMULATION TRACES TO IDENTIFY CONCURRENT MEMORY ACCESS PATTERNS**
Sofiane Lagraa, Alexandre Termier and Frédéric Pétrot
Grenoble Institute of Technology, FR

1200 **MODEL-BASED ENERGY OPTIMIZATION OF AUTOMOTIVE CONTROL SYSTEMS**
Joost-Pieter Katoen[1], Thomas Noll[1], Thomas Santen[2], Dirk Seifert[2], Hao Wu[1]
[1]RWTH Aachen University, DE, [2]Microsoft Research, DE

1215 **FORMAL ANALYSIS OF SPORADIC BURSTS IN REAL-TIME SYSTEMS**
Sophie Quinton, Mircea Negrean and Rolf Ernst
TU Braunschweig, DE

1230 **LUNCH BREAK**

6.8 EXHIBITION THEATRE: Silicon Europe – Leading European Regions Join Forces

Room - Lesdigiueres (Exhibition Theatre) 1100-1230

Organiser: Jürgen Haase - edacentrum, DE

Moderator: Thomas Reppe - Silicon Saxony, DE

Four of the leading European micro- and nanoelectronics regions are joining their research, development and production expertise to form the transnational, research-driven cluster "Silicon Europe – The Leaders for Energy Efficient ICT Electronics". The cluster partners from Germany, Belgium, France and the Netherlands are linked by a common goal: They aim to secure and expand Europe's position as the world's leading center for energy efficient micro- and nanoelectronics and information and communications technology (ICT). In order to reach this goal, Silicon Saxony (Dresden/Germany), DSP Valley (Belgium), Minalogic (Grenoble/France) and High Tech NL (Eindhoven/Netherlands) are cooperating in research, development and business expertise. Together they represent about 800 research institutes and companies, which account for more than 150,000 jobs; among the companies are global market leaders such as Philips, NXP, Globalfoundries, Infineon, STMicroelectronics, Schneider Electric und Thales. This makes Silicon Europe one of the largest technology clusters of the world.

1100 **SILICON EUROPE - CLUSTER ALLIANCE FOR EUROPEAN MICRO- AND NANOELECTRONICS INDUSTRY - TOPICS, CHALLENGES, OPPORTUNITIES**
Thomas Reppe, Silicon Saxony, DE

1120 **MINALOGIC: FROM RESEARCH TO INDUSTRY**
Jean Chabbal, Minalogic, FR

1135 **SILICON SAXONY - A HIGH TECH LOCATION OF GREAT DIVERSITY**
Andreas Brüning, Silicon Saxony, DE

1150 **THE DUTCH SEMICON CLUSTER: A COMPLETE VALUE CHAIN**
Ben van der Zon, High Tech NL, NL

1205 **DSP VALLEY - REGION OF EXCELLENCE IN EMBEDDED SIGNAL PROCESSING SYSTEMS DESIGN**
Peter Simkens, DSP Valley, BE

1220 **PANEL**
Thomas Reppe and Andreas Brüning, Silicon Saxony, DE
Jean Chabbal, Minalogic, FR
Ben van der Zon, High Tech NL, NL
Peter Simkens, DSP Valley, BE

1230 **LUNCH BREAK**

7.0 SPECIAL DAY 1 LUNCH-TIME KEYNOTE

Room - Oisans 1330-1400

1330 **ENERGY-EFFICIENT COMPUTING**
John Goodacre, ARM, UK

Since the first mobile computer, power efficiency was a key measure for success. As the need for performance ever increases, the energy cost of performance has metric well beyond just the life of the battery in mobile. Energy efficiency is now the driver in most consumer products, the compute density of a server, and has become the primary limit in the delivery of high performance. During this talk we will consider the various power related limitations of compute while discovering how the techniques and new capabilities introduced into mobile computing also bring the flexibility to address the limitations of the traditional computing approach.

1400 **EXHIBITION BREAK**

7.1 SPECIAL DAY 1 HOT TOPIC - Many-Core SoC Approaches to Energy-Efficiency

Room - Oisans 1430-1600

Organiser:
Ahmed Jerraya - CEA-LETI-MINATEC, FR

Chair: Marc Duranton, CEA, FR
Co-Chair: Ahmed Jerraya, CEA-LETI-MINATEC, FR

Moderators:
Marc Duranton, CEA, FR
Ahmed Jerraya, CEA-LETI-MINATEC, FR

The evolution of the semiconductor industry is allowing intensive computing on a single chip through heterogeneous and homogeneous architectures. This increase in compute density on a single chip is both a threat and an opportunity for energy-efficiency. This Hot-Topic Session presents different many-core SoC approaches to improve energy-efficiency.

1430 **DEVELOPMENT OF LOW POWER MANY-CORE SOC FOR MULTIMEDIA APPLICATIONS**
Takashi Miyamori, Hui Xu, Takeshi Kodaka, Hiroyuki Usui, Toru Sano and Jun Tanabe
Toshiba, JP

1450 **SOC LOW-POWER PRACTICES FOR WIRELESS APPLICATIONS**
Nicolas Darbel and Stephane Lecomte, ST-Ericsson, FR

1510 **FUTURE LOW-POWER SOC**
Koji Inoue, Kyushu University, JP

1530 **3D INTEGRATION FOR POWER-EFFICIENT COMPUTING**
Denis Dutoit, Eric Guthmuller and Ivan Miro-Panades
CEA-Leti, FR

1600 **EXHIBITION BREAK/IP3**

7.2 Formal Verification Algorithms and Models

Room - Belle-Etoile 1430-1600

Chair: Christoph Scholl, University of Freiburg, DE
Co-Chair: Jason Baumgartner, IBM, US

The session covers an application of formal methods to the verification of Transactional Memories as well as techniques to broaden the scope of modern core verification techniques. The first paper presents a formal model for Hybrid Transactional Memories and a correctness proof based on this formalization. The second paper extends IC3 / PDR (a recent, highly successful method for model checking by incrementally building inductive invariants) from Boolean formulas to quantifier-free formulas with bit vectors. Finally, the third paper presents a method for semi-canonical labeling And Inverter Graphs which aims at speeding-up sequential verification by identifying isomorphic structures.

1430 **VERIFYING SAFETY AND LIVENESS FOR THE FLEXTM HYBRID TRANSACTIONAL MEMORY**
Parosh Abdulla[1], Sandhya Dwarkadas[2], Ahmed Rezine[3], Arrvindh Shriraman[4], Yunyun Zhu[1]
[1]Uppsala University, SE [2]Rochester University, US, [3]Linköping University, SE [4]Simon Fraser University, CA

1500 **QF_BV MODEL CHECKING WITH PROPERTY DIRECTED REACHABILITY**
Tobias Welp[1] and Andreas Kuehlmann[2]
[1]University of California at Berkeley, US, [2]Coverity, US

1530 **A SEMI-CANONICAL FORM FOR SEQUENTIAL AIGS**
Alan Mishchenko[1], Niklas Een[1], Robert Brayton[1], Michael Case[2], Pankaj Chauhan[2], Nikhil Sharma[2]
[1]UC Berkeley, US, [2]Calypto Design Systems, US

IPs **IP3-8, IP3-9, IP3-10**

1600 **EXHIBITION BREAK/IP3**

7.3 Dynamic Reconfiguration

Room - Stendhal 1430-1600

Chair: Diana Goehringer, Karlsruhe Institute of Technology, DE
Co-Chair: Fabrizio Ferrandi, Politecnico di Milano, IT

In this session dynamic reconfiguration techniques are presented and exploited in new tools and hardware architectures. The first paper deals with an algorithm for prefetching dynamic partial bit streams in hardware platforms that support dynamic partial reconfiguration.The second paper introduces a new tool performing dynamic circuit synthesis for designing reconfigurable multi-mode circuits. The two short papers propose first a generic binary format for VLIW processors with adaptive issue-widths and second a modular IP-core based approach to simplify the design of run-time reconfigurable systems.

1430 **DYNAMIC CONFIGURATION PREFETCHING BASED ON PIECEWISE LINEAR PREDICTION**
Adrian Lifa, Petru Eles and Zebo Peng
Linköping University, SE

1500 **AN AUTOMATIC TOOL FLOW FOR THE COMBINED IMPLEMENTATION OF MULTI-MODE CIRCUITS**
Brahim Al Farisi[1], Karel Bruneel[1], João M. P. Cardoso[2], Dirk Stroobandt[1]
[1]University of Ghent, BE, [2]University of Porto, PT

1530 **SUPPORT FOR DYNAMIC ISSUE WIDTH IN VLIW PROCESSORS USING GENERIC BINARIES**
Anthony Brandon and Stephan Wong
TUDelft, NL

1545 **THE RECOBLOCK SOC PLATFORM:A FLEXIBLE ARRAY OF REUSABLE RUN-TIME-RECONFIGURABLE IP-BLOCKS**
Byron Navas, Ingo Sander and Johnny Öberg
KTH Stockholm, SE

IPs **IP3-11, IP3-12**

1600 **EXHIBITION BREAK/IP3**

7.4 Emerging Memory

Room - Chartreuse 1430-1600

Chair: Ian O'Connor, Lyon Institute of Nanotechnology, FR
Co-Chair: Siddharth Garg, University of Waterloo, CA

This session has three papers discussing STT-MRAM based Cache, Dual-Port Acces STT-MRAM, and NAND FLASH storage with PRAM/DRAM Hybrid Buffer.

1430 **OAP: AN OBSTRUCTION-AWARE CACHE MANAGEMENT POLICY FOR STT-RAM LAST-LEVEL CACHES**
Jue Wang, Xiangyu Dong, Yuan Xie
Pennsylvania State University, US

1500 **STT-RAM CELL DESIGN SUPPORTING DUAL-PORT ACCESSES**
Xiuyuan Bi[1], Mohamed Anis Weldon[2], Hai Li[1]
[1]University of Pittsburgh, US,
[2]Polytechnic Institute of New York University, US

1530 **LOW COST POWER FAILURE PROTECTION FOR MLC NAND FLASH STORAGE SYSTEMS WITH PRAM/DRAM HYBRID BUFFER**
Jie Guo, Jun Yang, Youtao Zhang and Yiran Chen
University of Pittsburgh, US

IPs **IP3-13, IP3-14, IP3-15, IP3-16**

1600 **EXHIBITION BREAK/IP3**

7.5 Energy-efficient architectures and software design for power-constrained systems

Room - Meije 1430-1600

Chair: Geoff Merrett, University of Southampton, UK
Co-Chair: Gangadhar Garipelli, EPFL, CH

This session proposes new solutions for energy-efficient hardware design and software architectures targetting highly power-constrained environments. The first two papers in this session address energy-optimized architectures and algorithms for distributed systems operating in smart buildings and cars. The last two papers present the design of low-power signal acquisition approaches and innovative processing architectures for electrocorticographic (ECoG) and electrocardiogram (ECG) biosignals analysis.

1430 **OPTIMAL CONTROL OF A GRID-CONNECTED HYBRID ELECTRICAL ENERGY STORAGE SYSTEM FOR HOMES**
Yanzhi Wang[1], Xue Lin[1], Sangyoung Park[2], Naehyuck Chang[2], Massoud Pedram[1]
[1]University of Southern California, US
[2]Seoul National University, KR

1500 **RADAR SIGNATURE IN MULTIPLE TARGET TRACKING SYSTEM FOR DRIVER ASSISTANT APPLICATION**
Haisheng Liu[1] and Smail Niar[2]
[1]Nantong University, FR,
[2]Universite de Valenciennes, FR

1515 **DEVELOPMENT OF A FULLY IMPLANTABLE RECORDING SYSTEM FOR ECOG SIGNALS**
Jonas Pistor, Janpeter Hoeffmann, David Rotermund, Elena Tolstosheeva, Tim Schellenberg, Dmitriy Boll, Victor Gordillo-Gonzales, Sunita Mandon, Dagmar Peters-Drolshagen, Andreas Kreiter, Martin Schneider, Walter Lang, Klaus Pawelzik, and Steffen Paul
University of Bremen, DE

1530 **A METHODOLOGY FOR EMBEDDED CLASSIFICATION OF HEARTBEATS USING RANDOM PROJECTIONS**
Rubén Braojos, Giovanni Ansaloni and David Atienza
École Polytechnique Fédérale de Lausanne, CH

IPs **IP3-17, IP3-18, IP3-19, IP3-20**

1600 **EXHIBITION BREAK/IP3**

7.6 On-Line Approaches Towards Processor Resilience

Room - Bayard 1430-1600

Chair: Yiorgos Makris, University of Texas, Dallas, US
Co-Chair: Xavier Vera, Intel, ES

This session brings the audience papers dealing with on-line detection and resilience for processors by task replication and redundant execution.

1430 **EFFICIENT SOFTWARE BASED FAULT TOLERANCE APPROACH ON MULTICORE PLATFORMS**
Hamid Mushtaq, Zaid Al-Ars and Koen Bertels
TU Delft, NL

1500 **USING EXPLICIT OUTPUT COMPARISONS FOR FAULT TOLERANT SCHEDULING (FTS) ON MODERN HIGH-PERFORMANCE PROCESSORS**
Yue Gao, Sandeep K. Gupta and Melvin Breuer
University of Southern California, US

1530 **LOW COST PERMANENT FAULT DETECTION USING ULTRA-REDUCED INSTRUCTION SET CO-PROCESSORS**
Sundaram Ananthanarayan[1], Siddharth Garg[2], Hiren Patel[2]
[1]Stanford University, US, [2]University of Waterloo, CA

IPs **IP3-21, IP3-22**

1600 **EXHIBITION BREAK/IP3**

7.7 EMBEDDED TUTORIAL: From multi-core SoC to scale-out processors

Room - Les Bans 1430-1600

Organiser: Marcello Coppola - STMicroelectronics, FR

Chair: Marcello Coppola, STMicroelectronics, FR
Co-Chair: Luca Fanucci, University of Pisa, IT

Advanced computing is generally recognized as a way to accelerate progress in scientific research in the 21st Century. Heterogeneous multicore architecture has long been accepted within embedded computing the way to deliver improved performance and subsequent improved power efficiency. However to build a usable system within an affordable power budget both architectures and applications will need to change dramatically. These changes will impact all scales of computing from single MPSoC to racks to supercomputers. The entire computing industry faces the same power, memory, concurrency and programmability challenges. While Mobile, Consumer systems target the best tradeoff between area, performance and power, scale-out datacenters have additional challenges, notably performance per total cost of ownership (performance/TCO). Emerging applications (e.g., data serving and web search) that run in these datacenters operate on vast datasets that are not accommodated by on-die caches of existing server chips. Large caches reduce the die area available for cores and lower performance through long access latency when instructions are fetched. In this embedded tutorial, we will introduce the next generation multicore ARM based SoC to address the challenge of maintaining the homogeneity of the software architecture while extending to the benefits of heterogeneity. Then we will introduce the future evolutions of multi-core architectures in mobile and consumer SoCs, describing how gates will be used to meet the new application requirements. Finally, we introduce a methodology for designing scalable and efficient scale-out server processors that facilitates the design of optimal multi-core configurations, which divide the server processor's real estate into performance-optimal modules that couple many lean cores with a small last-level cache to maximize throughput per area given a power budget.

1430 **THE 64BITS MULTICORE ARM BASED SOC**
John Goodacre - ARM, UK

1500 **VIRTICAL: THE VIRTUALIZATION READY SoC PLATFORM FOR MOBILE AND CONSUMER**
George Kornaros[1] and Marcello Coppola[2]
[1]TEI, GR, [2]STMicroelectronics, FR

1530 **SCALE OUT PROCESSORS**
Babak Falsafi EPFL, CH

1600 **EXHIBITION BREAK/IP3**

IP3 Interactive Presentations

Room – Salle de Reception 1600-1630

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP3-1 **HYPERVISED TRANSIENT SPICE SIMULATIONS OF LARGE NETLISTS & WORKLOADS ON MULTI-PROCESSOR SYSTEMS**
Grigorios Lyras, Dimitrios Rodopoulos, Antonis Papanikolaou and Dimitrios Soudris
NTUA-ECE-MicroLab, GR

IP3-2 **STATICALLY-SCHEDULED APPLICATION-SPECIFIC PROCESSOR DESIGN: A CASE-STUDY ON MMSE MIMO EQUALIZATION**
Mostafa Rizk[1, 2], Amer Baghdadi[1], Michel Jezequel[1], Yasser Mohana[2], Youssef Atat[2]
[1]Telecom Bretagne, FR, [2]Lebanese University, LB

IP3-3 **EXPLORING RESOURCE MAPPING POLICIES FOR DYNAMIC CLUSTERING ON NOC-BASED MPSOCS**
Gustavo Girao, Thiago Santini and Flavio Wagner
Federal University of Rio Grande do Sul, BR

IP3-4 **CHARACTERIZING THE PERFORMANCE BENEFITS OF FUSED CPU/GPU SYSTEMS USING FUSIONSIM**
Vitaly Zakharenko[1], Tor Aamodt[2], Andreas Moshovos[1]
[1]University of Toronto, CA,
[2]University of British Columbia, CA

IP3-5 **RELIABILITY ANALYSIS FOR INTEGRATED CIRCUIT AMPLIFIERS USED IN NEURAL MEASUREMENT SYSTEMS**
Nico Hellwege, Nils Heidmann, Dagmar Peters-Drolshagen and Steffen Paul University of Bremen, DE

IP3-6 **ON-LINE TESTING OF PERMANENT RADIATION EFFECTS IN RECONFIGURABLE SYSTEMS**
Luca Cassano[1], Dario Cozzi[2], Sebastian Korf[2], Jens Hagemeyer[2], Mario Porrmann[2], Luca Sterpone[3]
[1]University of Pisa, IT, [2]Bielefeld University, DE,
[3]Politecnico di Torino, IT

IP3-7 **AN APPROACH FOR REDUNDANCY IN FLEXRAY NETWORKS USING FPGA PARTIAL RECONFIGURATION**
Shanker Shreejith[1], Kizheppatt Vipin[1], Suhaib A Fahmy[1], Martin Lukasiewycz[2]
[1]Nanyang Technological University, SG, [2]TUM CREATE, SG

IP3-8 **FAST CONE-OF-INFLUENCE COMPUTATION AND ESTIMATION IN PROBLEMS WITH MULTIPLE PROPERTIES**
Carmelo Loiacono[1], Marco Palena[1], Paolo Pasini[1], Denis Patti[1], Stefano Quer[1], Stefano Ricossa[1], Danilo Vendraminetto[1], Jason Baumgartner[2]
[1]Politecnico di Torino, IT, [2]IBM Research, US

IP3-9 **USING CUBES OF NON-STATE VARIABLES WITH PROPERTY DIRECTED REACHABILITY**
John Backes and Marc Riedel
University of Minnesota, US

IP3-10 **BRIDGING THE GAP BETWEEN DUAL PROPAGATION AND CNF-BASED QBF SOLVING**
Alexandra Goultiaeva[1], Martina Seidl[2], Armin Biere[2]
[1]University of Toronto, CA,
[2]Johannes Kepler University, AT

IP3-11 **DANCE: DISTRIBUTED APPLICATION-AWARE NODE CONFIGURATION ENGINE IN SHARED RECONFIGURABLE SENSOR NETWORKS**
Chih-Ming Hsieh, Zhonglei Wang and Jörg Henkel
Karlsruhe Institute of Technology, DE

IP3-12 **HYBRID INTERCONNECT DESIGN FOR HETEROGENEOUS HARDWARE ACCELERATORS**
Cuong Pham-Quoc[1], Jan Heisswolf[2], Stephan Werner[2], Zaid Al-Ars[1], Jürgen Becker[2], Koen Bertels[1]
[1]Delft University of Technology, NL
[2]Karlsruhe Institute of Technology, DE

IP3-13 **SPAC: A SEGMENT-BASED PARALLEL COMPRESSION FOR BACKUP ACCELERATION IN NONVOLATILE PROCESSORS**
Xiao Sheng, Yiqun Wang, Yongpan Liu and Huazhong Yang
Tsinghua University, CN

IP3-14 **THE DESIGN OF SUSTAINABLE WIRELESS SENSOR NETWORK NODE USING SOLAR ENERGY AND PHASE CHANGE MEMORY**
Ping Zhou[1], Youtao Zhang[2], Jun Yang[2]
[1]Intel, US [2]Univ. of Pittsburgh, US

IP3-15 **OPTICAL LOOK UP TABLE**
Zhen Li, Sébastien Le Beux, Christelle Monat, Xavier Letartre and Ian Oconnor
Lyon Institute of Nanotechnology, FR

IP3-16 **A VERILOG-A MODEL FOR RECONFIGURABLE LOGIC GATES BASED ON GRAPHENE PN-JUNCTIONS**
Sandeep Miryrala, Mehrdad Montazeri, Andrea Calimera, Enrico Macii and Massimo Poncino
Politecnico di Torino, IT

IP3-17 **A SURVEY OF MULTI-SOURCE ENERGY HARVESTING SYSTEMS**
Alex S. Weddell[1], Michele Magno[2], Davide Brunelli[3], Geoff V. Merrett[1], Bashir M. Al-Hashimi[1], Luca Benini[2]
[1]University of Southampton, UK,
[2]University of Bologna, IT,
[3]University of Trento, IT

IP3-18 **CAPITAL COST-AWARE DESIGN AND PARTIAL SHADING-AWARE ARCHITECTURE OPTIMIZATION OF A RECONFIGURABLE PHOTOVOLTAIC SYSTEM**
Yanzhi Wang[1], Xue Lin[1], Jaemin Kim[2], Naehyuck Chang[2], Massoud Pedram[1]
[1]University of Southern California, US
[2]Seoul National University, KR

IP3-19 **AN ULTRA-LOW POWER HARDWARE ACCELERATOR ARCHITECTURE FOR WEARABLE COMPUTERS USING DYNAMIC TIME WARPING**
Reza Lotfian and Roozbeh Jafari
University of Texas at Dallas, US

IP3-20 **EFFICIENT CACHE ARCHITECTURES FOR RELIABLE HYBRID VOLTAGE OPERATION USING EDC CODES**
Bojan Maric[1, 2], Jaume Abella[2], Mateo Valero[1, 2]
[1]Barcelona Supercomputing Center, ES,
[2]Universitat Politecnica de Catalunya, ES

IP3-21 **IMPROVING FAULT TOLERANCE USING HARDWARE-SOFTWARE-CO-SYNTHESIS**
Heinz Riener[1], Stefan Frehse[1], Goerschwin Fey[2]
[1]University Bremen, DE, [2]German Aerospace Center, DE

IP3-22 **A DYNAMIC SELF-ADAPTIVE CORRECTION METHOD FOR ERROR RESILIENT APPLICATION**
Yan Luming, Liang Huaguo, Huang Zhengfeng
Hefei University of Technology, CN

8.1 SPECIAL DAY 1 HOT TOPIC - Fabrication Technology Approaches to Energy-Efficiency

Room - Oisans 1700-1830

Organiser/Chair:
Ahmed Jerraya, CEA-LETI-MINATEC, FR

SoC designs integrate an increasing number of heterogeneous programmable units (CPU, GPU, ASIP sub-systems), sophisticated interconnect, innovative memory architecture, and are using energy-efficient libraries that target advanced fabrication process technologies. This Hot-Topic Session presents the key challenges for aligning the most advanced fabrication technologies, FDSOI with circuit and architecture technologies to master energy-efficiency.

1700 **UTBB FD-SOI: A PROCESS/DESIGN SYMBIOSIS FOR BREAKTHROUGH ENERGY-EFFICIENCY**
Philippe Magarshack, Philippe Flatresse, and Giorgio Cesana
ST Microelectronics, FR

1720 **WIRELESS INTERCONNECT FOR BOARD AND CHIP LEVEL**
Gerhard Fettweis, Najeeb ul Hassan, Lukas Landau and Erik Fischer
TU Dresden, DE

1740 **ENERGY-EFFICIENT LIBRARIES**
Yannick Nevers
ARM, FR

1800 **FUTURE MEMORY AND INTERCONNECT TECHNOLOGIES**
Yuan Xie
Penn State University, US

1830 **CLOSE**

8.2 Scheduling for Real-Time Embedded Systems

Room - Belle-Etoile 1700-1830

Chair: Wido Kruijtzer, Synopsys, NL
Co-Chair: Jan Madsen, Technical University of Denmark, DK

The first paper addresses the challenge of integrating a safety-critical real-time system consisting of a set of single cores into a multi-core system, with the aim to reduce recertification cost. The second paper presents a scheduling approach for multiple media streams, efficiently utilizing available resources. The third paper presents a methodology for the priority assignment of processes and messages in event-triggered systems with tight end-to-end real-time deadlines.

1700 **OPTIMIZED SCHEDULING OF MULTI-IMA PARTITIONS WITH EXCLUSIVE REGION FOR SYNCHRONIZED REAL-TIME MULTI-CORE SYSTEMS**
Jung-Eun Kim[1], Man-Ki Yoon[1], Sungjin Im[2], Richard Bradford[3], Lui Sha[1]
[1]University of Illinois at Urbana-Champaign, US, [2]Duke University, US, [3]Rockwell Collins, US

1730 **QUALITY-AWARE MEDIA SCHEDULING ON MPSoC PLATFORMS**
Deepak Gangadharan[1], Samarjit Chakraborty[2], Roger Zimmermann[3]
[1]DTU Informatics, DK, [2]TU Munich, DE, [3]University of Singapore, SG

1800 **PRIORITY ASSIGNMENT FOR EVENT-TRIGGERED SYSTEMS USING MATHEMATICAL PROGRAMMING**
Martin Lukasiewycz[1], Sebastian Steinhorst[1], Samarjit Chakraborty[2]
[1]TUM CREATE, SG, [2]TUM, DE

IPs **IP4-1, IP4-2**

1830 **CLOSE**

8.3 Logic Synthesis Techniques

Room - Stendhal 1700-1830

Chair: Michel Berkelaar, Delft University of Technology, NL
Co-Chair: Jordi Cortadella, Universitat Politècnica Catalunya, ES

The first paper of this session presents a new multi-level optimization technique based on Boolean Relations. The second paper proposes a methodology to incorporate human intuition into Engineering Change Orders. The third paper describes a retiming technique for Soft-Error optimization.

1700 **MINIMIZATION OF P-CIRCUITS USING BOOLEAN RELATIONS**
Anna Bernasconi[1], Valentina Ciriani[2], Gabriella Trucco[2], Tiziano Villa[3]
[1]Universita' di Pisa, IT,
[2]Universita' degli Studi di Milano, IT,
[3]Universita' degli Studi di Verona, IT

1730 **INTUITIVE ECO SYNTHESIS FOR HIGH PERFORMANCE CIRCUITS**
Haoxing Ren[1], Ruchir Puri[1], Lakshmi Reddy[1], Smita Krishnaswamy[2], Cindy Washburn[1], Joel Earl[1], Joachim Keinert[1]
[1]IBM, DE, [2]Columbia University, US

1800 **RETIMING FOR SOFT ERROR MINIMIZATION UNDER ERROR-LATCHING WINDOW CONSTRAINTS**
Yinghai Lu[1] and Hai Zhou[2]
[1]Synopsys, US, [2]Northwestern University, US

IPs **IP4-3, IP4-4, IP4-5**

1830 **CLOSE**

8.4 High-Speed Robust NoCs

Room - Chartreuse 1700-1830

Chair: Luca Carloni, Columbia University, Us
Co-Chair: Georgios Dimitrakopoulos, Thrace University, GR

This session explores the challenges and opportunities offered by current and future manufacturing technologies. The first paper proposes a cutting-edge, extremely-high-frequency implementation. The other two papers take steps to combat aging effects due to NBTI phenomena.

1700 **EXPLORING TOPOLOGIES FOR A SOURCE-SYNCHRONOUS RING-BASED NETWORK-ON-CHIP**
Ayan Mandal, Sunil Khatri and Rabi Mahapatra
Texas A&M University, US

1730 **PROACTIVE AGING MANAGEMENT IN HETEROGENEOUS NoCs THROUGH A CRITICALITY-DRIVEN ROUTING APPROACH**
Dean Michael Ancajas, Koushik Chakraborty and Sanghamitra Roy
Utah State University, US

1800 **SENSOR-WISE METHODOLOGY TO FACE NBTI STRESS OF NoC BUFFERS**
Davide Zoni and William Fornaciari
Politecnico di Milano, IT

IPs **IP4-6, IP4-7**

1830 **CLOSE**

8.5 Industrial Experiences with Embedded System Design

Room - Meije 1700-1830

Chair: Roberto Zafalon, ST Microelectronics, IT
Co-Chair: Ralf Pferdmenges, Infineon Technologies, DE

This session feature six industrial research and practice cases for the design of embedded systems. Attendees will learn about future research demands and latest developments in design automation and embedded software.

1700 **DESIGNING TIGHTLY-COUPLED EXTENSION UNITS FOR THE STxP70 PROCESSOR**
Yves Janin, Valérie Bertin, Hervé Chauvet, Thomas Deruyter, Christophe Eichwald, Olivier-André Giraud, Vincent Lorquet and Thomas Thery
STMicroelectronics, FR

1715 **FAST AND ACCURATE METHODOLOGY FOR POWER ESTIMATION AND REDUCTION OF PROGRAMMABLE ARCHITECTURE**
Erwan Piriou[1], Raphael David[1], Fahim Rahim[2] and Solaiman Rahim[3]
[1]CEA LIST, FR, [2]Atrenta, FR, [3]Atrenta, US

1730 **A GATE LEVEL METHODOLOGY FOR EFFICIENT STATISTICAL LEAKAGE ESTIMATION IN COMPLEX 32nm CIRCUITS**
Smriti Joshi[1], Anne Lombardot[1], Marc Belleville[2], Edith Beigne[2] and Stephane Girard[3]
[1]ST Microelectronics FR, [2]CEA, FR, [3]INRIA, FR

1745 **A NEAR-FUTURE PREDICTION METHOD FOR LOW POWER CONSUMPTION ON A MANY-CORE PROCESSOR**
Takeshi Kodaka, Akira Takeda, Shunsuke Sasaki, Akira Yokosawa, Toshiki Kizu, Takahiro Tokuyoshi, Hui Xu, Toru Sano, Hiroyuki Usui, Jun Tanabe, Takashi Miyamori and Nobu Matsumoto
Toshiba, JP

1800 **TIME- AND ANGLE-TRIGGERED REAL-TIME KERNEL FOR POWERTRAIN APPLICATIONS**
Damien Chabrol[1], Didier Roux[1], Vincent David[2], Mathieu Jan[2], Moha Ait Hmid[2], Gilles Zeppa[3] and Patrice Oudin[3]
[1]Krono-Safe, FR, [2]CEA LIST, FR,
[3]Delphi Diesel Systems, FR

1815 **AN EXTREMELY COMPACT JPEG ENCODER FOR ADAPTIVE EMBEDDED SYSTEMS**
Josef Schneider and Sri Parameswaran
UNSW, AU

1830 **CLOSE**

8.6 DfT Methods

Room - Bayard 1700-1830

Chair: Peter Harrod, ARM, UK
Co-Chair: Luigi Dilillo, LIRMM, FR

This session deals with DfT for new design techniques and strategies seen in today's IC manufacturing. Furthermore, algorithmic optimizations to improve test and diagnosis are presented.

1700 **NON-INVASIVE PRE-BOND TSV TEST USING RING OSCILLATORS AND MULTIPLE VOLTAGE LEVELS**
Sergej Deutsch and Krishnendu Chakrabarty Duke University, US

1730 **LFSR SEED COMPUTATION AND REDUCTION USING SMT-BASED FAULT-CHAINING**
Dhrumeel Bakshi and Michael Hsiao Virginia Tech, US

1800 **SCAN DESIGN WITH SHADOW FLIP-FLOPS FOR LOW PERFORMANCE OVERHEAD AND CONCURRENT DELAY FAULT DETECTION**
Sébastien Sarrazin[1], Samuel Evain[1], Lirida Alves de Barros Naviner[2], Yannick Bonhomme[1] and Valentin Gherman[1]
[1]CEA-LIST, FR, [2]Telecom ParisTech, FR

1815 **ON CANDIDATE FAULT SETS FOR FAULT DIAGNOSIS AND DOMINANCE GRAPHS OF EQUIVALENCE CLASSES**
Irith Pomeranz Purdue University, US

IPs **IP4-8**

1830 **CLOSE**

8.7 Monitoring and Control of Cyber Physical Systems

Room - Les Bans 1700-1830

Chair: Rolf Ernst, Technische Universität Braunschweig, DE
Co-Chair: Haibo Zeng, McGill University, CA

Cyber-physical systems deal with the tight integration of computers and physical processes, with control and communication as enabling technologies. The integrative aspect is present in all papers, of which the third one focuses on communications, the fourth and fifth ones on controls, and the first two on a combination thereof.

1700 **CONTROL-QUALITY DRIVEN DESIGN OF CYBER-PHYSICAL SYSTEMS WITH ROBUSTNESS GUARANTEES**
Amir Aminifar[1], Petru Eles[1], Zebo Peng[1] and Anton Cervin[2]
[1]Linköping University, SE, [2]Lund University, SE

1730 **COMPOSITIONAL ANALYSIS OF SWITCHED ETHERNET TOPOLOGIES**
Reinhard Schneider, Licong Zhang, Dip Goswami, Alejandro Masrur and Samarjit Chakraborty Technical University of Munich, De

1745 **SUPERVISOR SYNTHESIS FOR CONTROLLER UPGRADES**
Johannes Kloos and Rupak Majumdar MPI-SWS, DE

1800 **EVENT DENSITY ANALYSIS FOR EVENT TRIGGERED CONTROL SYSTEMS**
Tobias Bund, Benjamin Menhorn, Frank Slomka Ulm University, DE

1815 **MODEL PREDICTIVE CONTROL OVER DELAY-BASED DIFFERENTIATED SERVICES CONTROL NETWORKS**
Riccardo Muradore, Davide Quaglia, Paolo Fiorini University of Verona, IT

IPs **IP4-9, IP4-10**

1830 **CLOSE**

8.8 HOT TOPIC: Countering Counterfeit Attacks on Micro-Electronics

Room - Lesdigiueres (Exhibition Theatre) 1700-1830

Organisers:
Erik Jan Marinissen - IMEC, BE
Ingrid Verbauwhede - KU Leuven, BE

Chair: Steven Jeter, Infineon Technologies, DE
Co-Chair: Ingrid Verbauwhede, KU Leuven, BE

Counterfeited ICs are an increasing problem. In 2011, a record high of 1,363 counterfeit-part incidents were reported world-wide, representing a $169B risk. Counterfeit incidents include the relatively straight-forward extra production at an outsourced manufacturing site for sales through alternative channels, but also the technically more advanced Trojan Horse "sniffer" ICs hidden in a 3D die stack of a telecom product. What can semiconductor suppliers do in technology, design, and test to assure that their customers get to use only genuine components in their systems?

1700 **ANTI-COUNTERFEITING TECHNOLOGIES IMPLEMENTATION INTO IC PACKAGES: CHALLENGES AND ACHIEVEMENTS**
Nathalie Kae-Nune and Stephanie Pesseguier ST Microelectronics, FR

1730 **ANTI-COUNTERFEITING TECHNIQUES IN IC DESIGN**
Benjamin Levine Cryptography Research, US

1800 **ANTI-COUNTERFEITING WITH HARDWARE INTRINSIC SECURITY**
Vincent van der Leest and Pim Tuyls Intrinsic-ID, NL

1830 **CLOSE**

Special Day More-than-Moore

THURSDAY 21 MARCH, 2013

0730 **REGISTRATION and SPEAKERS' BREAKFAST**

9.1 SPECIAL DAY 2 - HOT TOPIC: Smart Grid and Buildings

Room - Oisans 0830-1000

Organiser: Luca Benini, Università di Bologna IT

Chair: Andrea Acquaviva, Politecnico di Torino, IT
Co-Chair: Luca Benini, Università di Bologna, IT

This session will provide a top-down view of energy management and optimization in Smart Environments, with emphasis on Buildings and grid-level integration. The first paper will focus on the design and computer-aided optimization of regional policies for generation, storage and distribution of sustainable energy. The second paper will give a holistic view of grids and building as cyber-physical systems and propose autonomic approaches for managing them. Finally, the third paper will look at design challenges for the distributed smart energy metering infrastructure, with the ultimate goal of reaching self-sustainability through energy harvesting

0830 **SUSTAINABLE ENERGY POLICIES: RESEARCH CHALLENGES AND OPPORTUNITIES**
Michela Milano
Università di Bologna, IT

0930 **SELF-AWARE CYBER-PHYSICAL SYSTEMS AND APPLICATIONS IN SMART BUILDINGS AND CITIES**
Levent Gurgen, Ozan Gunalp, Yazid Benazzouz and Mathieu Galissot
CEA-LETI, FR

1000 **PERPETUAL AND LOW-COST POWER METER FOR MONITORING RESIDENTIAL AND INDUSTRIAL APPLIANCES**
Davide Brunelli[1], Giacomo Paci[2], Domenico Balsamo[3] and Danilo Porcarelli[3]
[1]University of Trento, IT [2]Wispes, IT
[3]Università di Bologna, IT

1000 **EXHIBITION BREAK/IP4**

9.2 System-Level Analysis and Simulation

Room - Belle-Etoile 0830-1000

Chair: Wolfgang Müller, University of Paderborn, DE
Co-Chair: Christian Haubelt, University of Rostock, DE

This session covers different approaches to system-level analysis and simulation. The first two papers propose novel techniques to improve accuracy and simulation speed for TLM and dataflow models. The last two papers present novel approaches to timing analysis and model understanding.

0830 **ANALYTICAL TIMING ESTIMATION FOR TEMPORALLY DECOUPLED TLMS CONSIDERING RESOURCE CONFLICTS**
Kun Lu, Daniel Mueller-Gritschneder and Ulf Schlichtmann
Technische Universitaet Muenchen, DE

0900 **TOWARDS PERFORMANCE ANALYSIS OF SDFGS MAPPED TO SHARED-BUS ARCHITECTURES USING MODEL-CHECKING**
Maher Fakih[1], Kim Grüttner[1], Martin Fränzle[2] and Achim Rettberg[2]
[1]OFFIS Institute for Information Technology, DE
[2]Carl von Ossietzky University, DE

0930 **TOWARD POLYCHRONOUS ANALYSIS AND VALIDATION FOR TIMED SOFTWARE ARCHITECTURES IN AADL**
Yue Ma[1], Huafeng Yu[1], Thierry Gautier[1], Loic Besnard[2], Paul Le Guernic[1], Jean-Pierre Talpin[1] and Maurice Heitz[3]
[1]INRIA, FR, [2]IRISA/CNRS, FR,
[3]C-S Communication & Systems, FR

0945 **TUNING DYNAMIC DATA FLOW ANALYSIS TO SUPPORT DESIGN UNDERSTANDING**
Jan Malburg[1], Alexander Finder[1], Görschwin Fey[2]
[1]University of Bremen, DE,
[2]German Aerospace Center, DE

IPs **IP4-11, IP4-12, IP4-13**

1000 **EXHIBITION BREAK/IP4**

9.3 Thermal/Power Management Techniques for Energy-Efficient Systems

Room - Stendhal 0830-1000

Chair: Wolfgang Nebel, University of Oldenburg, DE
Co-Chair: Alberto Macii, Politecnico di Torino, IT

This session presents four papers on power/thermal techniques for energy efficient systems. The first paper proposes an ultra-low-power management circuit for a miniature sensor node completely powered by an energy harvester for autonomous operation. The second paper presents a bio-inspired power saving method to reduce the power consumption of LED backlit panels. The third paper combines clock and power gating to save energy in disabled flip-fops. And finally the fourth paper introduces a new thermal sensor placement algorithm by exploiting the correlation of power estimation errors among functional blocks.

0830 **A SUB-UA POWER MANAGEMENT CIRCUIT IN 0.18um CMOS FOR ENERGY HARVESTERS**
Biswajit Mishra, Cyril Botteron, Gabriele Tasselli, Christian Robert and Pierre A Farine
EPFL, CH

0900 **SALIENCY AWARE DISPLAY POWER MANAGEMENT**
Yang Xiao[1], Kevin Irick[1], Dongwha Shin[2], Naehyuck Chang[2] and Vijay Narayanan[1]
[1]Pennsylvania State University, US,
[2]Seoul National University, KR

0930 **ACTIVE-MODE LEAKAGE REDUCTION WITH DATA-RETAINED POWER GATING**
Andrew B. Kahng[1], Seokhyeong Kang[1] and Bongil Park[2]
[1]UC San Diego, US, [2]Samsung Electronics, KR

0945 **A POWER-DRIVEN THERMAL SENSOR PLACEMENT ALGORITHM FOR DYNAMIC THERMAL MANAGEMENT**
Hai Wang[1], Sheldon Tan[2], Sahana Swarup[2] and Xue-Xin Liu[2]
[1]University of Electronic Science and Technology of China, CN, [2]University of California, Riverside, US

IPs **IP4-14, IP4-15**

1000 **EXHIBITION BREAK/IP4**

9.4 Emerging Architectures

Room - Chartreuse 0830-1000

Chair: Yvain Thonnart, CEA-LETI, FR
Co-Chair: Michael Niemier, University of Notre Dame, US

This sesssion covers emerging architectures including 3D multi-core processors, reversible logic, and rotary oscillators.

0830 **SPARSE-ROTARY OSCILLATOR ARRAY (SROA) DESIGN FOR POWER AND SKEW REDUCTION**
Ying Teng and Baris Taskin
Drexel University, US

0900 **REVERSIBLE LOGIC SYNTHESIS OF k-INPUT, m-OUTPUT LOOKUP TABLES**
Alireza Shafaei, Mehdi Saeedi, Massoud Pedram
University of Southern California, US

0930 **3D-MMC: A MODULAR 3D MULTI-CORE ARCHITECTURE WITH EFFICIENT RESOURCE POOLING**
Tiansheng Zhang[1], Alessandro Cevrero[2], Giulia Beanato[2], Panagiotis Athanasopoulos[2], Ayse Coskun[1] and Yusuf Leblebici[2]
[1]Boston University, US, [2]EPFL, CH

IPs **IP4-16, IP4-17, IP4-18**

1000 **EXHIBITION BREAK/IP4**

9.5 Manufacturing and Design Security

Room - Meije 0830-1000

Chair: Fresco Regazzoni, TU Delft / University of Lugano, CH
Co-Chair: Patrick Schaumont, Virginia Tech, US

This session describes novel results in the manufacturing and operation of secure chips. The first paper addresses the risks in a secure manufacturing process, and presents a suitable countermeasure. A major risk in secure manufacturing is the insertion of hardware trojans in the design; the second and third paper describe detection techniques for such malicious insertions. The proposed techniques use delay measurements, and multi-modal characterization to achieve high detection probability despite the effects of manufacturing variation. An attacker may also target the design phase and steal intellectual property. The fourth paper introduces a reverse engineering technique to reconstruct a design from a low-level netlist. To answer these threats, we will need new tools and methods. The last paper in this session presents a design method to analyze timing-based security leaks in a design.

0830 **IS SPLIT MANUFACTURING SECURE?**
Jeyavijayan Rajendran[1], Ozgur Sinanoglu[2] and Ramesh Karri[1]
[1]Polytechnic Institute of New York University, US
[2]New York University - Abu Dhabi, AE

0900 **TROJAN DETECTION VIA DELAY MEASUREMENTS: A NEW APPROACH TO SELECT PATHS AND VECTORS TO MAXIMIZE EFFECTIVENESS AND MINIMIZE COST**
Byeongju Cha and Sandeep K. Gupta
University of Southern California, US

0930 **HIGH-SENSITIVITY HARDWARE TROJAN DETECTION USING MULTIMODAL CHARACTERIZATION**
Kangqiao Hu[1], Abdullah N. Nowroz[2], Sherief Reda[2] and Farinaz Koushanfar[1]
[1]Rice University, US, [2]Brown University, US

IPs **IP4-19, IP4-20**

1000 **EXHIBITION BREAK/IP4**

9.6 Improving IC Quality and Lifetime Though Advanced Characterisation

Room - Bayard 0830-1000

Chair: Rob Aitken, ARM, US
Co-Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE

Papers in this session address a broad range of challenges which we face in advanced technologies: how NAND flash ages and how this can be measured, how to ensure high yield for SRAM by doing very

effective simulations, and an adaptive self-calibrating synchronizer that can cope with supply voltage, temperature and process variation.

0830 **THRESHOLD VOLTAGE DISTRIBUTION IN MLC NAND FLASH MEMORY: CHARACTERIZATION, ANALYSIS AND MODELING**
Yu Cai[1], Erich Haratsch[2], Onur Mutlu[1], Ken Mai[1]
[1]Carnegie Mellon University, US, [2]LSI Corporation, US

0900 **EFFICIENT IMPORTANCE SAMPLING FOR HIGH-SIGMA YIELD ANALYSIS WITH ADAPTIVE ONLINE SURROGATE MODELING**
Jian Yao, Zuochang Ye, Yan Wang
Tsinghua University, CN

0930 **METASTABILITY CHALLENGES FOR 65NM AND BEYOND; SIMULATION AND MEASUREMENTS**
Salomon Beer[1], Ran Ginosar[1], Jerome Cox[2], Tom Chaney[2] and Davis M. Zar[2]
[1]Technion, IL, [2]Blendics, US

IPs **IP4-21**

1000 **EXHIBITION BREAK/IP4**

9.7 Design and Scheduling

Room - Les Bans 0830-1000

Chair: Giuseppe Lipari, ENS – Cachan, FR
Co-Chair: Stefan Petters, CISTER/INESC-TEC, ISEP, PT

This session present novel research finding on design and analysis technique for real-time systems. The first paper presents an achitecture for optimally configuring a multi-channel memory controller, so to reduce contention when accessing memory in a multi-processor on-chip system. The second paper presents a method for optimizing the scheduling parameters for a hierarchical scheduling system, where sub-systems can have different periods. The third paper presents a design methodology for code generation of real-time systems from synchronous FSM specifications. Finally, the last paper presents a real-time contention manager for transactional memory based systems.

0830 **ARCHITECTURE AND OPTIMAL CONFIGURATION OF A REAL-TIME MULTI-CHANNEL MEMORY CONTROLLER**
Manil Dev Gomony[1], Benny Akesson[2] and Kees Goossens[1]
[1]Eindhoven University of Technology, NL
[2]Polytechnic Institute of Porto, PT

0900 **HOLISTIC DESIGN PARAMETER OPTIMIZATION OF MULTIPLE PERIODIC RESOURCES IN HIERARCHICAL SCHEDULING**
Man-Ki Yoon[1], Jung-Eun Kim[1], Richard Bradford[2] and Lui Sha[1]
[1]University of Illinois at Urbana-Champaign, US
[2]Rockwell Collins, US

0930 **ROBUST AND EXTENSIBLE TASK IMPLEMENTATION OF SYNCHRONOUS FINITE STATE MACHINES**
Qi Zhu[1], Peng Deng[1], Marco Di Natale[2], and Haibo Zeng[3]
[1]University of California, Riverside, US
[2]Scuola Superiore Sant'Anna, IT [3]McGill University, CA

0945 **FBLT: A REAL-TIME CONTENTION MANAGER WITH IMPROVED REAL-TIME SCHEDULABILITY**
Mohammed Elshambakey and Binoy Ravindran
Virginia Tech, US

IPs **IP4-22, IP4-23**

1000 **EXHIBITION BREAK/IP4**

IP4 Interactive Presentations

Room - Salle de Reception 1000-1030

Interactive Presentations run simulatenously during a 30-minute slot. A poster associated to the IP paper is on display throughout the morning. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP4-1 **EFFICIENT AND SCALABLE OPENMP-BASED SYSTEM-LEVEL DESIGN**
Alessandro Cilardo, Luca Gallo, Antonino Mazzeo and Nicola Mazzocca
University of Naples Federico II, IT

IP4-2 **UTILIZING VOLTAGE-FREQUENCY ISLANDS IN C-TO-RTL SYNTHESIS FOR STREAMING APPLICATIONS**
Xinyu He[1], Shuangchen Li[1], Yongpan Liu[1], X. Sharon Hu[2] and Huazhong Yang[1]
[1]Tsinghua University, CN, [2]University of Notre Dame, US

IP4-3 **BICONDITIONAL BDD: A NOVEL CANONICAL BDD FOR LOGIC SYNTHESIS TARGETING XOR-RICH CIRCUITS**
Luca Amarú, Pierre-Emmanuel Gaillardon and Giovanni De Micheli
EPFL, CH

IP4-4 **OPTIMIZING BDDS FOR TIME-SERIES DATASET MANIPULATION**
Stergios Stergiou and Jawahar Jain
Fujitsu, US

IP4-5 **INCORPORATING THE IMPACTS OF WORKLOAD-DEPENDENT RUNTIME VARIATIONS INTO TIMING ANALYSIS**
Farshad Firouzi[1], Saman Kiamehr[1], Sani Nassif[2] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE [2]IBM, US

IP4-6 **AN AREA-EFFICIENT NETWORK INTERFACE FOR A TDM-BASED NETWORK-ON-CHIP**
Jens Sparsø, Evangelia Kasapaki and Martin Schoeberl
Technical University of Denmark, DK

IP4-7 **CARS: CONGESTION-AWARE REQUEST SCHEDULER FOR NETWORK INTERFACES IN NOC-BASED MANYCORE SYSTEMS**
Masoud Daneshtalab, Masoumeh Ebrahimi, Juha Plosila and Hannu Tenhunen
University of Turku, FI

IP4-8 **A FAST AND EFFICIENT DFT FOR TEST AND DIAGNOSIS OF POWER SWITCHES IN SOCs**
Xiaoyu Huang, Jimson Mathew, Rishad A Shafik, Subhashish Bhattacharjee and Dhiraj K Pradhan
University of Bristol, UK

IP4-9 **MULTIRATE CONTROLLER DESIGN FOR RESOURCE- AND SCHEDULE-CONSTRAINED AUTOMOTIVE ECUS**
Dip Goswami[1], Alejandro Masrur[1], Reinhard Schneider[1], Chun Jason Xue[2] and Samarjit Chakraborty[1]
[1]TU Munich, DE, [2]City University, Hong Kong, HK

IP4-10 **DESIGN OF AN ULTRA-LOW POWER DEVICE FOR AIRCRAFT STRUCTURAL HEALTH MONITORING**
Alessandro Perelli[1], Carlo Caione[1], Luca De Marchi[2], Davide Brunelli[2], Alessandro Marzani[1], and Luca Benini[1]
[1]University of Bologna, IT
[2]University of Trento, IT

IP4-11 **FAST AND ACCURATE TLM SIMULATIONS USING TEMPORAL DECOUPLING FOR FIFO-BASED COMMUNICATIONS**
Claude Helmstetter[1], Jérôme Cornet[2], Matthieu Moy[3], Pascal Vivet[1] and Bruno Galilée[2]
[1]CEA-LETI, FR [2]STMicroelectronics, FR [3]Verimag, FR

IP4-12 **DETERMINING RELEVANT MODEL ELEMENTS FOR THE VERIFICATION OF UML/OCL SPECIFICATIONS**
Julia Seiter, Robert Wille, Mathias Soeken and Rolf Drechsler
University of Bremen, DE

IP4-13 **TOWARDS A GENERIC VERIFICATION METHODOLOGY FOR SYSTEM MODELS**
Robert Wille, Martin Gogolla, Mathias Soeken, Mirco Kuhlmann and Rolf Drechsler
University of Bremen, DE

IP4-14 **ACTIVE POWER-GATING-INDUCED POWER/GROUND NOISE ALLEVIATION USING PARASITIC CAPACITANCE OF ON-CHIP MEMORIES**
Xuan Wang[1], Jiang Xu[1], Wei Zhang[2], Xiaowen Wu[1], Yaoyao Ye[1], Zhehui Wang[1], Mahdi Nikdast[1] and Zhe Wang[1]
[1]Hong Kong University of Science and Technology, HK
[2]Nanyang Technological University, SG

IP4-15 **ADAPTIVE THERMAL MANAGEMENT FOR PORTABLE SYSTEM BATTERIES BY FORCED CONVECTION COOLING**
Qing Xie[1], Siyu Yue[1], Donghwa Shin[2], Naehyuck Chang[2] and Massoud Pedram[1]
[1]University of Southern California, US
[2]Seoul National University, KR

IP4-16 **CACHE COHERENCE ENABLED ADAPTIVE REFRESH FOR VOLATILE STT-RAM**
Jianhua Li[1], Liang Shi[1], Qingan Li[2], Chun Jason Xue[3], Yiran Chen[4] and Yinlong Xu[1]
[1]University of Science and Technology of China, CN,
[2]Wuhan University, CN,
[3]City University of Hong Kong, CN
[4]University of Pittsburgh, US

IP4-17 **IS TSV-BASED 3D INTEGRATION SUITABLE FOR INTER-DIE MEMORY REPAIR?**
Mihai Lefter, George Razvan Voicu, Mottaqiallah Taouil, Marius Enachescu, Said Hamdioui and Sorin Dan Cotofana
Delft University of Technology, NL

IP4-18 **THERMOMECHANICAL STRESS-AWARE MANAGEMENT FOR 3D IC DESIGNS**
Qiaosha Zou[1], Tao Zhang[1], Eren Kursun[2] and Yuan Xie[1]
[1]Pennsylvania State University, US [2]IBM research, US

IP4-19 **REVERSE ENGINEERING DIGITAL CIRCUITS USING FUNCTIONAL ANALYSIS**
Pramod Subramanyan, Nestan Tsiskaridze, Kanika Pasricha, Dillon Reisman, Adriana Susnea, and Sharad Malik
Princeton University, US

IP4-20 **A PRACTICAL TESTING FRAMEWORK FOR ISOLATING HARDWARE TIMING CHANNELS**
Jason Oberg[1], Sarah Meiklejohn[1], Timothy Sherwood[2], and Ryan Kastner[1]
[1]UC San Diego, US, [2]UC Santa Barbara, US

IP4-21 **DESIGN AND IMPLEMENTATION OF AN ADAPTIVE PROACTIVE RECONFIGURATION TECHNIQUE FOR SRAM CACHES**
Peyman Pouyan, Esteve Amat, Francesc Moll, and Antonio Rubio
Universitat Politècnica de Catalunya, Es

IP4-22 **A VIRTUAL PROTOTYPING PLATFORM FOR REAL-TIME SYSTEMS WITH A CASE STUDY FOR A TWO-WHEELED ROBOT**
Daniel Mueller-Gritschneder, Kun Lu, Erik Wallander, Marc Greim and Ulf Schlichtmann
Technische Universitaet Muenchen, DE

IP4-23 **SUFFICIENT REAL-TIME ANALYSIS FOR AN ENGINE CONTROL UNIT WITH CONSTANT ANGULAR VELOCITIES**
Victor Pollex[1], Timo Feld[1], Frank Slomka[1], Ulrich Margull[2], Ralph Mader[3] and Gerhard Wirrer[3]
[1]Ulm University, DE, [2]Ingolstadt University of Applied Sciences, DE, [3]Continental, DE

10.1 SPECIAL DAY 2 - HOT TOPIC: Smart Data Centers Design and Optimisation

Room - Oisans 1100-1230

Organiser: David Atienza - EPFL, CH

Chair: Roman Hermida, UCM, ES
Co-Chair: Ayse Coskun, Boston University, US

This special session presents an overview of some of the hottest research topics towards the conception of future smart and energy-efficient datacenters. The first presentation explores the limits in the conception of highly dense datacenter infrastructures under current and future energy constraints. The second presentation presents smart energy-aware allocation techniques in virtualized datacenters to maximize the use of free cooling. The third presentation explores the limits of energy-efficient servers and resources utilization in next-generation computing systems for datacenters.

1100 **ROADMAP TOWARDS ULTIMATELY EFFICIENT ZETA-SCALE DATACENTERS**
Patrick Ruch, Thomas Brunschwiler, Gerhard Ingmar Meijer, Gerd Schlottig, Stephan Paredes and Bruno Michel
IBM, US

1130 **CORRELATION-AWARE VIRTUAL MACHINE ALLOCATION FOR ENERGY-EFFICIENT DATACENTERS**
Jungsoo Kim[1], Martino Ruggiero[1], David Atienza[1], and Marcel Lederberger[2]
[1]EPFL, CH, [2]Credit Suisse, CH

1200 **RESOURCE EFFICIENT COMPUTING FOR WAREHOUSE-SCALE DATACENTERS**
Christos Kozyrakis
Stanford University, US

1230 **LUNCH BREAK**

10.2 EMBEDDED TUTORIAL: On the Use of GP-GPUs for Accelerating Computing-Intensive EDA Applications

Room - Belle-Etoile 1100-1230

Chair: Franco Fummi, University of Verona, IT
Co-Chair: Florian Letombe, SpringSoft, FR

General purpose graphics processing units (GP-GPUs) have recently been explored as a new computing paradigm for accelerating computation intensive EDA applications. Such many-core architectures have been applied for (i) accelerating both logic and fault simulation of HDL designs, (ii) accelerating simulation of such designs described both at RTL and Gate level, (iii) accelerating SystemC simulation.

This embedded tutorial presents a comprehensive analysis of the best results obtained by adopting GP-GPUs in all these EDA applications.

1100 **ON THE USE OF GP-GPUS FOR ACCELERATING LOGIC SIMULATION**
Valeria Bertacco and Debapriya Chatterjee
University of Michigan, US

1130 **ACCELERATING RTL SIMULATION WITH GP-GPUS: CUDA VS. OPENCL**
Nicola Bombieri and Sara Vinco
University of Verona, IT

1200 **PARALLELIZING SYSTEMC SIMULATIONS ACROSS CPUs AND GPUs**
Hiren Patel
University of Waterloo, CA

1230 **LUNCH BREAK**

10.3 Thermal Analysis and Power Optimisation Techniques

Room - Stendhal - 1100-1230

Chair: Siddharth Garg, University of Waterloo, CA
Co-Chair: Yiran Chen, University of Pittsburgh, US

The circuit reliability is greatly impacted by its thermal profile and power consumption. This session starts with the power optimization and lifetime enhancements for modern VLSI circuits, followed by thermal analysis and simulation methods of 3D ICs

1100 **SUBSTITUTE-AND-SIMPLIFY: A UNIFIED DESIGN PARADIGM FOR APPROXIMATE AND QUALITY CONFIGURABLE CIRCUITS**
Swagath Venkataramani, Kaushik Roy, and Anand Raghunathan
Purdue University, US

1130 **ENHANCING MULTICORE RELIABILITY THROUGH WEAR COMPENSATION IN ONLINE ASSIGNMENT AND SCHEDULING**
Thidapat Chantem[1], Yun Xiang[2], X. Sharon Hu[3] and Robert P. Dick[2]
[1]Utah State University, US, [2]University of Michigan, US
[3]University of Notre Dame, US

1200 **NUMANA: A HYBRID NUMERICAL AND ANALYTICAL THERMAL SIMULATOR FOR 3-D ICS**
Yu-Min Lee[1], Tsung-Heng Wu[1], Pei-Yu Huang[2] and Chi-Ping Yang[1]
[1]National Chiao Tung University, TW
[2]Industrial Technology Research Institute, TW

1215 **EXPLICIT TRANSIENT THERMAL SIMULATION OF LIQUID-COOLED 3D ICS**
Alain Fourmigue, Giovanni Beltrame and Gabriela Nicolescu
Ecole Polytechnique Montreal, CA

IPs **IP5-1, IP5-2**

1230 **LUNCH BREAK**

10.4 Abstraction Techniques and SAT/SMT-Based Optimisations

Room - Chartreuse 1100-1230

Chair: Fahim Rahim, Atrenta, FR
Co-Chair: Julian Schmaltz, Open University of the Netherlands, NL

Automatically computing abstractions of large circuits combined with powerful SAT and SMT solvers is key to the success of formal verification techniques. The papers of this session present significant improvements in abstraction techniques and SAT/SMT-based optimizations. SAT- and SMT-abstractions are guided by unsatisfiable cores. Three papers address the issue of reducing the size of interpolants generated during the construction of abstractions. The second paper proposes a new abstraction technique demonstrating a significant improvement in gate-level abstractions.

1100 **GLA: GATE-LEVEL ABSTRACTION REVISITED**
Alan Mishchenko[1], Niklas Een[1], Robert Brayton[1], Jason Baumgartner[2], Hari Mony[2] and Pradeep Nalla[3]
[1]UC Berkeley, US, [2]IBM, US, [3]IBM, IN

1130 **LEMMA LOCALIZATION: A PRACTICAL METHOD FOR DOWNSIZING SMT-INTERPOLANTS**
Florian Pigorsch and Christoph Scholl
University of Freiburg, DE

1200 **CORE MINIMIZATION IN SAT-BASED ABSTRACTION**
Anton Belov[1], Huan Chen[1], Alan Mishchenko[2] and Joao Marques-Silva[1]
[1]University College Dublin, IE
[2]University of California, Berkeley, US

1215 **OPTIMIZATION TECHNIQUES FOR CRAIG INTERPOLANT COMPACTION IN UNBOUNDED MODEL CHECKING**
Gianpiero Cabodi, Carmelo Loiacono and Danilo Vendraminetto
Politecnico di Torino, IT

IPs **IP5-3, IP5-4**

1230 **LUNCH BREAK**

10.5 Design and Verification of Mixed-Signal Circuits

Room - Meije 1100-1230

Chair: Catherine Dehollain, EPFL, CH
Co-Chair: Gunhan Dundar, Bogazici University, TR

Some key questions in mixed-signal design are low-power design, modeling, and verification. This session addresses design of low power, low-voltage sensor interfaces as well as non-linear model extraction of analogue circuits and statistical MOSFET models. On the verification front, formal verification of analogue circuits and reachability analysis of non-linear circuits are discussed.

1100 **A LOW-POWER AND LOW-VOLTAGE BBPLL-BASED SENSOR INTERFACE IN 130nm CMOS FOR WIRELESS SENSOR NETWORKS**
Jelle Van Rethy, Hans Danneels, Valentijn De Smedt, Wim Dehaene and Georges Gielen
KU Leuven, BE

1130 **REACHABILITY ANALYSIS OF NONLINEAR ANALOG CIRCUITS THROUGH ITERATIVE REACHABLE SET REDUCTION**
Seyed Nematollah Ahmadyan and Shohba Vasudevan
University of Illinois at Urbana-Champaign, US

1200 **FORMAL VERIFICATION OF ANALOG CIRCUIT PARAMETERS ACROSS VARIATION UTILIZING SAT**
Merritt Miller and Forrest Brewer
University of California, Santa Barbara, US

1215 **EXTRACTING ANALYTICAL NONLINEAR MODELS FROM ANALOG CIRCUITS BY RECURSIVE VECTOR FITTING OF TRANSFER FUNCTION TRAJECTORIES**
Dimitri De Jonghe[1], Dirk Deschrijver[2], Tom Dhaene[2] and Georges Gielen[1]
[1]KU Leuven, BE [2]University of Ghent, BE

IPs **IP5-5, IP5-6**

1230 **LUNCH BREAK**

10.6 On-Line Testing Techniques

Room - Bayard 1100-1230

Chair: Cecilia Metra, University of Bologna, IT
Co-Chair: Cristiana Bolchini, Politecnico Di Milano, IT

This session proposes several approaches for on-line testing and analysis of in-core components such as register files and memory sub-systems.

1100 **ON-LINE FUNCTIONALLY UNTESTABLE FAULT IDENTIFICATION IN EMBEDDED PROCESSOR CORES**
Paolo Bernardi[1], Ernesto Sanchez[1], Matteo Sonza Reorda[1], Oscar Ballan[2] and Matteo Bonazza[1]
[1]Politecnico di Torino, IT, [2]STMicroelectronics, IT

1130 **CAPTURING VULNERABILITY VARIATIONS FOR REGISTER FILES**
Xavier Vera[1], Javier Carretero[1], Enric Herrero[1], Matteo Monchiero[2] and Tanausu Ramirez[1]
[1]Intel, ES, [2]Intel, IT

1200 **ERROR DETECTION IN TERNARY CAMS USING BLOOM FILTERS**
Salvatore Pontarelli[1], Marco Ottavi[1], Adrian Evans[2] and Shi-Jie Wen[2]
[1]University of Rome "Tor Vergata", IT,
[2]Cisco Systems, CA,
[3]Cisco Systems, US

1215 **AVF-DRIVEN PARITY OPTIMIZATION FOR MBU PROTECTION OF IN-CORE MEMORY ARRAYS**
Michail Maniatakos[1], Maria Michael[2] and Yiorgos Makris[3]
[1]New York University Abu Dhabi, AE
[2]University of Cyprus, CY
[3]University of Texas at Dallas, US

IPs **IP5-7, IP5-8, IP5-9**

1230 **LUNCH BREAK**

10.7 Embedded Software for Many-Core Architectures

Room - Les Bans 1100-1230

Chair: Oliver Bringmann, University of Tübingen, DE
Co-Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, FR

This session deals with parallel programming models and scheduling. The first paper employs game theory to decentralized task migration for execution speed-up and fault tolerance. The other three papers propose parallel-programming models and scheduling approaches for software pipelines, fine-grained OpenMP, and asynchronous joining of forked tasks, respectively.

1100 **GAME-THEORETIC ANALYSIS OF DECENTRALIZED CORE ALLOCATION SCHEMES ON MANY-CORE SYSTEMS**
Stefan Wildermann, Tobias Ziermann and Jürgen Teich
University Erlangen-Nuremberg, DE

1130 **ENABLING FINE-GRAINED OPENMP TASKING ON TIGHTLY-COUPLED SHARED MEMORY CLUSTERS**
Paolo Burgio, Giuseppe Tagliavini, Andrea Marongiu and Luca Benini
University of Bologna, IT

1200 **ARTM: A LIGHTWEIGHT FORK-JOIN FRAMEWORK FOR MANYCORE EMBEDDED SYSTEMS**
Maroun Ojail, Raphaël David, Yves Lhuillier and Alexandre Guerre
CEA LIST, FR

1215 **PIPELETS: SELF-ORGANIZING SOFTWARE PIPELINES FOR MANY CORE ARCHITECTURES**
Janmartin Jahn and Jörg Henkel
Karlsruhe Institute of Technology, DE

IPs **IP5-10**

1230 **LUNCH BREAK**

10.8 PANEL: Will 3D-IC Remain a Technology of the Future... Even in the Future?

Room - Lesdigiueres (Exhibition Theatre) 1100-1230

Organiser: Marco Casale-Rossi, Synopsys, US

Chair: Giovanni De Micheli, EPFL
Co-Chair: Marco Casale-Rossi, Synopsys, US

Panellists:
Patrick Blouet ST-Ericsson, FR
Brendan Farley Xilinx, IE
Anna Fontanelli Monozukuri, IT
Patrick Leduc LETI, FR
Dragomir Milojevic IMEC, BE
Steve Smith Synopsys, US

If asked "who needs faster planes?" the vast majority of the 2.75 billion airline passengers (source: IATA 2011) would say that they do need faster planes, and that they need them right now. Still, the commercial aircrafts cruising speed has remained the same – 800 km/hour – over the last 50+ years, and after the sad end of the Concorde project, neither Airbus nor Boeing are seriously working on the topic. Along the same lines, when asked "who needs 3D-IC?", most IC designers say that they desperately need 3D-IC to keep advancing electronic products performance, whilst addressing the needs of higher bandwidth, lower cost, heterogeneous integration, and power constraints. Still, 3D-IC continues to be the technology of the future. What are the road blocks towards 3D-IC adoption? Is it process technology, foundry or OSAT commercial offering, or EDA, or the business economics that is holding 3D-IC on the ground? In the introductory presentation of this panel session, LETI Patrick Leduc will illustrate the state-of-the-art of commercial, mainstream 3D-IC. EPFL Professor Giovanni de Micheli will moderate an industry and research panel, to understand what are the key factors preventing 3D-IC from becoming the technology of today.

1230 **LUNCH BREAK**

11.0 SPECIAL DAY 2 LUNCH-TIME KEYNOTE

Room - Oisans 1330-1400

1330 **SMART CITIES AND COMMUNITIES AT THE REGIONAL, NATIONAL AND EUROPEAN LEVELS**
Francesco Profumo, Italian Minister of Education, University and Research and
Genevieve Fioraso, French Minister for Higher Education and Research

1400 **BREAK**

11.1 SPECIAL DAY 2 - HOT TOPIC: Smart Health

Room - Oisans 1400-1530

Chair: Daniela De Venuto, Politecnico di Bari, IT
Co-Chair: Alberto Sangiovanni Vincentelli, University of California, Berkeley, US

The Smart Health session is about fundamental technical and scientific advances that may change radically the way healthcare is conceived today. Longer life expectation, aging, overweight and pollution are among factors that pose severe challenges to healthcare and its sustainability. Wireless devices, brain-machine interfaces, and cognitive process models may provide potential solutions to a vast array of problems involving clinical and human aspects, as well as economics and social issues. The presenters will introduce and discuss some aspects of devices and technologies that are essential in defining new approaches to healthcare and human well-being.

1400 **DR. FRANKENSTEIN'S DREAM MADE POSSIBLE: IMPLANTED ELECTRONIC DEVICES**
Daniela De Venuto[1]
and Alberto Sangiovanni Vincentelli[2]
[1]Politecnico di Bari, IT,
[2]University of California, Berkeley, US

1420 **MANAGING HEALTH INSTEAD OF MANAGING ILLNESS - AN OPPORTUNITY FOR WIRELESS WEARABLE SENSORS**
Chris Van Hoof[1] **and Julien Penders**[2]
[1]IMEC, BE [2]IMEC/Holst Centrum, NL

1445 **ELECTRONIC IMPLANTS: POWER DELIVERY AND MANAGEMENT**
Jacopo Olivo, Sara S. Ghoreishizadeh, Sandro Carrara and Giovanni De Micheli
EPFL, CH

1510 **CYBORG INSECTS, NEURAL INTERFACES AND OTHER THINGS: BUILDING INTERFACES BETWEEN THE SYNTHETIC AND THE MULTICELLULAR**
J. Van Kleef, T. Massey, P. Ledochowitsch, R. Muller, R. Tiefenauer, T. Blanche, Hirotaka Sato and Michel M. Maharabiz -
University of California, Berkeley, US

1530 **BREAK/IP5**

11.2 High-Level Synthesis and Coarse-Grained Reconfigurable Architectures

Room - Belle-Etoile 1400-1530

Chair: Philippe Coussy, Universite de Bretagne-Sud, FR
Co-Chair: Fadi Kurdahi, University of California Irvine, US

The first paper investigates the impact of simultaneous scheduling and binding in high-level synthesis. The second paper improves latency by performing high-level code transformation with Taylor Expansion Diagrams. The thirth paper presents a platform based on custom reconfigurable arrays for multi-processor systems exploiting instruction- and thread-level parallelism.The fourth paper proposes a high-level modelling tool chain for embedded FPGAs.

1400 **SHARE WITH CARE: A QUANTITATIVE EVALUATION OF SHARING APPROACHES IN HIGH-LEVEL SYNTHESIS**
Alex Kondratyev, Luciano Lavagno, Mike Meyer and Yosinori Watanabe
Cadence Design Systems, US

1430 **FPGA LATENCY OPTIMIZATION USING SYSTEM-LEVEL TRANSFORMATIONS AND DFG RESTRUCTURING**
Daniel Gomez-Prado, Maciej Ciesielski and Russell Tessier
University of Massachusetts, US

1445 **A TRANSPARENT AND ENERGY AWARE RECONFIGURABLE MULTIPROCESSOR PLATFORM FOR SIMULTANEOUS ILP AND TLP EXPLOITATION**
Mateus Rutzig[1], Antonio Carlos Schneider Beck[2] and Luigi Carro[2]
[1]Federal University of Santa Maria, BR
[2]Federal University of Rio Grande do Sul, BR

1500 **HIGH-LEVEL MODELING AND SYNTHESIS FOR EMBEDDED FPGAs**
Xiaolin Chen, Shuai Li, Jochen Schleifer, Thomas Coenen, Anupam Chattopadhyay, Gerd Ascheid and Tobias Noll
RWTH Aachen University, DE

IPs **IP5-11, IP5-12, IP5-13**

1530 **BREAK/IP5**

11.3 Efficient NoC Routing Mechanisms

Room - Stendhal 1400-1530

Chair: Fabien Clermidy, CEA-LETI, FR
Co-Chair: Jose Flich, Technical University of Valencia, ES

This session proposes novel NoC routing mechanisms and policies that push the envelope of efficient SoC design. The first paper reduces latencies in deflection-based systems, while the other two focus on fault tolerance.

1400 **DEBAR: DEFLECTION BASED ADAPTIVE ROUTER WITH MINIMAL BUFFERING**
John Jose, Bhawna Nayak, Kranthi Kumar and Madhu Mutyam
Indian Institute of Technology Madras, IN

1430 **CONTRASTING WAVELENGTH-ROUTED OPTICAL NOC TOPOLOGIES FOR POWER-EFFICIENT 3D-STACKED MULTICORE PROCESSORS USING PHYSICAL-LAYER ANALYSIS**
Luca Ramini[1], Paolo Grani[2], Sandro Bartolini[2] and Davide Bertozzi[1]
[1]University of Ferrara, IT [2]University of Siena, IT

1500 **TOPOLOGY AGNOSTIC FAULT-TOLERANT NOC ROUTING METHOD**
Eduardo Wachter, Augusto Erichsen, Alexandre Amory and Fernando Moraes
PUCRS, BR

IPs **IP5-14, IP5-15**

1530 **BREAK/IP5**

11.4 System-Level Modelling for Physical Properties

Room - Chartreuse 1400-1530

Chair: Frank Oppenheimer, OFFIS, DE
Co-Chair: François Pêcheux, UPMC, FR

Physical properties have a great impact on the robustness and predictable behaviour of complex micro-electronic systems, and therefore should be considered at system-level. The first paper addresses power and thermal management at the transaction level, while the last two papers present innovative analysis techniques to increase system reliability.

1400 **SYSTEM-LEVEL MODELING OF ENERGY IN TLM FOR EARLY VALIDATION OF POWER AND THERMAL MANAGEMENT**
Tayeb Bouhadiba[1, 2], Matthieu Moy[1, 3] and Florence Maraninchi[1, 3]
[1]Verimag, FR, [2]CNRS, FR, [3]Grenoble INP, FR

1430 **SYSTEM-LEVEL MODELING AND MICROPROCESSOR RELIABILITY ANALYSIS FOR BACKEND WEAROUT MECHANISMS**
Chang-Chih Chen and Linda Milor Georgia Institute of Technology, US

1500 **AUTOMATIC SUCCESS TREE-BASED RELIABILITY ANALYSIS FOR THE CONSIDERATION OF TRANSIENT AND PERMANENT FAULTS**
Hananeh Aliee, Michael Glaß, Felix Reimann and Jürgen Teich University of Erlangen-Nuremberg, DE

IPs **IP5-16**

1530 **BREAK/IP5**

11.5 Energy Challenges for Multi-Core and NoC Architectures

Room - Meije 1400-1530

Chair: Alberto Garcia-Ortiz, University of Bremen, DE
Co-Chair: Domenik Helms, OFFIS, DE

This session presents four papers targeting multi-core and NoCs architectures. The first paper presents models for protecting and preventing intermittent device defects. The second paper proposes a self-resetting logic repeater (SRLR) for a signaling datapath of a mesh NoC. The third paper describes how 3D technology can be used to regulate power delivery for a multi-core system. Finally, the fourth paper presents a data-path merging heat distribution aware algorithm for coarse-grained reconfigurable processors.

1400 **COMMUNICATION AND MIGRATION ENERGY AWARE DESIGN SPACE EXPLORATION FOR MULTICORE SYSTEMS WITH INTERMITTENT FAULTS**
Anup Das, Akash Kumar and Bharadwaj Veeravalli National University of Singapore, SG

1430 **40.4FJ/BIT/MM LOW-SWING ON-CHIP SIGNALING WITH SELF-RESETTING LOGIC REPEATERS EMBEDDED WITHIN A MESH NoC IN 45nm SOI CMOS**
Sunghyun Park, Masood Qazi, Li-Shiuan Peh and Anantha Chandrakasan MIT, US

1500 **3D RECONFIGURABLE POWER SWITCH NETWORK BY SPACE-TIME MULTIPLEXING FOR DEMAND-SUPPLY MATCHING BETWEEN ON-CHIP MULTI-OUTPUT POWER CONVERTERS AND MANY-CORE MICROPROCESSORS**
Kanwen Wang[1], Hao Yu[1], Chun Zhang[2] and Benfei Wang[1]
[1]Nanyang Technological University, SG
[2]Missouri University of Science and Technology, US

1515 **THERMAL-AWARE DATAPATH MERGING FOR COARSE-GRAINED RECONFIGURABLE PROCESSORS**
Sotirios Xydis, Gianluca Palermo and Cristina Silvano Politecnico Di Milano, IT

1530 **BREAK/IP5**

11.6 Modelling and Design for Signal and Power Integrity

Room - Bayard 1400-1530

Chair: Stefano Grivet-Talocia, Politecnico di Torino, IT
Co-Chair: Piero Triverio, University of Toronto, IT

This session discusses state-of-the-art approaches for modelling and design optimization of signal and power distribution networks. Advancements are illustrated on power supply pads placement based on locality and temperature-dependent electromigration, on optimized GPU implementations for capacitance extraction, jitter charaterization via incoherent undersampling and coding-based crosstalk mitigation.

1400 **PLACEMENT OPTIMIZATION OF POWER SUPPLY PADS BASED ON LOCALITY**
Pingqiang Zhou, Vivek Mishra and Sachin Sapatnekar
University of Minnesota, Twin Cities, US

1430 **GPU-FRIENDLY FLOATING RANDOM WALK ALGORITHM FOR CAPACITANCE EXTRACTION OF VLSI INTERCONNECTS**
Kuangya Zhai, Wenjian Yu and Hao Zhuang
Tsinghua University, CN

1500 **PERIODIC JITTER AND BOUNDED UNCORRELATED JITTER DECOMPOSITION OF INCOHERENT UNDERSAMPLING**
Nicholas Tzou, Debesh Bhatta, Sen-Wen Hsiao and Abhijit Chatterjee
Georgia Tech, US

1515 **CROSSTALK AVOIDANCE CODES FOR 3D VLSI**
Rajeev Kumar and Sunil Khatri
Texas A&M University, US

IP **IP5-17**

1530 **BREAK/IP5**

11.7 Powerful Aging

Room - Les Bans 1400-1530

Chair: Jose Pineda de Gyvez, NXP Semiconductors, NL
Co-Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE

This session focuses on two general topics: power supply networks and transistor aging effects. The first paper proposes a methodology to more accurately select library characterization voltages to account for aging in the presence of adaptive voltage scaling. The second paper provides an efficient way to simultaneously analyze the electrical and thermal behaviour of a power grid while the third paper uses process, voltage, temperature, and aging sensors at the architecture level to improve the performance of a circuit. The fourth paper describes a new way to construct area-efficient irregular power networks.

1400 **IMPACT OF ADAPTIVE VOLTAGE SCALING ON AGING-AWARE SIGNOFF**
Tuck-Boon Chan, Wei-Ting Chan and Andrew B. Kahng University of California at San Diego, US

1430 **A PARALLEL FAST TRANSFORM-BASED PRECONDITIONING APPROACH FOR ELECTRICAL-THERMAL CO-SIMULATION OF POWER DELIVERY NETWORKS**
Konstantis Daloukas, Alexia Marnari, Nestor Evmorfopoulos, Panagiota Tsompanopoulou and George I. Stamoulis University of Thessaly, GR

1500 **HIERARCHICALLY FOCUSED GUARDBANDING: AN ADAPTIVE APPROACH TO MITIGATE PVT VARIATIONS AND AGING**
Abbas Rahimi[1], Luca Benini[2] and Rajesh Gupta[1]
[1]University of California, San Diego, US
[2]University of Bologna, IT

1515 **EFFECTIVE POWER NETWORK PROTOTYPING VIA STATISTICAL-BASED CLUSTERING AND SEQUENTIAL LINEAR PROGRAMMING**
Sean Shih-Ying Liu[1], Chieh-Jui Lee[1], Chuan-Chia Huang[1], Hung-Ming Chen[1], Chang-Tzu Lin[2], Chia-Hsin Lee[2]
[1]National Chiao Tung University, TW
[2]Industrial Technology Research Institute, TW

IPs **IP5-18, IP5-19**

1530 **BREAK/IP5**

11.8 EMBEDDED TUTORIAL: Advances in Asynchronous Logic: from Principles to GALS & NoC, Recent Industry Applications, and Commercial CAD Tools

Room - Lesdigiueres (Exhibition Theatre) 1400-1530

Organiser: Pascal Vivet, CEA-LETI, FR

Chair: Robin Wilson, STMicroelectronics, FR
Co-Chair: Beigné Edith, CEA-LETI, FR

The growing variability and complexity of advanced CMOS technologies makes the physical design of clocked logic in large Systems-on-Chip more and more challenging. Asynchronous logic has been studied for many years and become an attractive solution for a broad range of applications, from massively parallel multi-media systems to systems with ultra-low power & low-noise constraints, like cryptography, energy autonomous systems, and sensor-network nodes.

The objective of this embedded tutorial is to give a comprehensive and recent overview of asynchronous logic. The tutorial will cover the basic principles and advantages of asynchronous logic, some insights on new research challenges, and will present the GALS scheme as an intermediate design style with recent results in asynchronous Network-on-Chip for future Many Core architectures. Regarding industrial acceptance, recent asynchronous logic applications within the microelectronics industry will be presented, with a main focus on the commercial CAD tools available today.

1400 **ASYNCHRONOUS DESIGN PRINCIPLES, FROM INTRODUCTION TO RESEARCH CHALLENGES**
Alex Yakovlev Newcastle University, UK

1430 **GALS & NOC FOR STRUCTURED SOC LEVEL INTERCONNECTS, AND ADVANCES OF ASYNCHRONOUS LOGIC IN THE INDUSTRY**
Pascal Vivet CEA-LETI, FR

1500 **INTRODUCTION TO TIEMPO ASYNCHRONOUS CIRCUIT SYNTHESIS AND DESIGN FLOW**
Marc Renaudin TIEMPO, FR

1530 **BREAK/IP5**

IP5 Interactive Presentations

Room - Salle de Reception 1530-1600

Interactive Presentations run simulatenously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation.

IP5-1 **MITIGATING DARK SILICON PROBLEMS USING SUPERLATTICE-BASED THERMOELECTRIC COOLERS**
Francesco Paterna and Sherief Reda
Brown University, US

IP5-2 **RUN-TIME PROBABILISTIC DETECTION OF MISCALIBRATED THERMAL SENSORS IN MANY-CORE SYSTEMS**
Jia Zhao, Shiting (Justin) Lu, Wayne Burleson and Russell Tessier
University of Massachusetts, US

IP5-3 **FORMAL ANALYSIS OF STEADY STATE ERRORS IN FEEDBACK CONTROL SYSTEMS USING HOL-LIGHT**
Osman Hasan and Muhammad Ahmad
National University of Sciences and Technology, PK

IP5-4 **A NOVEL CONCURRENT CACHE-FRIENDLY BINARY DECISION DIAGRAM CONSTRUCTION FOR MULTI-CORE PLATFORMS**
Mahmoud El-Bayoumi[1], Michael Hsiao[1] and Mustafa ElNainay[2]
[1]Virginia Tech, US [2]Alexanderia University, EG

IP5-5 **STATISTICAL MODELING WITH THE VIRTUAL SOURCE MOSFET MODEL**
Li Yu[1], Lan Wei[1], Dimitri Antoniadis[1], Ibrahim Elfadel[2] and Duane Boning[1]
[1]Massachusetts Institute of Technology, US
[2]Masdar Institute of Science and Technology, AE

IP5-6 **AUTOMATIC CIRCUIT SIZING TECHNIQUE FOR THE ANALOG CIRCUITS WITH FLEXIBLE TFTS CONSIDERING PROCESS VARIATION AND BENDING EFFECTS**
Yen-Lung Chen, Wan-Rong Wu, Guan-Ruei Lu and Chien-Nan Jimmy Liu
National Central University, TW

IP5-7 **AN ENHANCED DOUBLE-TSV SCHEME FOR DEFECT TOLERANCE IN 3D-IC**
Hsiu-Chuan Shih and Cheng-Wen Wu
National Tsing Hua University, TW

IP5-8 **MEMPACK: AN ORDER OF MAGNITUDE REDUCTION IN THE COST, RISK, AND TIME FOR MEMORY COMPILER CERTIFICATION**
Kartik Mohanram[1], Matthew Wartell[1] and Sundar Iyer[2]
[1]University of Pittsburgh, US, [2]Memoir Systems, US

IP5-9 **EXPLOITING REPLICATED CHECKPOINTS FOR SOFT ERROR DETECTION AND CORRECTION**
Fahrettin Koc, Kenan Bozdas, Burak Karsli and Oguz Ergin
TOBB University of Economics and Technology, TR

IP5-10 **AN INTEGRATED APPROACH FOR MANAGING THE LIFETIME OF FLASH-BASED SSDs**
Sungjin Lee, Taejin Kim, Ji-Sung Park and Jihong Kim
Seoul National University, KR

IP5-11 **SCHEDULING INDEPENDENT LIVENESS ANALYSIS FOR REGISTER BINDING IN HIGH LEVEL SYNTHESIS**
Vito Giovanni Castellana and Fabrizio Ferrandi
Politecnico di Milano, IT

IP5-12 **FAST SHARED ON-CHIP MEMORY ARCHITECTURE FOR EFFICIENT HYBRID COMPUTING WITH CGRAS**
Jongeun Lee, Yeonghun Jeong and Sungsok Seo
UNIST, KR

IP5-13 **COMPILING CONTROL-INTENSIVE LOOPS FOR CGRAS WITH STATE-BASED FULL PREDICATION**
Kyuseung Han[1], Jongeun Lee[2], Kiyoung Choi[1]
[1]Seoul National University, KR [2]UNIST, KR

IP5-14 **FAULT-TOLERANT ROUTING ALGORITHM FOR 3D NoC USING HAMILTONIAN PATH STRATEGY**
Masoumeh Ebrahimi, Masoud Daneshtalab and Juha Plosila
University of Turku, FI

IP5-15 **MODELING AND ANALYSIS OF FAULT-TOLERANT DISTRIBUTED MEMORIES FOR NETWORKS-ON-CHIP**
Abbas BanaiyanMofrad[1], Gustavo Girão[2] and Nikil Dutt[1]
[1]University of California, Irvine, US
[2]Federal University of Rio Grande do Sul, BR

IP5-16 **HYBRID PROTOTYPING OF MULTICORE EMBEDDED SYSTEMS**
Ehsan Saboori and Samar Abdi
Concordia University, CA

IP5-17 **LARGE-SCALE FLIP-CHIP POWER GRID REDUCTION WITH GEOMETRIC TEMPLATES**
Zhuo Feng Michigan Technological University, US

IP5-18 **A NETWORK-FLOW BASED ALGORITHM FOR POWER DENSITY MITIGATION AT POST-PLACEMENT STAGE**
Sean Shih-Ying Liu, Ren-Guo Luo and Hung-Ming Chen
National Chiao Tung University, TW

IP5-19 **AN EFFICIENT WIRELENGTH MODEL FOR ANALYTICAL PLACEMENT**
B.N.B. Ray and Shankar Balachandran
Indian Institute of Technology, Madras, IN

12.1 SPECIAL DAY 2 - HOT TOPIC: Internet of Energy – Connecting Smart Mobility in the Cloud

Room - Oisans 1600-1730

Organiser: Ovidiu Vermesan, SINTEF, NO

Chair: Andrea Acquaviva, Politecnico di Torino, IT
Co-Chair: Marcello Coppola, STMicroelectronics, FR

The Internet of Energy (IoE) provides an innovative concept for power distribution, energy storage, grid monitoring and communication. It will allow units of energy to be transferred when and where it is needed. Power consumption monitoring will be performed on all levels, from local individual devices up to national and international level. In this context the new smart electric mobility vehicles will be integrated in the Internet of Energy, creating new mobile ecosystems based on trust, security and convenience to mobile/contactless services and transportation applications will ensure security, mobility and convenience to consumer-centric transactions and services. This special session/workshop will provide different views on the smart mobility concepts and future electric mobility trends by addressing the interaction with the smart city environments in creating an intelligent energy network platform for sustainable transportation systems.

1600 **INTERACTIONS OF LARGE SCALE EV MOBILITY AND VIRTUAL POWER PLANTS**
Randolf Mock Siemens, DE

1615 **INNOVATIVE ENERGY STORAGE SOLUTIONS FOR FUTURE ELECTRO MOBILITY IN SMART CITIES**
Kevin Green Qinetiq, UK

1630 **AUTOMOTIVE ETHERNET: IN-VEHICLE NETWORKING AND SMART MOBILITY**
Peter Hank, Thomas Suermann and Steffen Müller
NXP Semiconductors, DE

1645 **SMART, CONNECTED AND MOBILE: ARCHITECTING FUTURE ELECTRIC MOBILITY ECOSYSTEMS**
Ovidiu Vermesan, Lars-Cyril Blystad and Roy Bahr - SINTEF, NO
Reiner John - Infineon Technologies, DE
Peter Hank - NXP Semiconductors, DE
Alessandro Moscatelli - STMicroelectronics, IT

1700 **E-MOBILITY THE NEXT FRONTIER FOR AUTOMOTIVE INDUSTRY**
Roberto Zafalon - STMicroelectronics, IT
Giovanni Coppola - Enel distribuzione, IT
Ovidiu Vermesan - SINTEF, NO

1715 **SEMICONDUCTOR TECHNOLOGIES FOR SMART MOBILITY MANAGEMENT**
Reiner John and Martin Schulz - Infineon Technologies, DE
Ovidiu Vermesan - SINTEF, NO
Kai Kriegel - Siemens, DE

1730 **CLOSE**

12.2 Methodologies to Improve Yield, Reliability and Security in Embedded Systems

Room - Belle-Etoile 1600-1730

Chair: Luciano Lavagno, Politecnico di Torino, IT
Co-Chair: Jürgen Teich, University of Erlangen-Nuremberg, DE

The first paper in the session discusses how to selectively duplicate hardware in order to optimize yield in a binning scenario. The second paper also uses duplication and re-execution to optimize software reliability by taking error masking into account. Finally the third paper considers variable levels of security and intrusion detection, while satisfying tight performance constraints both at design and at run-time.

1600 **A NEW PARADIGM FOR TRADING OFF YIELD, AREA AND PERFORMANCE TO ENHANCE PERFORMANCE PER WAFER**
Yue Gao, Melvin Breuer and Yanzhi Wang
University of Southern California, US

1630 **LEVERAGING VARIABLE FUNCTION RESILIENCE FOR SELECTIVE SOFTWARE RELIABILITY ON UNRELIABLE HARDWARE**
Semeen Rehman, Muhammad Shafique, Pau Vilimelis Aceituno, Florian Kriebel, Jian-Jia Chen and Jörg Henkel
Karlsruhe Institute of Technology, DE

1700 **OPTIMIZATION OF SECURE EMBEDDED SYSTEMS WITH DYNAMIC TASK SETS**
Ke Jiang, Petru Eles, Zebo Peng
Linköping University, SE

1730 **CLOSE**

12.3 NoC Mapping and Synthesis

Room - Stendhal 1600-1730

Chair: Andreas Hansson, ARM, UK
Co-Chair: Jaime Murillo, EPFL, CH

This session optimizes NoC performance by means of design-time algorithms. Two of the papers focus on mapping of applications on NoCs, while the third proposes new means of synthesizing efficient NoC topologies.

1600 **SHARED MEMORY AWARE MPSoC SOFTWARE DEPLOYMENT**
Timo Schönwald[1], Alexander Viehl[1], Oliver Bringmann[2] and Wolfgang Rosenstiel[2]
[1]Forschungszentrum Informatik, DE
[2]Universität Tübingen, DE

1630 **FAST AND OPTIMIZED TASK ALLOCATION METHOD FOR LOW VERTICAL LINK DENSITY 3-DIMENSIONAL NETWORKS-ON-CHIP BASED MANY CORE SYSTEMS**
Haoyuan Ying[1], Thomas Hollstein[2] and Klaus Hofmann[1]
[1]Darmstadt University of Technology, DE
[2]Tallinn University of Technology, EE

1700 **A SPECTRAL CLUSTERING APPROACH TO APPLICATION-SPECIFIC NETWORK-ON-CHIP SYNTHESIS**
Vladimir Todorov[1], Daniel Mueller-Gritschneder[2], Helmut Reinig[1] and Ulf Schlichtmann[2]
[1]Intel Mobile Communications, DE
[2]Technische Universitaet Muenchen, DE

1730 **CLOSE**

12.4 Emerging Logic

Room - Chartreuse 1600-1730

Chair: Aida Todri-Sanial, CNRS-LIRMM, FR
Co-Chair: Marco Ottavi, University of Rome "Tor Vegata", IT

This session contains papers on emerging logic including nano-magentic logic, graphene FETs, nano-corssbar arrays, and single-electron transistors

1600 **A SPICE-COMPATIBLE MODEL OF GRAPHENE NANO-RIBBON FIELD-EFFECT TRANSISTORS ENABLING CIRCUIT-LEVEL DELAY AND POWER ANALYSIS UNDER PROCESS VARIATION**
Ying-Yu Chen[1], Artem Rogachev[1], Amit Sangai[1], Giuseppe Iannaccone[2], Gianluca Fiori[2] and Deming Chen[1]
[1]University of Illinois at Urbana-Champaign, US
[2]University of Pisa, IT

1630 **SYSTEMATIC DESIGN OF NANOMAGNET LOGIC CIRCUITS**
Indranil Palit, Michael Niemier, Xiaobo Hu and Joshep Nahas
University of Notre Dame, US

1700 **DEFECT-TOLERANT LOGIC HARDENING FOR CROSSBAR-BASED NANO-SYSTEMS**
Yehua Su and Wenjing Rao
University of Illinois at Chicago, US

1715 **ON RECONFIGURABLE SINGLE-ELECTRON TRANSISTOR ARRAYS SYNTHESIS USING REORDERING TECHNIQUES**
Chang-En Chiang[1], Li-Fu Tang[1], Chun-Yao Wang[1], Ching-Yi Huang[1], Yung-Chih Chen[2], Suman Datta[3], and Vijaykrishnan Narayanan[3]
[1]National Tsing Hua University, TW
[2]Yuan Ze University, TW
[3]Pennsylvania State University, US

1730 **CLOSE**

12.5 Emerging Technology Architectures for Energy-Efficient Memories

Room - Meije 1600-1730

Chair: Marisa López-Vallejo, Universidad Politecnica Madrid, ES
Co-Chair: Naehyuck Chang, Seoul National University, KR

This session presents three papers targeting energy efficiency in memory architectures. The first paper presents a new hybrid DRAM/MRAM approach, the second paper describes a sensitivity analysis to simulate SRAMs dynamic write-ability under process variations and the third one reports how domain wall memories can be used for design on-chip cache hierarchies.

1600 **D–MRAM CACHE: ENHANCING ENERGY EFFICIENCY WITH 3T–1MTJ DRAM / MRAM HYBRID MEMORY**
Hiroki Noguchi[1], Kumiko Nomura[1], Keiko Abe[1], Shinobu Fujita[1], Eishi Arima[2], Kyundong Kim[2], Takashi Nakada[2], Shinobu Miwa[2] and Hiroshi Nakamura[2]
[1]Toshiba, JP [2]University of Tokyo, JP

1630 **LEVERAGING SENSITIVITY ANALYSIS FOR FAST, ACCURATE ESTIMATION OF SRAM DYNAMIC WRITE Vmin**
James Boley[1], Vikas Chandra[2], Robert Aitken[2] and Benton Calhoun[1]
[1]University of Virginia, US, [2]ARM, US

1700 **DWM-TAPESTRI - AN ENERGY EFFICIENT ALL-SPIN CACHE USING DOMAIN WALL SHIFT BASED WRITES**
Rangharajan Venkatesan, Mrigank Sharad, Kaushik Roy and Anand Raghunathan
Purdue University, US

1730 **CLOSE**

12.6 Clock Distribution and Analogue Circuit Synthesis

Room - Bayard 1600-1730

Chair: Tiziano Villa, University of Verona, IT
Co-Chair: Georges Gielen, Katholieke Universiteit Leuven, BE

The first two papers of this session address the optimization of clock distribution. The first paper deals with clock-skew scheduling combined with clock-gating. The second paper addresses the power reduction of the clock-tree using multi-bit flip-flops. The last two papers of this session address the synthesis of analogue circuits, dealing with hierarchy, layout issues, and non-CMOS technologies.

1600 **CO-SYNTHESIS OF DATA PATHS AND CLOCK CONTROL PATHS FOR MINIMUM-PERIOD CLOCK GATING**
Wen-Pin Tu, Shih-Hsu Huang and Chun-Hua Cheng
Chung Yuan Christian University, TW

1630 **SLACK BUDGETING AND SLACK-TO-ENGTH CONVERTING FOR MULTI-BIT FLIP-FLOP MERGING**
Chia-Chieh Lu and Rung-Bin Lin
Yuan Ze University, TW

1645 **AREA OPTIMIZATION ON FIXED ANALOG FLOORPLANS USING CONVEX AREA FUNCTIONS**
Ahmet Unutulmaz[1], Gunhan Dundar[1] and Francisco Fernandez[2]
[1]Bogazici University, TR,
[2]IMSE-CNM, CSIC and University of Sevilla, ES

1700 **PAGE: PARALLEL AGILE GENETIC EXPLORATION TOWARD UTMOST PERFORMANCE FOR ANALOG CIRCUIT DESIGN**
Po-Cheng Pan, Hung-Ming Chen and Chien-Chih Lin
National Chiao Tung University, TW

1730 **CLOSE**

12.7 Physical Design

Room - Les Bans 1600-1730

Chair: Carl Sechen, University of Texas at Dallas, US
Co-Chair: Bill Swartz, InternetCAD, US

The first paper proposes solving the Lagrangian dual problem using discrete gate sizes. The second paper describes accurate meta-modelling techniques applicable to IC design. The third paper suggests better wire lengths in placement are obtained using a super-linear weighting factor. The last paper shows the advantages of doing layer assignment before global routing.

1600 **FAST AND EFFICIENT LAGRANGIAN RELAXATION-BASED DISCRETE GATE SIZING**
Vinicius dos S. Livramento[1], Chrystian Guth[1], José Luís Güntzel[1] and Marcelo O. Johann[2]
[1]Federal University of Santa Catarina, BR
[2]Federal University of Rio Grande do Sul, BR

1630 **ENHANCED METAMODELING TECHNIQUES FOR HIGH-DIMENSIONAL IC DESIGN ESTIMATION PROBLEMS**
Andrew B. Kahng, Bill Lin and Siddhartha Nath
University of California, San Diego, US

1700 **SUB-QUADRATIC OBJECTIVES IN QUADRATIC PLACEMENT**
Markus Struzyna University of Bonn, DE

1515 **CATALYST: PLANNING LAYER DIRECTIVES FOR EFFECTIVE DESIGN CLOSURE**
Yaoguang Wei[1], Zhuo Li[2], Cliff Sze[2], Shiyan Hu[3], Charles J. Alpert[2] and Sachin S. Sapatnekar[1]
[1]University of Minnesota - Twin Cities, US,
[2]IBM Austin Research Laboratory, US
[3]Michigan Technological University, US

1730 **CLOSE**

12.8 EMBEDDED TUTORIAL: Closed-Loop Control for Power and Thermal Management in Multi-core Processors: Formal Methods and Industrial Practice

Room - Lesdigiueres (Exhibition Theatre) 1600-1730

Organiser:
Ibrahim Elfadel - Masdar Institute of Science and Technology, AE

Chair: Petru Eles, Linköping University, SE
Co-Chair: Jose Ayala, Complutense University of Madrid, ES

The objective of this embedded tutorial is to bring DATE attendees who are interested in low-power design for MPSoC to the forefront of the latest academic research and industrial practice in the area of closed-loop control of power and temperature in MPSoC. Starting with power capping techniques based on classical control theory, the tutorial will cover the more advanced techniques of optimal control, model predictive control, and adaptive control. Practical issues such as power and thermal proxies, power and thermal sensors, and various actuation techniques will be surveyed. Furthermore, the tutorial will cover recent techniques for pro-active and reactive closed-loop temperature control for 2D and 3D MPSoC, including the handling of emerging inter-tier liquid cooling techniques. It will also address optimal power control techniques in NoC architectures, with particular attention to methods for handling multiple voltage and clock domains under variable workloads. Important emerging problems such as heterogeneity of the computational fabric and scalability of the control methods will also be discussed along with their emerging solutions.

1600 **CLOSED-LOOP CONTROL FOR POWER AND THERMAL MANAGEMENT IN MULTI-CORE PROCESSORS**
Ibrahim Elfadel[1], Radu Marculescu[2], David Atienza[3]
[1]Masdar Institute of Science and Technology, AE
[2]Carnegie Mellon University, US [3]EPFL, CH

1730 **CLOSE**

friday workshops

Co-Chairs:
Lorena Anghel, TIMA, FR
Cristiana Bolchini, Politecnico di Milano, IT

The DATE Friday's Workshops initiative was first introduced in 2003 and, since then, the workshops topics have diversified and the participation has increased to over 280 researchers and designers, attending eight workshops at DATE 2012.

This initiative has now become an integral part of the conference, offering workshops on current and emerging important issues in design, test, EDA and software, to complement the regular conference programme running throughout the week. They provide a unique opportunity for the various research and design communities to spend a day discussing the latest and the best outcomes, sharing their experiences and visions.

The Friday's Workshops programme for DATE 2013 includes nine workshop themes, ranging from embedded systems to 3D integration. The broad embedded systems field, of growing interest to the DATE community, is covered by three workshops focused on embedded parallel computing platforms, platform 2012/STHORM embedded many cores accelerations, and reconfigurable computing. One workshop is focused on methods for system-level design, in particular on the integration of SystemC Design and Verification with AMS and Algorithm Design. Building on the success from the previous four years, the 3D integration workshop covers a broad spectrum of topics from technology and test to chip package and board co-design challenges. For attendees interested in the reliability and resilient design through software approaches, two workshops will discuss the lessons learned from large multi-institutional research programs. For the first time at DATE, the workshop entitled Neuromorphic and Brain-Based Computing Systems is proposed to discuss new/emerging areas relevant to the electronic design automation community. Finally a workshop focusing on Industry-Driven Approaches for Cost-effective Certification of Safety-Critical, Mixed-Criticality Systems (WICERT) aims at gathering a strong industrial community to discuss and evaluate new HW/SW architectures and mechanisms and safety guidelines to achieve a more cost-effective, precise, and scalable certification.

Friday's Workshops attendees should choose in advance one workshop among W1, W2, W3, W4, W5, W6, W7, W8 or W9. The workshops run from 08:15 until 17:00. The individual timetables for each workshop may vary, and for the detailed version of the workshop programmes, visit the following workshop pages.

W1

ESCUG 2013: ESL - Putting the Pieces Together: Integrating SystemC Design and Verification with AMS and Algorithm Design

Room – Meije 2 0830 - 1630

Organisers:
Axel Braun, European SystemC Users' Group & U Tuebingen, DE
Wolfgang Rosenstiel, U Tuebingen, DE

Description: This workshop is focused on the integration of SystemC design and verification with AMS and algorithm design. It gives deep insights in how techniques may collaborate and converge. These topics gain more and more interest, because a seamless integration of all relevant design and verification techniques is crucial. Besides digital hardware design, this is substantially important for the areas of algorithm and AMS design.

0830 **Welcome and Opening**
Axel Braun, European SystemC Users' Group & U Tuebingen, DE

0835 **Keynote Session: Multi Physical Domain Applications Challenges: Design Flow integration**
Serge Scotti - STMicroelectronics, FR

0900 **Design Methodology Session: Towards Co-Design of HW/SW/AMS System**
Christoph Grimm - TU Kaiserslautern, DE

1000 **Coffee Break**

1030 **Virtual Prototyping Session: Virtual Prototyping for High Performance Mixed Signal Products**
Martin Barnasconi - NXP, NL

1130 **SystemC AMS Session 1: AMS IP Handling and Simulation**
Karsten Einwich - Fraunhofer IIS, DE

1200 **Lunch Break**

1300 **SystemC AMS Session 2: AMS IP Handling and Simulation**
Karsten Einwich - Fraunhofer IIS, DE

1400 **SystemC TLM Session: Improving Timing Accuracy for TLM-LT Models**
Simon Hufnagel - Bosch, DE

1430 **Coffee Break**

1500 **Town Hall Meeting Session: Interactive Discussion on "ESL Integration Experience"**
Axel Braun, European SystemC Users' Group & U Tuebingen, DE

1620 **Wrap-Up & Closing**

W2 1st RIIF Workshop - Towards Standards for Specifying and Modeling the Reliability of Complex Electronic Systems

Room – Stendhal 0830 -1600

Organisers:
Adrian Evans, IRoC Technologies, FR
Oliver Bringmann, FZI / Tübingen University, DE
Viacheslav Izosimov, Semcon, SE

Description: Complex silicon devices are increasingly controlling critical systems where safety and reliability are key concerns. Silicon technology is subject to numerous failure modes which can be broadly classified into soft- error effects (due to natural radiation) and life-time effects (e.g. electro-migration, NBTI, HCI). It is necessary to consider all of these failure modes and how they propagate through the system and produce user-visible effects. There are no consistent tools or methodologies to address this problem. Current ad-hoc approaches are not able to cope with the diversity of technology failure modes, increased design sizes and the complex industrial relationships between consumers and suppliers of electronic components. RIIF (Reliability Information Interchange Format), is an initiative to develop a standard modeling approach for specifying the failure mechanisms in silicon devices and systems built using these devices. One of the main goals of the workshop is to establish the requirements for RIIF and assess the current implementation.

0830 **Session 1: Opening**

Introduction to the RIIF Initiative
Adrian Evans - iROC Technologies, FR

0850 **Session 2: Processor Reliability**

Improving Server Reliability – A Front-End Design Engineering Perspective
Burcin Aktan - Intel, US

0925 **Reliability Availability Serviceability (RAS) of IBM POWER & Mainframe (z) Servers**
Michael Müller - IBM, DE

1000 **Reliability Modeling Challenges – An IP Provider's Perspective**
Peter Harrod - ARM, UK

1030 **Coffee Break**

1100 **Session 3: Reliability in Automotive Applications**

Reliability Modeling for Automotive Semiconductors
Göran Jerke - Bosch, DE

1120 **Embedded Tutorial : Using RIIF to Model a Complex Automotive System**
Viacheslav Izosimov - Semcon, SE

1140 **Robustness Metrics for Automotive Power Microelectronics**
Thomas Nirmaier - Infineon, DE

1200 **Lunch Break**

1300 **Session 4: Modeling and Dependability**

From Component Reliability to System Dependability: A Modeling and Assessment Perspective
Jean Arlat - LAAS/CNRS, FR

1325 **Session 5: Panel Discussion**

Can RIIF Address The Reliability Modeling Gap?
David Appello - ST, FR
Jean Arlat - LAAS/CNRS, FR
Michael Müller - IBM, DE
Michael Nicolaidis - TIMA Laboratory, FR
Göran Jerke - Bosch, DE
Ulf Schlichtmann - Technische Universität München, DE

1425 **Session 6: Poster Session / Coffee Break**

1445 **Session 7: Reliability Analysis and Optimization**

Towards Near Zero Cost of Fault Tolerance for Reliable Low Power Designs
Saquib Khursheed - University of Southampton, UK

1505 **System-Level Reliability Modeling for MPSoCs**
Thidapat Chantem - Utah State University, US

1520 **Session 8: Next Steps for RIIF**

IEEE Standardization, Case Studies, Working Protocols

1550 **Closing Remarks**
Oliver Bringmann - FZI / Tübingen University, DE

W3

International Workshop on Neuromorphic and Brain-Based Computing Systems (NeuComp 2013)

Room – Oisans 0830 -1630

Organisers:
Philippe Coussy, Université de Bretagne-Sud/Lab-STICC, FR
Nikil Dutt, University of California, US

Technical Program Committee Co-Chairs:
Jeff Krichmar, University of California, US
Philippe Coussy, Université de Bretagne-Sud/Lab-STICC, FR

Description: Biological neural systems are well known for their robust and power-efficient operation in highly noisy environments. Biological circuits are made up of low-precision, unreliable and massively parallel neural elements with highly reconfigurable and plastic connections. Two of the most interesting properties of the neural systems are its self-organizing capabilities and its template architecture. Recent research in biologically-plausible neural networks has demonstrated interesting principles about learning and neural computation. Understanding and applying these principles to practical problems is only possible if large-scale neural simulators or circuits can be constructed. This workshop will outline key modelling abstractions for the brain and focus on recent neural network models. Aspects of neuronal processing and computational issues related to modelling these processes will be discussed. Hardware and software solutions readily usable by neuroscientists and computer scientists and efficient enough to construct very large networks comparable to brain networks will be presented.

0830 **Welcome and introduction**
Organiser(s):
Nikil Dutt - University of California, US
Philippe Coussy - Université de Bretagne-Sud/ Lab-STICC, FR

0835 **Brain: principles & modeling abstractions**
Jeff Krichmar - University of California, US

0900 **Session 1**

Simulating the brain without a computer - Achievements and Challenges of Brain Inspired Computing
Karlheinz Meier - Heidelberg University, DE

0930 **Neuromorphic Visual Systems on FPGAs**
Vijaykrishnan Narayanan -
Pennsylvania State University, US

1000 **Break & Poster/demo session 1**

1100 **Session 2**

When neural networks meet error-correction coding: new perspectives in associative memories
Claude Berrou - Telecom Bretagne / Lab-STICC, FR

1130 **The emergent microconnectome of neocortical circuitry**
Sean Hill - INCF, US

1200 **Lunch Break**

1300 **Session 3**

SpiNNaker: a Biologically-Inspired Massively-Parallel Architecture
Steve Furber - Manchester University, UK

1330 **Hierarchical event-based reconfigurable systems for cognitive neuromorphic engineering**
Emre Neftci and Gert Cauwenberghs - UCSD, US

1400 **Break & Poster/demo session 2**

1500 **Session 4**

UPSIDE – Unconventional Processing of Signals for Intelligent Data Exploitation
Dan Hammerstrom - DARPA, US

1530 **A Scalable Analog Neuromorphic Learning System**
Narayan Srinivasa - HRL, US

1600 **A closed-loop neurobotic system for fine touch sensing**
Angelo Arleo - Université Pierre et Marie Curie, FR

1630 **Wrap up and close**
Nikil Dutt - University of California, US
Philippe Coussy - Université de Bretagne-Sud/ Lab-STICC, FR

W4 Platform 2012 / STHORM embedded many-core acceleration

Room – Chartreuse 0830 - 1630

Organisers:
Diego Melpignano, STMicroelectronics, IT
Luca Benini, STMicroelectronics and U Bologna, IT
Fabien Clermidy, CEA, FR

Description: Platform 2012 / STHORM is a many-core embedded architecture that has been designed by STMicroelectronics and by CEA as a scalable and customizable acceleration device. A test chip in 28nm is being sampled now, featuring 69 processors in less than 20 mm2. The STHORM development environment is being used by a community of researchers that have been implementing many parallel applications, programming models and runtime solutions with it.

0830 **Opening of the workshop**
Diego Melpignano - STMicroelectronics, IT

0850 **ST perspectives on programmable accelerators for embedded vision**
Éric Flamand - STMicroelectronics, FR

0920 **CEA vision on multicores architecture evolution**
Thierry Collette - CEA, FR

0950 **Coffee Break**

1020 **Implementation of an Accurate Canny Edge Detector on Platform 2012**
Gabriela Nicolescu et al. -
École Polytechnique de Montréal, CA

1040 **An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to P2012**
Vittorio Zaccaria et al. - Politecnico di Milano, IT

1100 **Complex Embedded Vision Application**

1120 **FPGA mapping of STHORM, an experimental testbed for the research community**
Yassine Hariri - CMC Microsystems, CA
Peter Stokes - CMC Microsystems, CA

1140 **Leveraging HW IPs in shared memory STHORM clusters**
Andrea Marongiu - University of Bologna, IT

1200 **Lunch + demonstrations + posters**

1300 **Evaluating Software Managed Memory with MapReduce**
Alexandra Fedorova et al. - Simon Fraser University, CA

1320 **Porting Applications to Multicore Platforms: Results from the BIP & MCAPI Tool Chain for STHORM**
Julien Mottin - CEA, FR
Marius Bozga et al. - VERIMAG, FR

1340 **Thermal Modeling of Deep Nano-Meter Heterogeneous Many-Core Platforms**
David Atienza - EPFL, CH

1400 **STHORM demos: Object Recognition and Face detection**

1430 **Coffee Break + poster sessions**

1500 **Run-Time Resource Management on Many-Core STHORM Platform**
Patrick Bellasi - Politecnico di Milano, IT

1520 **Dynamic Voltage and Frequency Management under Thermal Constraints in SoC: Towards an Event-Based Approach**
Suzanne Lesecq et al. - CEA, FR

1540 **Supporting dataflow CAL language on STHORM**
Marco Mattavelli - EPFL, CH

1600 **Kernel Genius: a novel approach to vision code generation**
Thierry Lepley - STMicroelectronics, FR

1620 **Conclusions of the workshop**

W5 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test

Room – Bayard 0830 - 1640

Organisers:
Qiang Xu, The Chinese University of Hong Kong, HK
Saqib Khursheed, University of Southampton, UK

Program Co-Chairs:
Terrence Mak, The Chinese University of Hong Kong, HK
Said Hamdioui, Delft University of Technology, NL

Description: 3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. To produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges..

0830 **Session 1: Opening**
Bjørn B. Larsen - NTNU, NO

0840 **Keynote Address: 3D IC Design and CAD Research: Challenges and Opportunities**
Sung Kyu Lim - Georgia Tech, US

0925 **Invited Talk: 3D IC Test Challenges and Solutions**
Erik Jan Marinissen - IMEC, BE

1000 **Session 2: Posters**

1030 **Session 3: Design, Manufacturing and Test of 3D-Ics**
Moderator: Haykel Ben Jamaa - CEA-LETI, FR

Silicon Interposers with Through Silicon Vias - A Base Approach for 3D Wafer Level System Integration
Kai Zoschke, Rene Puschmann and Juergen Wolf - Fraunhofer IZM, DE
Oswin Ehrmann and Klaus-Dieter Lang - Technical U of Berlin, DE

1053 **Thermal-aware Energy Efficient Run-Time Incremental Mapping for 3-D Networks-on-Chips**
Xiaohang Wang - Guangzhou Ins. of Adv. Tech., CN
Mei Yang and Yingtao Jiang - U of Nevada, US
Maurizio Palesi - Kore U, IT
Terrence Mak - The Chinese U of Hong Kong, HK

1115 **3D MPSoC Design Using 2D EDA tools: Analysis of Parameters**
Mohamad Jabbar - GIPSA-Lab/ENSTA Paristech, FR
Abir M'Zah and Omar Hammami - ENSTA Paristech, FR
Dominique Houzet - GIPSA-Lab, FR

1138 **Pre-bond Test of TSVs in 3D SICs using Ring Oscillators**
Yassine Fkih - CEA, Leti/LIRMM U Montpellier II, FR
Pascal Vivet - CEA-Leti, FR
Bruno Rouzeyre, Marie-Lise Flottes and
Giorgio Di Natale - LIRMM U Montpellier II, FR

1200 **Lunch Break**

1300 **Session 4: Performance, Reliability and Cost Modelling of 3D Ics**
Moderator: Rishad A. Shafik - University of Bristol, UK

MoNICA: A Performance- and Thermal-Aware Floorplan Tool for Heterogeneous 3D NoC-based MPSoCs
Felipe Frantz, Lioua Labrak and Ian O'Connor - Lyon Inst. of Tech., FR
da Silva Matos, Luigi Carro and Altamiro Susin - Federal U of Rio Grande do Sul, BR
Fabien Clermidy - CEA-LETI, FR

1323 **Short-Circuit Current Free NEMFET Based Logic and NEMFET-MOS Hybrid 3D Memory**
Marius Enachescu, Mihai Lefter, George Razvan Voicu and Sorin Cotofana - Delft U of Tech., NL

1345 **3D-COSTAR: A Cost Model for 3D Stacked Ics**
Mottaqiallah Taouil and Said Hamdioui - Delft U of Tech., NL, Erik Jan Marinissen - IMEC, BE
Sudipta Bhawmik - Qualcomm, US

1408 **WIOMING, a Low Power Wide IO compatible 3D circuit**
Denis Dutoit, Pascal Vivet and Alexandre Valentian - CEA, FR

1430 **Coffee Break & Posters**
(list available online)

1500 **Session 6: Invited Talk**
Moderator: Denis Dutoit - CEA-LETI, FR

3D Design Methodology - A Trifecta of Options
Steve Carlson - Cadence, US

1540 **Workshop: Session 7: Panel Discussion**
Moderator: Pascal Vivet - CEA-Leti, FR

2.5D vs 3D: Who is winning and why?
Paul Franzon - University North Carolina, US
Georg Kimmich - STEricsson, FR
Juan Rey - Mentor Graphics, US
Ravi Varadarajan - Atrenta, FR

1640 **Close**

W6 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications

Room – Berlioz 0830 - 1630

General Co-Chairs:
João Cardoso, Universidade do Porto, PT
Cristina Silvano, Politecnico Milano, IT
Dimitrios Soudris, National Technical University of Athens, GR

Description: Embedded computing is shifting to multi/many-core designs to boost performance due to unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence, embedded system designers are increasingly faced with several big challenges, namely: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant design issues:

• How can applications that exploit the underlying (parallel) architecture be written without burdening the application designer?

• What does the application designer really need to know of the underlying architecture?

• What tools are needed to efficiently map applications and what part of the mapping process should/could be automated?

• How should we design and optimize the underlying architectures?

This workshop brings together researchers and practitioners actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

Topic Areas:

The workshop will have three main topic areas:

• Architectures: on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.

• Design tools: on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.

• Applications: on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

0830 **Opening Session**
General Co-Chairs:
João Cardoso - Universidade do Porto, PT
Cristina Silvano - Politecnico Milano, IT,
Dimitrios Soudris -
National Technical University of Athens, GR

0845 **Morning Session on Many-Core Architectures and Compilers**

Invited Talk: "Multiprocessor Systems for H.264/AVC video encoding: A platform approach"
Sri Parameswaran - University of New South Wales, AU

0945 **Invited Talk: "C Compilation in the Dark Age of Many-Core Programming"**
Marcel Beemster - ACE Associated Compiler Experts, NL

1030 **Coffee Break & Posters**
(list available online)

1100 **Panel: Embedding High Performance Computing: A supercomputer in your pocket or ultra low power exaflop design?**

Panel Organizer and Moderator(s):
Georgi Gaydadjiev - Chalmers University of Technology, SE

Panelist(s):
Todd Austin - The University of Michigan, US
John Goodacre - ARM, UK
Andreas Moshovos - University of Toronto, CA
Alex Ramirez - Barcelona Supercomputing Center, ES
Eugenio Villar - University of Cantabria, ES

1200 **Lunch Break**

1300 **Workshop: Afternoon Session on Design Tools and Applications for Many-Core Architectures**

Invited Talk: "The role of runtime system management in dynamic execution environments"
Dionisios Pnevmatikatos,
Technical University of Crete, GR

1400 **Coffee Break & European Projects Parallel Demos**
(list available online)

1430 **Panel on: "Lessons learnt from European Projects: 2PARMA, COMPLEX, DESYRE, ERA, FASTER, MADNESS, PARAPHRASE, REFLECT, SMECY and TERAFLUX"**
William Fornaciari - Politecnico di Milano, IT
Georgi Gaydadjiev -
Chalmers University of Technology, SE
Philipp A. Hartmann - OFFIS, DE
Stephan Wong - TU Delft, NL
Dionisios Pnevmatikatos -
Technical University of Crete, GR
Luigi Raffo - Università di Cagliari, IT
Kevin Hammond - University of St. Andrews, UK
Zlatko Petrov - Honeywell, CZ
Francois Pacull - CEA, FR
Roberto Giorgi - Università di Siena, IT

1530 **Design Tools and Application -- Posters Session**
(list available online)

1630 **Final Wrap up**

W7 Reconfigurable Computing V2.0: The Next Generation of Technology, Architectures and Design Tools

Room – Les Bans 0830 - 1600

Organisers:
Diana Göhringer, KIT, DE
Michael Hübner, Ruhr-U Bochum, DE

Description: Reconfigurable computing gained interest in the scientific and industrial community many years ago. It targeted the substitution of application specific integrated circuits (ASICs) by offering additional benefits, such as flexibility at design- and runtime. Since this time, various trends were followed and led to different generalizations and specializations e.g. through the offer of specific chips with more digital signal processing units or more logic cells or even embedded processors such as the Power PC 405 in Xilinx Virtex II Pro Field Programmable Gate Array (FPGA). In the meanwhile, other technologies such as Graphic Processing Units (GPUs) entered the marked and established themselves in the domain of high performance computing and nowadays also in embedded computing. However, the vendors of FPGAs continued improving the architectures, and the technology of their devices as well as the design tools and programming environments. Novel high performance architectures such as the Xilinx Zynq or Microsemi Smart Fusion, tailored for the embedded market, are some examples that the FPGA market is still growing. Virtual development platforms such as provided e.g. from Cadence enable an efficient design of complex systems without building a prototype in early stages of the development phase. Especially, this example shows how former hurdles will be bridged by introducing novel development tools for the chips which could be programmed in former times only by specialists. The introduction of novel technologies like MRAM, FRAM and also MEMRISTOR will further revolutionize the FPGA hardware and lead to a new era of reconfigurable computing.

0830 **Welcome Session**

Chairs:
Diana Göhringer - KIT, DE,
Michael Hübner - Ruhr-U Bochum, DE

0900 **Session 1: System-on-Chip FPGAs from Xilinx and Altera: Novel Architectures and Design Tools**
Diana Göhringer - KIT, DE

FPGA's Entering the Era of All Programmable SoCs
Ivo Bolsens - Xilinx, US

0945 **High Level Design Convergence for SoC FPGAs**
Steven Perry - Altera, UK

1000 **Coffee Break & Poster Session**

1100 **Session 2: Flexibility with Embedded FPGAs**
Michael Hübner - Ruhr-U Bochum, DE

1100 **Flexible SoCs with embedded-FPGAs**
Laurent Rougé - Menta, FR

1200 **Lunch Break**

1300 **Session 3: Novel Architectures and Technologies**
Diana Göhringer - KIT, DE

SmartFusion2 for industrial and harsh environment applications
Hichem Belhadj - Microsemi, US

1345 **FPGA goes 3D**
Ahmed Jerraya - CEA Leti, FR

1430 **Coffee Break & Poster Session**

1500 **Interactive Panel**

Organiser:
Michael Hübner - Ruhr-U Bochum, DE

Interactive Panel
Ivo Bolsens - Xilinx, US
Steven Perry - Altera, UK
Laurent Rougé - Menta, FR
Ahmed Jerraya - CEA Leti, FR
Hichem Belhadj - Microsemi, US

1600 **Closing Session**
Diana Göhringer - KIT, DE
Michael Hübner - Ruhr-U Bochum, DE

W8 Workshop on Industry-Driven Approaches for Cost-effective Certification of Safety-Critical, Mixed-Criticality Systems (WICERT)

Room – Belle-Etoile 0830 - 1630

Organisers:
Jarkko Mäkitalo, KONE Oij
Rolf Ernst, TU Braunschweig, DE
Michael Paulitsch, EADS, DE
Javier Díaz Alonso, University of Granada, ES
Simon Brewerton, Infineon Technologies
Huáscar Espinoza, TECNALIA, ES
José Luis Gutiérrez Rivas, University of Granada, ES

Increased complexity of embedded systems implies high certification costs to comply with functional safety standards and regulations. The use of technologies such as for example multi-core and FPGA is particularly a challenge in mixed-criticality configurations. Mixed criticality is the concept of allowing applications at different levels of criticality to interact and co-exist on the same computational platform. In a mixed-criticality system, low-critical and high-critical applications coexist and must therefore share processing time in a safe way. Unfortunately, certification of such systems is more difficult, because it requires that even the components of less criticality be certified at the highest criticality level.

This workshop aims to present and evaluate different industry-driven approaches for reducing certification costs in safety-critical, mixed-criticality systems. In particular, WICERT will provide a platform for industrial demonstrations, thematic presentations and in-depth discussions about new HW/SW architectures and mechanisms and safety guidelines to achieve a more cost-effective, precise, and scalable certification. WICERT aims at bringing together experts, researchers, and practitioners, from diverse communities, such as safety and security engineering, certification processes, model-based technologies, software and hardware design, safety- critical systems and applications communities (aerospace, automotive, industrial manufacturing, health, etc.).

0835 **Workshop Introduction**

Speaker: Huáscar Espinoza - TECNALIA, ES

0845 **Workshop: KEYNOTE 1**

MULCORS - The Use of MULticore proCessORs in airborne Systems. Project EASA.2011.OP.30. (study done for EASA: European Aviation Safety Agency)
Marc Gatti and Guy-Andre Berthon - Thales Avionics, FR

0920 **Session 1: Mixed-criticality HW/SW platforms**
Rolf Ernst - TU Braunschweig, DE

Isolation of Cores
Claus Stellwag - Elektrobit, DE
Swapnil Gandhi and Thorsten Rosenthal - Delphi, DE

0935 **Open platform for mixed-criticality applications**
Miguel Méndez - Seven Solutions, ES
José Luis Gutiérrez Rivas, David Fernández García-Valdecasas and Javier Díaz Alonso - University of Granada, ES

1000 **Servosystem control for theatre stage equipment**
Pavel Zemcik, Sevcovic Jiri, Michal Kajan and Josef Strnadel - Faculty of Information Technology, CZ
Pavol Korcek - Camea, CZ

1015 **Coffee Break**

1045 **Session 2: Certification on aerospace, automotive and automation industries with mixed-criticality**
Uwe Kremer - TÜV, DE

Hardware and Software Support for Mixed-Criticality Multicore Systems
Glenn Farrall - Infineon, UK
Claus Stellwag - Elektrobit, DE
Jonas Diemer and Rolf Ernst - TU Braunschweig, DE

1110 **IFCIMA - Incremental Functional Certification on Integrated Modular Avionics (IMA)**
Franck Aimé - Thales Avionics, FR

1135 **Impact of multicore platforms in hardware and software certification**
Risto Nevalainen - Spinet, FI
Uwe Kremer - TÜV, DE
Oscar Slotosch - Validas, DE
Dragos Truscan - Åbo Akademi, FI
Vicky Wong - SpaceSystems Finland, FI

1200 **Lunch Break**

1300 **KEYNOTE 2**

Industrial practice on mixed-criticality engineering and certification in the aerospace industry
Ondrej Kotaba - Honeywell, CZ

1330

Session 3: Methods and tools for cost-effective certification of safety critical systems
Huáscar Espinoza - TECNALIA, ES

Methods and tools for reducing certification costs of mixed-criticality applications on multi-core platforms: the RECOMP approach
Paul Pop - Technical University of Denmark, DK
Leonidas Tsiopoulos - Åbo Akademi, FI
Sebastian Voss - fortiss, DE
Oscar Slotosch - Validas, DE
Christoph Ficek - Symtavision, DE
Ulrik Nyman - Aalborg University, DK

1355

Towards Model-Driven Engineering for Mixed-Criticality Systems: MultiPARTES Approach
Christophe Jouvray and Cyril Grepet - Trialog, FR
Salvador Trujillo - Ikerlan-IK4, ES

1420

Multicore In Real-Time Systems – Temporal Isolation Challenges Due To Shared Resources
Ondrej Kotaba - Honeywell, CZ
Michael Paulitsch and Jan Nowotsch - EADS, DE
Stefan Petters - ISEP, PT
Henrik Theiling - SYSGO, DE

1445

Coffee Break

1500

Demonstrators and Poster session: Paralell demonstrators and posters
Simon Brewerton - Infineon Technologies, UK

Mixed-Critical Multi-Processor Motor Controller with Capabilities for Runtime Update of Software
Simon Holmbacka - Åbo Akademi, FI
José Luis Gutiérrez Rivas - University of Granada, ES
Miguel Méndez - Seven Solutions, ES

RECOMP Demonstration of Mixed-Criticality Approach
Claus Stellwag - Elektrobit, DE
Natalia Willey - Delphi , FR
Swapnil Gandhi and Thorsten Rosenthal - Delphi , DE

Emergency Shutdown System Demonstrator
Anton Hattendorf and Sebastian Voss - fortiss, DE

Tools for Compliance Management and Compositional Safety Assurance
Alejandra Ruiz and Huáscar Espinoza - TECNALIA, ES

1615

Wrap Up
Javier Ruiz - University of Granada, ES

W9 International Workshop on Software Approaches to Resilient System Design

Room – Meije 3 0830 - 1630

Organisers:
Puneet Gupta, U California Los Angeles, US
Jörg Henkel, KIT, DE
Medhi Tahoori, KIT, DE

Embedded systems are integrated into our daily lives, thanks to improvement in the VLSI technology. However, this trend is facing serious challenges, both at device and system levels. At nanoscale device-level, a host of vulnerabilities influence the robustness, reliability, and availability of embedded and critical systems. At the other end of the spectrum, embedded systems are seeing a tremendous increase in software content. Whereas traditional software design paradigms have assumed that the underlying hardware is fully predictable and error-free, there is now a critical need to build a software stack that is responsive to variations, and resilient against emerging vulnerabilities in the underlying hardware.

The objective of this workshop is to bring the attention of design automation community to the multi-level reliability challenges and solutions and possible paradigm shift to consider reliability throughout the design flow, from circuit to system. In addition, this workshop tries to synchronize various existing coordinated research programs on dependability which are currently underway worldwide to deal with these challenges. The goal is to have further collaborations among these programs such that the overall design and test automation community can benefit more from their outcomes.

0830 **Session 1: Opening**

Welcome Address
Mehdi Tahoori - KIT, DE

0845 **Morning Keynote Address**
Robert Aitken - ARM, US

0930 **Session 2: Variability**

Sensing and Emulating Variability
Puneet Gupta - UCLA, US

1000 **Variability Induced Compiler Directed Strategies**
Rajesh Gupta - UCSD, US

1030 **Coffee Break**

1100 **Session 3: Thermal and Aging Effects**

Reliability of On-Chip Systems from a Thermal Perspective
Jörg Henkel - KIT, DE

1130 **Software Approaches for Aging Modeling and Mitigation**
Mehdi Tahoori - KIT, DE

1200 **Lunch Break**

1300 **Session 4: Cross Layer Resilience**

Cross Layer Error resilience in MIMO Systems
Norbert Wehn - University of Kaiserslautern, DE

1330 **Variability-Aware Memory Management in the Operating System**
Alex Nicolau - UCI, US

1400 **Cross-layer Design of Distributed Embedded Controllers**
Dip Goswami - TU Munich, DE

1430 **Coffee Break**

1500 **Session 5: System Dependability**

Exploiting Variability in Flash Memories Through Non-binary Error Correction Coding
Lara Dolecek - UCLA, US

1530 **Brainstorming and discussion for future collaboration**
Medhi Tahoori - Karlsruhe Institute of Technology, DE
Puneet Gupta - University of California, Los Angeles, US

1615 **Concluding Remarks**

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50th DAC	4
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Blue Pearl Software	10
CEA LETI	54
CimAlpes	54
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fringe technical meetings

A number of specialist interest groups will be holding their meetings at DATE. Currently, the following meetings are scheduled but a full list of fringe meetings with description of content will be found on the DATE web portal – **www.date-conference.com**

Day	Time	Meeting & Contact	Room	Type
Mon	1300-1700	**Challenges in Design and Qualification for Automotive Electronics** Michael Nicolaidis, Rubin Parekhji <parekhji@ti.com>	7 Laux 4	Open
Mon	1900-2100	**EDAA PhD Forum** Peter Marwedel <peter.marwedel@tu-dortmund.de>	Salle de Reception	Open
Tues	1300-1430	**ETTTC Meeting** Matteo Sonza Reorda <matteo.sonzareorda@polito.it>	Bayard	Open
Tues	1830-1930	**EDAA General Assembly** Georges Gielen <georges.gielen@esat.kuleuven.be>	7 Laux 4	Open
Tues	1830-2130	**European SystemC Users Group Meeting** Axel Braun <abraun@informatik.uni-tuebingen.de>	Meije	Open

PhD forum

Monday: Room – Salle de Reception – 1900-2100

Organiser:
Peter Marwedel, TU Dortmund, DE

The ACM SIGDA / EDAA PhD forum is part of the DATE Conference and hosted by ACM SIGDA and the European Design Automation Association (EDAA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Also, representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank ACM SIGDA, EDAA, and DATE for making this Forum possible.. More information is available on the web – **www.date-conference.com**

university booth demonstrations

DATE 13 will feature the University Booth within the exhibition area at booth 46 where system and VLSI CAD tools developed in Universities and Research Institutes are demonstrated as well as circuits in their working environment. This provides an alternative and more direct way of communicating CAD research results and displaying working silicon to the interested specialists. A rotating schedule will operate throughout the three days. Access to the exhibition area is free of charge.

Please find detailed information and the online programme at the DATE website www.date-conference.com/group/exhibition/u-booth

Contacts:
Laurent Fesquet and Andreas Voerg

university-booth@date-conference.com

This is a programme of free events open to all attendees at DATE 13 in the Exhibition Theatre

exhibition theatre

Chair:
Juergen Haase, edacentrum, DE

In addition to the conference programme during DATE 13, there will be a presentation theatre from Tuesday 19 March to Thursday 21 March 2013. Attendees will profit from having an industry forum in the midst of of Europe's leading electronic systems design event. The theatre is located in Room Lesdiguieres which is within the exhibition hall and affords easy access for exhibition visitors as well as for conference delegates.

Like in previous years, open Special Conference Sessions from Track 8 (full details are contained in the main conference programme pages) will take place in the Exhibition Theatre. These sessions are open to conference delegates as well as to exhibition visitors and are as follows:

2.8	**Hot Topic** IP Subsystems: The next productivity wave?	**Tuesday 1130-1300**
3.8	**Hot Topic** Design for Variability, Manufacturability, Reliability, and Debug: Many Faces of the Same Coin?	**Tuesday 1430-1600**
8.8	**Hot Topic** Countering Counterfeit Attacks on Micro-Electronics	**Wednesday 1700-1830**
10.8	**Panel** Will 3D-IC Remain a Technology of the Future… Even in the Future?	**Thursday 1100-1230**
11.8	**Embedded Tutorial** Advances in Asynchronous logic: from principles to GALS & NoC, recent industry applications, and commercial CAD tools	**Thursday 1400-1530**
12.8	**Embedded Tutorial** Closed-Loop Control for Power and Thermal Management in Multi-core Processors: Formal Methods and Industrial Practice	**Thursday 1600-1730**

Additionally there will be a panel on collaboration in Europe and testimonials providing valuable experience on recent results of leading companies in application of advanced design methodologies and new tools.

Please see presented overleaf information on the panel and on the confirmed testimonials. The full programme with all the details of the exhibition sessions is available on the DATE web portal and in the Event Guide.

4.8 Exhibition Theatre Testimonials

Tuesday, March 19, 1700 - 1830

Organiser/Moderator: **Juergen Haase,** edacentrum, DE

Speakers:
Hubert Degoirat, STMicroelectronics, FR
Jack Kruppa, Infineon Technologies AG, DE
Senad Durakovic, Intel Corporation, USA
Axel Jantsch, ELSIP, SE

In this session industrial testimonials will offer engineers an insight into good working practices and state-of-the-art design methods of market leaders. This sessions features design centering of IO in 28nm FDSOI technology, SoC power integrity verification with focus on analogue/mixed signal macros, data management for future SoCs and evolutionary computation for validation, testing and design automation.

1700 **Design Centering of IO in 28nm FDSOI Technology**
Hubert Degoirat - STMicroelectronics, FR

1720 **Using Apache RedHawk for SoC Power Integrity Verification with Focus on Analogue/Mixed Signal Macros**
Jack Kruppa - Infineon Technologies AG, DE

1740 **Evolutionary Computation for Validation, Testing and Design Automation**
Senad Durakovic, Aktan Burcin - Intel Corporation, USA

1800 **Data Managment in Future SoCs Made Easy**
Axel Jantsch - ELSIP, SE

6.8 Exhibition Theatre Session

Wednesday, March 20, 1100 - 1230

Silicon Europe – leading European regions join forces

Organiser: **Juergen Haase,** edacentrum, DE

Moderator: **Thomas Reppe,** Silicon Saxony, DE

Panellists:
Jean Chabbal, Minalogic, FR
Andreas Brüning, Silicon Saxony, DE
Ben van der Zon, High Tech NL, NL
Peter Simkens, DSP Valley, BE

Four of the leading European micro- and nanoelectronics regions are joining their research, development and production expertise to form the transnational, research-driven cluster "Silicon Europe – The Leaders for Energy Efficient ICT Electronics". The cluster partners from Germany, Belgium, France and the Netherlands are linked by a common goal: They aim to secure and expand Europe's position as the world's leading center for energy efficient micro- and nanoelectronics and information and communications technology (ICT). In order to reach this goal, Silicon Saxony (Dresden/Germany), DSP Valley (Belgium), Minalogic (Grenoble/France) and High Tech NL (Eindhoven/Netherlands) are cooperating in research, development and business expertise. Together they represent about 800 research institutes and companies, which account for more than 150,000 jobs; among the companies are global market leaders such as Philips, NXP Semiconductors, GlobalFoundries, Infineon, STMicroelectronics, Schneider Electric and Thales. This makes Silicon Europe one of the largest technology clusters of the world.

1100 **Silicon Europe - Cluster Alliance for European Micro- and Nanoelectronics Industry - Topics, Challenges, Opportunities**
Thomas Reppe - Coordinator, Cluster manager Silicon Saxony, DE

1120 **Minalogic: from research to industry**
Jean Chabbal - Cluster manager Minalogic, FR

1135 **Silicon Saxony - A High Tech Location of great Diversity**
Andreas Bruening - Board Member Silicon Saxony, DE

1150 **The Dutch Semicon Cluster: a complete value chain**
Ben van der Zon - High Tech NL, NL

1205 **DSP Valley - Region of Excellence in Embedded Signal Processing systems design**
Peter Simkens, Cluster manager DSP Valley, BE

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Test for Defects, Variability, and Reliability

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Test for Mixed-Signal, Analog, RF, MEMS

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On-Line Testing and Fault Tolerance

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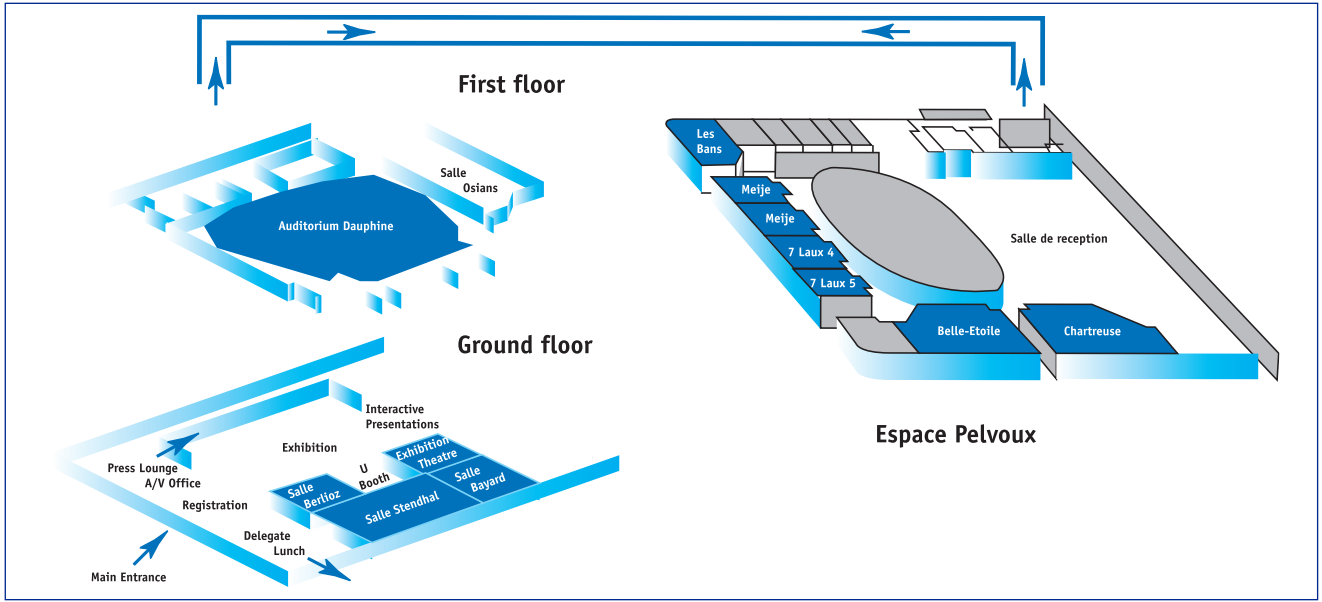

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