

advance programme

DATE 12

**Design, Automation
& Test in Europe**

**ICC, Dresden, Germany
March 12 - 16, 2012**

www.date-conference.com

Welcome	3
General Information	6

KEYNOTE SPEAKERS

4

Klaus Meder, Bosch, DE
Mojy Chian, GLOBALFOUNDRIES, DE
Max Lemke, European Commission

EXECUTIVE TRACK

7

Discussion Panels for Electronic Design Business Managers

E-MOBILITY DAY

8

MORE THAN MOORE DAY

9

SPECIAL SESSIONS

10

Hot Topics, Panels, Embedded Tutorials

DATE 12 - AT A GLANCE

12

A brief overview of the event

MONDAY TUTORIALS

17

Eight half-day tutorials, three full-day tutorials

TECHNICAL SESSIONS

26

Full listing of DATE technical programme, special sessions

AWARDS

26 55

DATE Awards Ceremonies

FRIDAY WORKSHOPS

93

Nine full-day workshops

EXHIBITION PROGRAMME

112

Exhibitor list, Special Conference Sessions and Business Presentations in the Exhibition Theatre

Detailed Index (inc. Committees and Site Plan)	115
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Dear Colleague,

We proudly present to you the Advance Programme of DATE 12. DATE combines the world's favourite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system level hardware and software implementation right down to integrated circuit design. While many conferences currently suffer from travel restrictions in many companies and face severe problems in attracting attendees, DATE 2012 received some 950 submissions. The boost in submissions by 37% and 18% in the Embedded Systems Software and the Applications Track reflects the key importance of software and applications for a wealthy economy and underlines the leading role of DATE in these fields. The importance of DATE as a worldwide indispensable meeting point is demonstrated by the fact that more than 50% of the submissions came from outside Europe. The most attractive topics this year were Simulation and Validation as well as Architectural and Microarchitectural Design.



For the 15th successive year DATE has prepared an exciting technical programme, with the help of more than 300 members of the Technical Programme Committee, who dedicated their time to thoroughly review the submissions, ranging from system level down to circuit design and covering all the most relevant application domains.

This year the conference will be held in Germany, at the ICC in Dresden and will span an entire working week starting on Monday March 12 with tutorials, and ending on Friday March 16 with workshops.

The **plenary keynote speakers** on Tuesday are Klaus Meder, President of the Automotive Electronics Division of Bosch to talk about 'The Mobile Society – Chances and Challenges for Micro- and Power Electronics', and Mojib Chian, Senior Vice President Design Enablement of GlobalFoundries, to talk about 'New Foundry Models – Accelerations in Transformations of the Semiconductor Industry'. On the same day, the **Executive Track** offers a series of business panels discussing hot topics in design. To emphasise that DATE is the major event for the designers, DATE 12 features invited sessions where **Europe's famous consumer industry presents its best designs and design practices.**

The main conference programme from Tuesday to Thursday includes 77 technical sessions organised in parallel tracks from four areas:

- D** – Design Methods, Tools, Algorithms and Languages
- A** – Application Design
- T** – Test Methods, Tools and Innovative Experiences
- E** – Embedded Software

Extra tracks are dedicated to the Executive Day on Tuesday and the two special days: **e-Mobility Day** on Wednesday and **More than Moore Day** on Thursday. There is a lunch-time Keynote on Wednesday Dr Max Lemke, Deputy Head of Unit Embedded Systems & Control, European Commission, Directorate General Information Society and Media who will talk on 'Research and Innovation on Advanced Computing – an EU Perspective'. Additionally, there are 74 Interactive Presentations which are organised into five IP sessions.

Finally, DATE offers a comprehensive overview of commercial design and verification tools in its exhibition including vendor seminars and abundant networking possibilities with fringe meetings.

We wish you a productive and exciting DATE 12 and a memorable social party on Wednesday evening.

DATE 12 General Chair

Wolfgang Rosenstiel
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DATE 12 Programme Chair

Lothar Thiele
ETH Zurich, Switzerland
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plenary session

Tuesday, March 13, 2012, 0830 – 1030

Opening Address – Awards – Keynote Speakers

first keynote address

The Mobile Society – Chances and Challenges for Micro- and Power Electronics

Klaus Meder, President of the Automotive Electronics Division, Robert Bosch GmbH, DE

In his speech "The mobile society - chances and challenges for Micro- and Power Electronics" Klaus Meder will demonstrate how the increasing society's request for a widespread mobility together with the need to save energy resources generates opportunities for a broad spectrum of new electronic systems - as well as some challenges for the KETs Design,

semiconductor technologies and assembly. Bosch is the leading automotive supplier worldwide with more than 280 manufacturing sites including a semiconductor fab in Reutlingen, Germany.



Research and Innovation on Advanced Computing – an EU Perspective

Dr Max Lemke, Deputy Head of Unit Embedded Systems & Control European Commission, Directorate General Information Society and Media

Under 'Components and Systems' in FP7-ICT, over the period 2007–2012, the EU has so far invested about 100M€ on Computing Systems research. Building on the industrial constituencies and activities of the Joint Technology Initiative ARTEMIS and complementing research on embedded systems and control, research and innovation on Computing Systems covers a broad spectrum of issues from multi-core scalability and mastering parallelism to hardware/software co-design and low energy/low cost chips. With the convergence of computing technologies, work covers the broad spectrum of computing systems from customised computing via data servers to high performance systems.



plenary session

Tuesday, March 13, 2012, 0830 – 1030

Opening Address – Awards – Keynote Speakers

second keynote address

New Foundry Models - Accelerations in Transformations of the Semiconductor Industry

Mojo Chian, Senior Vice President Design Enablement, GLOBALFOUNDRIES

Mojo Chian will give an outlook on the future development and role of foundries presenting "New Foundry Models - Accelerations in Transformations of the Semiconductor Industry", focusing on the new collaborative approach in technology development and high-end manufacturing. GLOBALFOUNDRIES is the first foundry with global footprint and leading edge manufacturing sites in Dresden, Germany, Singapore and the US.



wednesday lunchtime keynote

Work builds on and expands from European industrial strengths in embedded and mobile computing with low cost and energy efficiency being key drivers.

After a short overview of the research supported, some major trends in computing systems and their role in our society will be discussed. First ideas of new funding opportunities under Advanced Computing Systems in ICT Work Programme 2013 will be outlined. An outlook towards the next Framework Programme for Research and Innovation "Horizon 2020" and an overview of recommendations received from consultation activities with the constituencies in the broad context of Computing will conclude the presentation.

general information

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 12. Full General Information covering full technical programme details, conference registration costs and booking forms, hotel reservations and booking forms, travel to and in Dresden, and social event details is available on the conference website - www.date-conference.com

interactive programme on web

A fully interactive DATE 12 programme is available on the web – www.date-conference.com - where you will be able to view the entire detail of the programme and plan your attendance in advance.

venue

The Conference will take place from 12-16 March 2012 and the Exhibition from 13-15 March 2012 in the excellent facilities of the International Congress Center (ICC), Dresden, Germany - www.dresden-congresscenter.de

date party – wednesday

This year the DATE Party, sponsored by the City of Dresden, will take place in the Great Hall of the International Congress Center, Dresden. The evening will feature a buffet style dinner with plenty of buffet points and drinks to accompany dinner. There will be relaxed musical entertainment. In an enjoyable atmosphere participants will have the opportunity to meet and mingle with their friends and colleagues. All conference attendees, users, vendors and their guests are encouraged to come to the party. Additional tickets for the full Evening Social Programme may be obtained for 70 Euros each (see website for booking forms). Entrance will be by ticket only, so please check that you receive the party ticket when you register.

interactive presentations

Chair: Oliver Bringmann, FZI Karlsruhe, DE

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute, one-slide presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area.

Interactive Sessions will be held in the ICC, Dresden, on the lower ground floor close to the Exhibition area in 30-minute time slots during coffee and exhibition breaks. Coffee and water will be available during the sessions.

Organiser:

Yervant Zorian, Synopsys, US

DATE 2012 will again feature an Executive Track of presentations by leading company executives representing a range of semiconductor manufacturers, EDA vendors, fables houses and IP providers. This one-day program will be held on Tuesday 13 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks, except one post lunch session. All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view. The Executive Track sessions are below:

2.1 EXECUTIVE SESSION - What Roles will the Foundries and Fabless Houses Play in Advanced Technology Nodes?

– see page 27

3.1 EXECUTIVE SESSION – How to handle today's design complexity?

– see page 32

4.1 EXECUTIVE SESSION - Addressing Trends & Challenges of Automotive Chips

– see page 39

Organiser:

Oliver Bringmann, FZI Karlsruhe, DE

e-Mobility Special Day

DATE 2012 will take up the results of recent international e-mobility activities and will bring them to the next level by providing a unique platform for all stakeholders. For the first time the whole supply chain, ranging from EDA to car manufacturers Audi and Peugeot Citroën Automobiles and their suppliers like Robert Bosch GmbH and Infineon Technologies, will meet and work together on designing electronic systems for building hybrid and fully electrical cars that can drive longer distances and excel on robustness.

In several hot topic sessions the latest achievements and new requirements will be presented in the areas of optimised energy management and recovery, batteries and battery management systems, robustness challenges caused by combining high and low voltage electronics, and qualification of semiconductors in electric powertrains. Moreover, at DATE 2012 EDA market leaders Synopsys, Cadence and Mentor will team up with the tool providers of the automotive industry like AVL and will discuss in a dedicated panel session the role of EDA in the development of electric vehicles.

5.1

HOT TOPIC - Embedded Systems and Software Challenges in Electric Vehicles – see page 45

6.1

PANEL - Role of EDA in the Development of Electric Vehicles – see page 51

7.1

HOT TOPIC - Optimal energy management and recovery for FEV - see page 56

8.1

HOT TOPIC - Robustness Challenges in Automotive Electronics for Electric Vehicles – see page 64

Organiser:

Michel Brillouet, CEA-Leti, FR

More than Moore

This Special Day will start with three tutorials setting the More-than-Moore scene, in terms of present and future technologies (resp. Dr. Mart Graef from TU Delft and Dr. T. Skotnicki from STMicroelectronics) and from the application perspective.

Dedicated talks will then focus on specific MtM fields: analog mixed signal (Dr H Graeb from TU Munich), rf and power (Prof Lothar Frey from FhG-IISB) will be detailed as emblematic examples of MtM technologies.

The emerging field of heterogeneous integration will be addressed from the technology, design and test perspectives. Examples of 3D developments in Dresden (J Wolf from FhG/IZM) and Grenoble (M Scannell from CEA-Leti) will be given, followed by presentations on design techniques (Ass Prof Y Xie from Penn State University) and test challenges (E J Marinissen from IMEC).

Finally few applications have been selected illustrating the "More-than-Moore" domain. Silicon photonics is generating an increasing interest and will be detailed by L Fulbert from CEA-Leti both from the technology and design perspective. The wide field of MEMS/NEMS will be then covered before Prof G Fettweiss from TU Dresden addresses the critical field of high-speed ultra-low power design for healthcare applications.

9.1 More Moore - Setting the Scene
- see page 69

10.1 More Moore Technologies -
Analogue - RF - Power
- see page 75

11.1 More Moore - Heterogeneous
Integration - Tech/Design/Test
- see page 80

12.1 More Moore - Applications -
SI/MEMS/Biochip - see page 87

Special Sessions Chair:

Andreas Herkersdorf, TU Munich, DE

Raul Camposano, Nimbic, US

The following 17 Special Sessions have been organised, which should prove to be of great general interest.

Panel Sessions provide a forum in which motivated opinions on a controversial issue are discussed. The 'trend setters' are given a time-slot to present their views, which are then subjected to critical appraisal from the audience. **Hot Topic** sessions give technical information about emerging new topics and provide a good overview and technical insight. Presenters are leading experts in the field. They present their view on the relevant issues and their importance for research and development. **Embedded Tutorials** give an insight of relevant topics usually starting from an introductory base.

- 2.7 **HOT TOPIC: EDA Solutions to New-Defect Detection in Advanced Process Technologies**
Organiser: E J Marinissen, IMEC, BE
- 2.8 **EMBEDDED TUTORIAL: Beyond CMOS - Benchmarking for Future Technologies**
Organiser: R Popp, edacentrum, DE
- 3.5 **PANEL: Key Challenges for the next generation of computing systems taming the data deluge**
Organiser: R Riemenschneider, European Commission, BE
- 3.8 **HOT TOPIC: Design Automation Tools for Engineering Biological Systems**
Organiser: J Madsen, DTU, DK
- 4.5 **EMBEDDED TUTORIAL: State-of-the-art Tools and Techniques for Quantitative Modeling and Analysis of Embedded Systems**
Organiser: A Legay, INRIA/Rennes, FR
- 5.2 **PANEL: Accelerators and emulators: Can they become the platform of choice for hardware verification?**
Organiser: R Morad, IBM Research - Haifa, IL
- 6.2 **EMBEDDED TUTORIAL: Memristor Technology in Future Electronic System Design**
Organisers: R Tetzlaff, TU Dresden, DE and A Bruening, ZMDI AG, Dresden, DE
- 6.7 **HOT TOPIC: Design for Test and Reliability in Ultimate CMOS**
Organisers: L Anghel, TIMA, FR and M Nicolaidis, TIMA, FR
- 7.2 **HOT TOPIC: Virtual Platforms: Breaking New Grounds**
Organiser: R Leupers, RWTH Aachen U, DE
- 7.8 **HOT TOPIC: New Directions in Timing Modeling and Analysis of Automotive Software**
Organiser: W Mueller, U Paderborn, DE
- 8.2 **PANEL: What Is EDA Doing for Trailing Edge Technologies?**
Organiser: M Casale-Rossi, Synopsys, US
- 8.8 **EMBEDDED TUTORIAL: Batteries and Battery Management Systems**
Organisers: L Fanucci, U Pisa, IT and H Gall, austriamicrosystems, AT
- 9.2 **HOT TOPIC: Multi-Core Design: From Ultra-Low-Power Design to Exascale Computing**
Organiser: R Hermida, UCM Madrid, ES and T Simunic Rosing, UCSD, US
- 10.2 **HOT TOPIC: Pathways to Servers of the Future**
Organiser: G Fettweis, TU Dresden, DE
- 10.8 **EMBEDDED TUTORIAL: Moore meets Maxwell**
Organiser: R Camposano, Nimbic Inc., US
- 11.8 **HOT TOPIC: Programmability and Performance Portability Aspects of Heterogeneous Multi-/Manycore Systems**
Moderator: C Kessler, Linkoping U, SE
- 12.8 **EMBEDDED TUTORIAL: Advances in variation-aware modeling, verification, and testing of analog ICs**
Organiser: T McConaghy, Solido Design Automation, CA

MONDAY

Educational Tutorials
Welcome Reception

TUESDAY

Technical Conference and Exhibition Day 1
Vendor Exhibition
Exhibition Theatre (also featuring Track 8 special conference sessions)
Opening Plenary, Keynote Addresses and Distinguished Awards
Executive Sessions
Evening Reception sponsored by the IEEE Council on EDA

WEDNESDAY

Technical Conference and Exhibition Day 2
Vendor Exhibition
Exhibition Theatre (also featuring Track 8 special conference sessions)
e-Mobility Special Day
Keynote address
DATE Awards Ceremony
DATE Party sponsored by the City of Dresden

THURSDAY

Technical Conference and Exhibition Day 3
Vendor Exhibition
Exhibition Keynote and Exhibitors' Highlights
Exhibition Theatre (also featuring Track 8 special conference sessions)
More than Moore Special Day

FRIDAY

Special Interest Workshops

CONTACTS

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0730	TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS		
BREAKS	1100-1130 Morning, 1300-1430 Lunch, 1600-1630 Afternoon.		
0930 to 1800	A (Room - Saal 5) From MoC to SoC – Programming Embedded Multiprocessor-Systems	B (Room – Konferenz 2) Manufacturing, Design, and Test of 2.5D- and 3D-Stacked ICs	C (Room – Konferenz 3) Mixed Signal IC Design and Test: Challenges, Solutions, and Industry Practice
0930 to 1300	D1 (Room – Konferenz 1) Multi-Core Platforms for Mixed-Critical Embedded Systems	E1 (Room – Konferenz 4) HW - SW design and verification for safety critical electronic systems: theory, normative and industry practices	F1 (Room – Konferenz 5) On Variability and Reliability: Dynamic Margining and Low Power
1430 to 1800	D2 (Room – Konferenz 1) New Challenges and Technologies Behind Cloud Computing	E2 (Room – Konferenz 4) The Device-to-System Spectrum – A Tutorial on IC Design with Nanomaterials	F2 (Room – Konferenz 5) Design methodology and techniques in production low-power SOC designs
1800	Welcome Reception		
		G1 (Room – Konferenz 6) Demystifying Board-Level Test and Diagnosis	G2 (Room – Konferenz 6) Testing Embedded Memories in the Nano-Era: Fault Models, Tests, Industrial Results and BIST

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1030-1130 Exhibition Break, 1300-1430 Lunch, 1600-1700 Exhibition Break (1600-1630 IP1)					
0830	1.1 PLENARY: OPENING, KEYNOTE ADDRESSES AND AWARDS PRESENTATION, Grosser Saal							
	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
1130 to 1300	2.1 EXECUTIVE SESSION – What Roles will the Foundries and Fabless Houses Play in Advanced Technology Nodes?	2.2 Validation of Modern Microprocessors	2.3 Memory System Optimisation	2.4 Architectures and Efficient Designs for Automotive and Energy-Management Systems	2.5 Physical Design for Low-Power	2.6 Optimised Utilisation of Embedded Platforms	2.7 SPECIAL SESSION - HOT TOPIC: EDA Solutions to New-Defect Detection in Advanced Process Technologies	2.8 SPECIAL SESSION - EMBEDDED TUTORIAL: Beyond CMOS - Benchmarking for Future Technologies
1400	LUNCH							
	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
1430 to 1600	3.1 EXECUTIVE SESSION – How to handle today's design complexity?	3.2 Effective Functional Simulation and Validation	3.3 Industrial Design Methodologies	3.4 Large-Scale Energy and Thermal Management	3.5 PANEL - Key Challenges for Next-Generation Computing	3.6 Model-Based Design and Verification for Embedded Systems	3.7 Improving Reliability and Yield in Advanced Technologies	3.8 SPECIAL SESSION - HOT TOPIC: Design Automation Tools for Engineering Biological Systems
1700 to 1830	Room – Saal 5	Room – Konferenz 6	Room – Konferenz 1	Room – Konferenz 2	Room – Konferenz 3	Room – Konferenz 4	Room – Konferenz 5	Exhibition Theatre
	4.1 EXECUTIVE SESSION - Addressing Trends & Challenges of Automotive Chips	4.2 Routing solutions for upcoming NoC challenges	4.3 Industrial Embedded System Design	4.4 System-Level Power and Reliability Estimation and Optimisation	4.5 SPECIAL SESSION - EMBEDDED TUTORIAL: State-of-the-art Tools	4.6 Compilers and Source-Level Simulation	4.7 Advances in Test Generation	EXHIBITION PANEL - Modeling and Simulation Challenges in Automotive Electric System Design
1830	Evening Reception sponsored by the IEEE Council on EDA							

	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP2), 1230-1340 Lunch, 1600-1700 Exhibition Break (1600-1630 IP3)										
	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS					
0730													
0830 to 1000	5.1 SPECIAL DAY E-MOBILITY - HOT TOPIC: Embedded Systems and Software Challenges in Electric Vehicles	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre					
	5.2 SPECIAL SESSION - PANEL: Accelerators and emulators: Can they become the platform of choice for hardware verification?	Room - Konferenz 1	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	5.7 Testing of Non-Volatile Memories					EXHIBITION OPENS AT 1000
1100 to 1230	6.1 SPECIAL DAY E-MOBILITY - PANEL - Role of EDA in the Development of Electric Vehicles	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre					
	6.2 SPECIAL SESSION - EMBEDDED TUTORIAL: Memristor Technology in Future Electronic System Design	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	6.6 Timing Analysis					EXHIBITION PANEL - Foundry Design Practices
1340													
1430 to 1600	7.1 SPECIAL DAY E-MOBILITY - HOT TOPIC: Optimal energy management and recovery for FEV	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre					
	7.2 SPECIAL SESSION - HOT TOPIC: Virtual Platforms: Breaking New Grounds	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	7.7 Test and Repair of New Technologies					7.8 SPECIAL SESSION - HOT TOPIC: New Directions in Timing Modelling and Analysis of Automotive Software
1700 to 1830	8.1 SPECIAL DAY E-MOBILITY - HOT TOPIC: Robustness Challenges in Automotive Electronics for Electric Vehicles	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre					
	8.2 SPECIAL SESSION - PANEL: What Is EDA Doing for Trailing Edge Technologies?	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	8.7 On-Line Test for Secure Systems					8.8 SPECIAL SESSION - EMBEDDED TUTORIAL: Batteries and Battery Management Systems

AWARDS 1340-1400, KEYNOTE EUROPEAN COMMISSION 1400-1430 (SAAL 5) EXHIBITION PANEL 1315-1415, EXHIBITION THEATRE, 'NOT ME! WHO REALLY OWNS THE IP QUALITY ISSUE?'

	REGISTRATION & SPEAKERS' BREAKFAST		BREAKS		1000-1100 Exhibition Break, (1000-1030 IP4), 1230-1400 Lunch, 1530-1600 Break (1530-1600 IP5)			
	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
0730	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre
0830 to 1000	9.1 SPECIAL DAY MORE-THAN-MOORE: More Moore - Setting the Scene	9.2 SPECIAL SESSION - HOT TOPIC: Multi-Core Design: From Ultra-Low-Power Design to Exascale Computing	9.3 Architecture and Building Blocks for Secure Systems	9.4 Advances in High-Level Synthesis	9.5 Supply Voltage and Circuitry Based Power Reductions	9.6 Creation and Processing of System-Level Models	9.7 Test and Monitoring of RF and Mixed-Signal ICs	EXHIBITION OPENS AT 1000
1100 to 1230	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre
1100 to 1230	10.1 SPECIAL DAY MORE-THAN-MOORE: More Moore Technologies - Analogue - RF - Power	10.2 SPECIAL SESSION - HOT TOPIC: Pathways to Servers of the Future	10.3 Side-Channel Analysis and Protection of Secure Embedded Systems	10.4 Topics in High-Level Synthesis	10.5 Modelling of Complex Analogue and Digital Systems	10.6 Cyber-Physical Systems	10.7 On-Line Test and Fault Tolerance	10.8 SPECIAL SESSION - EMBEDDED TUTORIAL: Moore meets Maxwell
1230	EXHIBITION KEYNOTE AND EXHIBITORS' HIGHLIGHTS 1315-1400, EXHIBITION THEATRE 'KEY SUCCESS FACTORS 2012 FOR DESIGN'							
1400 to 1530	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre
1400 to 1530	11.1 SPECIAL DAY MORE-THAN-MOORE: Heterogeneous Integration - Tech/Design/Test	11.2 The Quest for NoC Performance	11.3 Emerging Memory Technologies (1)	11.4 Physical Anchors for Secure Systems	11.5 Analogue Design Validation	11.6 Techniques and Technologies Power Aware Reconfiguration	11.7 Rise and Fall of Layout	11.8 SPECIAL SESSION - HOT TOPIC: Prog ability & Perf. Portability Aspects of H geneous Multi/Manycore Sys
1600 to 1730	Room - Saal 5	Room - Konferenz 6	Room - Konferenz 1	Room - Konferenz 2	Room - Konferenz 3	Room - Konferenz 4	Room - Konferenz 5	Exhibition Theatre
1600 to 1730	12.1 SPECIAL DAY MORE-THAN-MOORE: Applications - SI/MEMS/Biochip	12.2 The Frontier of NoC Design	12.3 Emerging Memory Technologies (2)	12.4 Digital Communication Systems	12.5 Architecture and Networks for Adaptive Computing	12.6 Boolean Methods in Logic Synthesis	12.7 Impact of Modern Technology on Layout	12.8 SPECIAL SESSION - EMBEDDED TUTORIAL: Advcs in Variation/Aware Modelling V'fication & Testing of A'log ICs

WORKSHOP REGISTRATION & WELCOME REFRESHMENTS

Please see individual workshop programmes for lunch and break times

0730

BREAKS

0830

TO

1700

Room – Seminar 1

W1 Improving energy efficiency in buildings: from hardware to software aspects

Room – Konferenz 1

W2 Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow

Room – Konferenz 2

W3 Fourth Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools and Applications

Room – Konferenz 3

W4 Variability modelling and mitigation techniques in current and future technologies (VAMM)

Room – Saal 5

W5 3D Integration – Applications, Technology, Architecture, Design, Automation, and Test

Room – Konferenz 4

W6 European SystemC User's Group Workshop: OSCl and Accellera Core Technologies for the Next Generation of System-Level Design

Room – Konferenz 5

W7 Facing dependability challenges at nanoscale: from devices to systems

Room – Konferenz 6

W8 Computer Aided Network Design (CANDE) Workshop 2012

Room – Seminar 3

W9 Cyber Physical Systems (CPS) for Smart Mobility: Design, Architectures and Applications

0830

TO

1700

friday 16 march

FRIDAY

Organiser: Luca Fanuci, Pisa U, IT

Eleven pre-conference tutorials will be given on Monday. Three are full-day tutorials (A, B and C). Eight are half-day tutorials, four to be given in the morning (D1, E1, F1 and G1) and four in the afternoon (D2, E2, F2 and G2). A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.

The titles, organisers, speakers, and abstracts of the tutorials are given below:

0930

FULL-DAY TUTORIALS – A, B, C**A (Room - Saal 5)****From MoC to SoC – Programming Embedded Multiprocessor Systems**

Organisers: Rainer Leupers, RWTH Aachen U, DE
Gerhard Fettweis, TU Dresden, DE

Speakers: Alan Gatherer, Huawei Technologies, US
Gerhard Fettweis, TU Dresden, DE
Marco Bekooij, NXP, NL
Jos van Eijndhoven, Vector Fabrics, NL
Rainer Leupers, RWTH Aachen U, DE
Matthias Weiss, Intel, DE

The trend towards multicore, and even manycore, hardware platforms is a great revolution in the embedded computing industry. In particular, efficient mapping of applications to MPSoCs is a highly challenging task. This tutorial focuses on the application domain of wireless communication, including radio standards like UMTS, LTE, and beyond. MPSoCs for wireless have evolved to complex systems, providing homogeneous and heterogeneous processing elements next to multi-level memory hierarchies. This mix of hardware facilities is needed to obtain the required processing speed and power efficiency, but makes the system hard to implement from the application programmer perspective. With a blend of experienced academic and industrial speakers, the tutorial discusses the major challenges and state-of-the-art solution approaches in embedded MPSoC programming. It covers DSP oriented programming models and languages, spatial/temporal task mapping and scheduling techniques, as well as optimized parallel code generation. Further key aspects are SDR based modem implementation, handling of real-time constraints, advanced code instrumentation for code analysis, vector processing, and utilization of MPSoC communication architectures. The presentations will be rounded up by concrete tool descriptions and/or demos, showing how many of the presented concepts can assist embedded MPSoC programmers already today, and what is needed for the future.

B (Room - Konferenz 2)**Manufacturing, Design, and Test of 2.5D- and 3D-Stacked ICs****Organiser:** Erik Jan Marinissen, IMEC, BE**Speakers:** Armin Klumpp, Fraunhofer EMFT, DE
Paul Franzon, North Carolina State U, US
Erik Jan Marinissen, IMEC, BE

At the intersection of advanced semiconductor processing and advanced packaging, the semiconductor industry is preparing itself for vertical interconnection of multiple stacked dies by means of through-silicon vias (TSVs). TSVs are conducting nails which extend out of the back-side of a thinned-down die and enable the vertical interconnection to another die. TSVs are high-density, low-capacity interconnects compared to traditional wire-bonds, and hence allow for many more interconnections between stacked dies, while operating at higher speeds and consuming less power. TSVs promise to revolutionize the semiconductor industry by enabling the creation of new generations of 'super chips', in both "2.5D" (active dies placed on and interconnected by a passive silicon interposer containing TSVs) and "3D" (towers of vertically stacked dies, interconnected by TSVs). Recently, several leading semiconductor companies, foundries, assembly houses, and their suppliers, have done product announcements, as public testimonials that 2.5D- and 3D-Stacked ICs are real. Consequently, process, design, and test engineers throughout the entire semiconductor industry are preparing for this product reality.

This comprehensive tutorial consists of three parts: (1) manufacturing, (2) design, and (3) test. In Part 1, on manufacturing, the tutorial presents the process steps related to TSV manufacturing, as well as the subsequent steps of wafer thinning, back-side processing, bonding, and packaging. In Part 2, on design, the tutorial focuses on the differences in architectures and design implementation between the conventional (2D) and the new 2.5D- and 3D-chips, and the status of the design automation in this field. We illustrate the challenges and benefits of stacked design by means of several case studies. In Part 3, on test, the tutorial presents various 3D test flows and the cost modelling thereof and new defects and test generation for stacked ICs. We also cover the challenges and emerging solutions with respect to test access, in terms of wafer probing and on-die design-for-test hardware.

C (Room - Konferenz 3)**Mixed Signal IC Design and Test: Challenges, Solutions and Industry Practice****Organiser:** Gordon Roberts, McGill U, CA**Speaker:** Gordon Roberts, McGill U, CA

This tutorial will describe the challenges and practices of analog/mixed-signal (MS) design and test at a level that is suited to the non-expert. In much the same way that a computer program is written to implement a specific signal-processing algorithm, e.g., remove noise from a camera image, the goal of any analog/mixed-signal circuit design is to do a similar operation using a specialized transistor implementation. In order to appreciate the details of analog/MS design, this tutorial will begin with a review of the MOS transistor and how its voltage biasing and aspect ratio control its performance attributes. These insights will serve as the guide to the design of several basic circuits such as current sources and amplifiers.

During the manufacturing, such circuits experience large variations in behavior. To solve these problems, unit-ratio component design together with feedback methods are used.

While negative feedback has largely been responsible for the success of analog/MS circuits, it is also the reason that these circuits are so difficult to test. As analog/MS circuits today achieve incredibly high levels of performance, it does so by operating at the limits of what component matching and negative feedback can provide. This, in turn, makes testing these circuits extremely time consuming, i.e., costly, as the test information lies with very small signals buried in noise. This tutorial will describe both production test techniques and several DFT approaches used in practice today; as well we shall look ahead into possible DFT approaches being discussed today in various research circles.

0930

HALF-DAY TUTORIALS – D1, E1, F1, G1

D1 (Room - Konferenz 1)

Multi-Core Platforms for Mixed-Critical Embedded Systems

Organiser: Prof. Dr.-Ing. Rolf Ernst, TU Braunschweig, DE

Speakers: Prof. Dr.-Ing. Rolf Ernst, TU Braunschweig, DE
Glenn Farrall, Infineon, UK
Jonas Diemer, TU Braunschweig, DE
Henrik Theiling, Sysgo, DE
Matthieu Lemerre, CEA, FR
Swapnil Gandhi, Delphi, DE
Madeleine Faugère, Thales, FR

Mixed-critical systems integrate safety-critical and non-critical applications on the same platform leading to conflicts in verification, certification and maintenance. Most of the more complex embedded systems e.g. in automotive, avionics, or industrial automation are evolving as mixed critical systems to meet non-functional requirements (cost, space, weight, reliability, ...). Multi-core platforms offer improved isolation opportunities over single-core processors, but many challenges must be addressed, such as in core-to-core communication, isolation of shared resources and error protection.

The tutorial presenters are from hardware and real-time operating systems providers, covering different industrial segments and approaches. They will give an overview on the challenges and on the state of the art in industrial and academic solutions and give an outlook on the possible use in larger many-core systems and other open challenges. Specifically, the presenters will discuss hardware mechanisms for virtualization, isolation, and core-to-core communication, and present implementation examples. On the software side, the tutorial will detail how these mechanisms are used to provide a safe environment for applications following domain specific standards like ARINC and AUTOSAR. PikeOS and PHAROS will be covered as examples. Finally, the tutorial will discuss key applications of the presented platforms, focusing on domain specific requirements in both design and certification for automotive, avionics and industrial automation domains. The presenters collaborate in the RECOMP project (Reduced Certification Costs Using Trusted Multi-core Platforms, <http://www.recomp-project.eu>), a large European ARTEMIS project that focuses on multi-core platforms for mixed-critical systems.

E1 (Room - Konferenz 4)

HW - SW Design and Verification for Safety Critical Electronic Systems: Theory, Normative and Industry Practices

Organiser: Riccardo Mariani, YOGITECH SpA, IT

Speakers: Riccardo Mariani, YOGITECH SpA, IT
 Carsten Gebauer, Robert Bosch GmbH, DE
 Karl Greb, Texas Instruments, US
 Pete Harrod, ARM Ltd, UK
 Martin Schwarz, TTTech Computertechnik AG, AU
 Andreas Buchwieser, Wind River GmbH, DE
 Ioannis Sourdis, Chalmers U of Tech., SE

Nowadays, many HW and SW components are used in safety-critical domains such as automotive, industrial, medical, railway and aerospace. It is expected that within 2020 a great majority of electronic systems will have to cope - directly or indirectly - with safety requirements. From HW point of view, the new technologies are bringing new fault models and failure modes; from SW point of view, the coexistence in the same HW device of several applications and tasks with different safety requirements brings complex problems in terms of data and timing interferences. To handle this complexity, functional safety standards like IEC 61508 and ISO 26262 as other standards like DO-254 are giving requirements, evaluation metrics and methodologies to define "how much safe" shall be a given component or system.

The organizer will introduce the tutorial giving an overview of the theory behind functional safety and a practical overview of the functional safety standards like IEC 61508, ISO 26262 and DO-254/DO-178B. The presenters from industries will give the audience a complete view on how HW and SW safety critical electronic systems are conceived and designed: from a system perspective, from a silicon vendor perspective, from a SW perspective, from an on-chip and off-chip safety network perspective and from a processor perspective. From research point of view, the tutorial will include a presentation about most advanced researches ongoing in the safety-critical domain, on behalf of the DeSyRe FP7-ICT project consortium.

F1 (Room - Konferenz 5)

On Variability and Reliability; Dynamic Margining and Low Power

Organisers: Fadi J. Kurdahi, UC Irvine, US
 Ahmed M. Eltawil, UC Irvine, US
 Amin Khajeh, Qualcomm Inc, US

Speakers: Fadi J. Kurdahi, UC Irvine, US
 Ahmed M. Eltawil, UC Irvine, US
 Amin Khajeh, Qualcomm Inc, US

The design for manufacturing and yield (DFM&Y) is fast becoming an indispensable consideration in today's SoCs. Most current flows only consider manufacturability and yield at the lowest levels: process, layout and circuit. As such, these metrics are treated as an afterthought. With advanced process nodes, it has become increasingly expensive - and soon prohibitive - to guarantee bit level error free chips. The challenge now is to design reliable systems using chips that may have some faults. This has led to approaches that consider DFM&Y at the system level where more benefit can be reaped, and to consider the problem across the design layers. This tutorial covers cross layer approach to design for

DFM&Y spanning from the application all the way to manufacturing, overviews various techniques being explored today, and demonstrates its effectiveness on key applications including wireless communication systems (using WCDMA as the transmission physical layer), and multimedia applications (H.264). In addition, we explore the viability of cross-layer DFM&Y at the architectural level, focusing on processor caches. Experimental results that confirm the viability of such an approach will be presented and discussed. The results confirm that there is a significant opportunity for cross-layer error exploitation, resulting in an expanded design space with interesting design points that would otherwise have not been discovered or considered by SoC designers. The tutorial then proceeds to describe a scalable, unified statistical model that accurately reflects the impact of random hardware failures (embedded memory as an example) due to power management policies on the overall performance of a communication system. This enables system designers to efficiently and accurately determine the effectiveness of novel power management techniques and algorithms that are designed to manage both hardware failure and communication channel noise, without the added cost of lengthy system simulations that are inherently limited and suffer from lack of scalability.

G1 (Room - Konferenz 6)

Demystifying Board-Level Test and Diagnosis

Organiser: Krishnendu Chakrabarty, Duke U, US

Speakers: William Eklow, Cisco Systems Inc, US
Krishnendu Chakrabarty, Duke U, US

The gap between working silicon and a working board/system is becoming more significant and problematic as technology scales and complexity grows. The result of this increasing gap is failures at the board and system level that cannot be duplicated at the component level. These failures are most often referred to as "NTFs" (No Trouble Finds). The result of these NTFs can range from higher manufacturing costs and inventories to failure to get the product out of the door. The problem will only get worse as technology scales and will be compounded as new packaging techniques (SiP, SoC, 3D) extend and expand Moore's law. This is a problem that must be solved, yet, little effort has been applied up to this point. This tutorial will provide a detailed background on the nature of this problem and will provide DFT and test solutions at both the component and board/system level.

This tutorial is part of the annual IEEE Computer Society TTC Test Technology Educational Program (TTEP) 2012

D2 (Room - Konferenz 1)**New Challenges and Technologies Behind Cloud Computing**

Organisers: Marcello Coppola, STMicroelectronics, FR
Miltos Grammatikakis, TEI of Crete, GR

Speakers: Yiannis Kompatsiaris, ITI-CERTH, GR
Jan Kiszka, Siemens, DE
Marcello Coppola, ST Microelectronics, FR
Bernard Candaele, Thales, FR
Huy-Nam Nguyen, BULL, FR

The continuous decline of energy sources together with the rapid growth of commercial applications, such as online transaction processing, scientific computing, social media mining, multimedia-oriented web-services, and search engines, provided to end-users from a wide range of devices challenge existing large-scale computing, communication and data storage infrastructures. In fact, the extremely high energy costs of data centers due to vast server grids, power supply and cooling infrastructures, as well as the level of carbon emission in IT and communication technologies continue to raise public awareness, forcing policy makers to prepare legislation incentives towards green computing.

Existing high end multicore server architectures, such as IBM's Power7, Oracle Sun PowerNap and AMD's "Magny Cours" Opteron processor incarnation, already benefit from powerful out-of-order cores combined with large on-chip cache hierarchies and/or rapid, non-intrusive, automated power (or thermal) model transitions between a high-performance active state and a near-zero-power idle state.

Within this context, this tutorial examines challenges within the vast and ever-changing world of cloud technology, focusing on architectural trends, state-of-the-art design methodology and tools, full virtualization solutions, real-life applications and evolution towards large-scale, "green" multi-server cloud infrastructures. Key technology must be carefully weighed against potential costs, flexibility, scalability, performance, carbon footprint, power-efficiency, security, fault tolerance and overall quality of experience in accessing server content.

This tutorial brings together well-established actors from leading-edge companies, universities and research centers, firmly rooted in business realities and in tune with future research trends and evolution. The combined strongly-connected presentations will foster well-focused information exchange to the audience, providing ample space for questions.

E2 (Room - Konferenz 4)**The Device-to-System Spectrum – A Tutorial on IC Design with Nanomaterials**

Organisers: Deming Chen, U of Illinois at Urbana-Champaign, US
Subhasish Mitra, Stanford U, US

Speakers: Deming Chen, U of Illinois at Urbana-Champaign, US
Subhasish Mitra, Stanford U, US;
Eric Pop, U of Illinois at Urbana-Champaign, US
Naresh Shanbhag, U of Illinois at Urbana-Champaign, US

Nanomaterials such as carbon nanotubes (CNT), graphene nanoribbons (GNR), nanowires (NW), and other emerging electronic elements, have the potential to revolutionize nanoelectronics by enabling favorable device properties, novel functionality, or ultra-low power operation. Nanomaterials have a significant potential for building superior devices, routing structures, and interconnects. These nanomaterials may be essential to sustaining the advancement of electronic systems or bringing in new functionality. Yet they are also facing unique challenges, such as higher defect rate and nanomaterial-specific process-related variations. Such unique challenges are more apparent for scaled CMOS technologies as well. Given the great promise of nanotechnology for the development of future electronics and the general interest of research on this fast-growing area, we gathered a group of experts to give a tutorial to share the vision, present the promises and challenges, inspire the audience, and enable further development of nanotechnology.

In this tutorial, we will first present the current state-of-the-art fabrication, modeling and operation of several new nanoscale device and circuit components. These will include design and fabrication of GNR transistors, CNT transistors, CNT logic, low-power phase-change memory, etc. While these innovations are fundamental for the establishment of nanotechnology, the true impact for electronic systems demands that we translate these device and component-level capabilities into system-level benefits. Therefore, the second focus of this tutorial strives to bridge the gap between nanoelectronic device research and nanosystems design. These include nanosystems prototype design and modeling, statistical design approaches, and error-resilient designs targeting high performance, high reliability, and low power. The ultimate goal is to expose the potential of nanoelectronic technology and the unique challenges it presents across the whole device-to-system spectrum. Tutorial presentations will encompass four segments, with the first two segments focusing on nanodevices and nanocomponents, and the last two segments on nanosystems and system-level optimizations on performance, power and reliability.

F2 (Room - Konferenz 5)

Design Methodology and Techniques in Production Low-Power SOC Designs

Organiser: Kaijian Shi, Cadence Design Systems, US

Speakers: Kaijian Shi, Cadence Design Systems, US
Thomas Buechner, IBM, DE

Power has become a critical metric and key differentiator in sub-65nm SOC designs, due to growing power density driven by technology scaling and chip integration. This tutorial provides an overview of the low-power design methodologies and techniques in production SOC design perspective, emphasizing on the real design considerations and impact on chip success. We shall discuss pros and cons of the methods and techniques considering impacts on chip design schedule, yield, and overall power-performance target. We shall also discuss about design guidance and recommendations in various design steps and decision making points, based on our years of successful experience in production low-power SOC designs.

This tutorial is organized in two parts. In the first part, we shall overview power related challenges in sub-60nm SOC design and state-of-the-art techniques to reduce chip power. We shall give a holistic view from chip level to system and application levels. Practical industrial examples will be used to show how power savings can be

achieved in modern SoC, processors and computer systems. In the second part, we shall describe production low-power design methodology and techniques particularly the power-gating and the voltage & frequency scaling which are the two advanced power reduction methods used effectively in sub-65nm production low-power designs. We shall explain when, where and how these methods and techniques are applied to a chip according to the design goals and time-to-market requirement. We shall also overview production low-power design methodology and flow with power intent descriptions.

G2 (Room - Konferenz 6)

Testing Embedded Memories in the Nano-Era: Fault Models, Tests, Industrial Results and BIST

Organisers: Said Hamdioui, TU Delft, NL
Ad J Van de Goor, TU Delft and ComTex, NL

Speakers: Said Hamdioui, TU Delft, NL
Ad J Van de Goor, TU Delft and ComTex, NL

The cost of memory testing increases with every generation of new memory chips. New technologies are introducing new defect mechanisms that were unknown in the past. Precise fault modeling to design efficient tests is therefore essential in order to keep the test cost and test time within economically acceptable limits, while keeping a high product quality.

The objective is to provide attendees with an overview of fault modeling, test design, BIST and BISR for memory devices in the nano-era. Traditional fault modeling and recent development in fault models for current and future technologies are covered. Systematic methods are presented for designing and optimizing tests, supported by industrial results from different companies (e.g. Intel, ST, Infineon) and for different technology nodes (e.g., 0.13um, 65nm). Impact of algorithmic (e.g., data-background) and non-algorithmic (e.g. voltage) stresses is explored in order to get better insight in the test effectiveness. State-of-the art and novel BIST architectures are covered; special attention is given to the optimization of address generator designs as they typically consume considerable BIST area overhead. BISR and redundancy analysis are also discussed. Finally, future challenges in memory testing are highlighted.

This tutorial is part of the annual IEEE Computer Society TTC Test Technology Educational Program (TTEP) 2012

Tutorials

MONDAY 12 MARCH, 2012

0730 **TUTORIAL REGISTRATION**0800 **Tutorial Welcome Refreshments**

0930-1800

- A (Room – Saal 5) **From MoC to SoC – Programming Embedded Multiprocessor Systems**
- B (Room – Konferenz 2) **Manufacturing, Design, and Test of 2.5D- and 3D-Stacked ICs**
- C (Room – Konferenz 3) **Mixed Signal IC Design and Test: Challenges, Solutions, and Industry Practice**

0930

- D1 (Room – Konferenz 1) **Multi-Core Platforms for Mixed-Critical Embedded Systems**
- E1 (Room – Konferenz 4) **HW - SW Design and Verification for Safety Critical Electronic Systems: Theory, Normative and Industry Practices**
- F1 (Room – Konferenz 5) **On Variability and Reliability; Dynamic Margining and Low Power**
- G1 (Room – Konferenz 6) **Demystifying Board-Level Test and Diagnosis**
- 1430
- D2 (Room – Konferenz 1) **New Challenges and Technologies Behind Cloud Computing**
- E2 (Room – Konferenz 4) **The Device-to-System Spectrum – A Tutorial on IC Design with Nanomaterials**
- F2 (Room – Konferenz 5) **Design Methodology and Techniques in Production Low-Power SOC Designs**
- G2 (Room – Konferenz 6) **Testing Embedded Memories in the Nano-Era: Fault Models, Tests, Industrial Results and BIST**

Tutorial attendees should choose in advance one tutorial from D1, E1, F1 or G1, which take place in the morning, and/or one tutorial from D2, E2, F2 or G2, which take place in the afternoon. Those wishing to attend one of the full-day tutorials should choose in advance one of A, B or C. A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.

All tutorials run in parallel in accordance with the timetable below.

Rooms will be signposted.

- 0730 - 0930 **Registration and Tutorial Welcome Refreshments**
(Main Foyer)
- 0930 – 1100 **Tutorials**
- 1100 – 1130 **Break**
- 1130 – 1300 **Tutorials**
- 1300 – 1430 **Lunch Break**
- 1330 **CONFERENCE REGISTRATION BEGINS**
- 1430 – 1600 **Tutorials**
- 1600 – 1630 **Break**
- 1630 – 1800 **Tutorials**
- 1800 – 1930 **WELCOME RECEPTION** (Main Foyer)
- 1900 – 2100 **FRINGE TECHNICAL MEETINGS**

TUESDAY 13 MARCH, 2012

0730

REGISTRATION and SPEAKERS' BREAKFAST

1.1

Plenary: Opening and Keynote

Room - Grosser Saal 0830-1030

Moderator: W Rosenstiel, Tuebingen U and edacentrum, DE

0830

OPENING REMARKS AND AWARDSW Rosenstiel, Tuebingen U and edacentrum, DE
L Thiele, ETH Zurich, CH

Presentation of Distinguished Awards

0910

THE MOBILE SOCIETY - CHANCES AND CHALLENGES FOR MICRO- AND POWER ELECTRONICSK Meder, President, Automotive Electronics Division,
Robert Bosch GmbH, DE

0950

NEW FOUNDRY MODELS - ACCELERATIONS IN TRANSFORMATIONS OF THE SEMICONDUCTOR INDUSTRYM Chian, Senior Vice President Design Enablement,
GLOBALFOUNDRIES, DE

1030

EXHIBITION BREAK**Types of papers**

Tracks 1, 2, 3, 4, 5, 6, 7 and 8 (except the executive sessions 2.1, 3.1 and 4.1) of the conference programme will present scientific papers that have been reviewed based on their contribution in scientific innovation. Long presentation papers are allocated a 30-minute time slot for presentation and questions. Short presentation papers are allocated a 15-minute time slot for presentation and questions. All papers are published in the DATE 12 Proceedings on DVD.

Track IP contains the interactive presentations which are scientific papers that have been reviewed based on the criteria of presenting work in progress. The Interactive Presentation papers will be presented in 5 separate IP Sessions which will be held on the lower ground level close to the Exhibition area and will also each be introduced in a brief one-minute presentation during the relevant session prior to the IP Session. These papers are also published in the DATE 12 Proceedings on DVD.

(A) = Best Paper Award Candidate**IP = Interactive presentation**

SESSIONS technical sessions

2.1

EXECUTIVE SESSION - What Roles will the Foundries and Fabless Houses Play in Advanced Technology Nodes?

Room - Saal 5 1130-1300

Moderator:

Yervant Zorian,
Synopsys, US

Organiser:

Malcolm Penn,
Future Horizons, UK

Executives:

Robert Cadman,
General Manager & Vice President, eSilicon

Yves Mathys,
CEO, Abilis Systems, CH

Douglas Pattullo,
Director of Technology Support, TSMC Europe

Gerd Teepe,
Vice President, GLOBALFOUNDRIES, DE

Abstract: The continuously technology scaling in advanced nodes can dramatically impact business performance of the semiconductor industry. It can also significantly affect the age-old COT flow, fabless design and pure play wafer manufacturing flow. The executives in this session will discuss future trends and upcoming changes in the semiconductor industry and their impact on the roles to be played by of the foundries, the fabless houses and the rest of the value chain.

1300

LUNCH BREAK

2.2

Validation of Modern Microprocessors

Room - Konferenz 6 1130-1300

Moderators:

D Grosse, Bremen U, DE

V Bertacco, U of Michigan, US

The session highlights novel contributions to provide functional correctness in modern microprocessors. The first two papers focus on validating the memory subsystem in multi-core designs. The next two presentations improve test generation and simulation of instruction streams. Finally, the session discusses the verification of interconnect in multi-cores. The IP-presentations range from instruction-level to application validation.

TUESDAY

1130 (A)

AUTOMATED GENERATION OF DIRECTED TESTS FOR TRANSITION COVERAGE IN CACHE COHERENCE PROTOCOLS

X Qin and P Mishra, Florida U, US

1200

ON ESL VERIFICATION OF MEMORY CONSISTENCY FOR SYSTEM-ON-CHIP MULTIPROCESSING

E A Rambo, O P Henschel and L C V dos Santos, Federal U of Santa Catarina, BR

1215

GENERATING INSTRUCTION STREAMS USING ABSTRACT CSP

Y Katz, M Rimon and A Ziv, IBM Research - Haifa, IL

1230

A CYCLE-APPROXIMATE, MIXED-ISA SIMULATOR FOR THE BLIND ARCHITECTURE

T Stripf, R Koenig and J Becker, Karlsruhe Institute of Technology, DE

1245

A CLUSTERING-BASED SCHEME FOR CONCURRENT TRACE IN DEBUGGING NOC-BASED MULTICORE SYSTEMS

J Gao, J Wang, Y Han and X Li, Central South U, CN

IPs

IP1-1, IP1-2, IP1-3

1300

LUNCH BREAK

2.3

Memory System Optimisation

Room - Konferenz 1 1130-1300

Moderators:

T Austin, EECS, U Michigan, US

C Silvano, Politecnico di Milano, IT

This session will present new results in memory system optimisation. The first paper introduces a new modeling approach to 3D stacked memories. The second paper explores architectural support for efficiently managing software-based transactional memory meta-data. The third paper in the session examines an energy-efficient reconfigurable last-level cache design. The final paper in the session investigates DRAM system design for real-time systems.

1130

CACTI-3DD: ARCHITECTURE-LEVEL MODELLING FOR 3D DIE-STACKED DRAM MAIN MEMORY

K Chen and J B Brockman, Notre Dame U, US
S Li, N Muralimanchar and N P Iouppi, HP Labs, US
J H Ahn, Seoul National U, KR

1200

TAGTM - ACCELERATING STMS WITH HARDWARE TAGS FOR FAST META-DATA ACCESS

S Stipic, S Tomic, ? Feradz?, O Unsal, A Cristal and M Valero, Barcelona Supercomputing Centre, ES

1230

DYNAMICALLY RECONFIGURABLE HYBRID CACHE: AN ENERGY-EFFICIENT LAST-LEVEL CACHE DESIGN

Y-T Chen, H Huang, B Liu, C Liu, J Cong, M Potkonjak and G Reinman, UCLA, US

1245

DRAM SELECTION AND CONFIGURATION FOR REAL-TIME MOBILE SYSTEMS

M D Gomony, B Akesson and K Goossens,
TU Eindhoven, NL
C Weis and N Wehn, TU Kaiserslautern, DE

IPs

IP1-4, IP1-5

1300

LUNCH BREAK

2.4

Architectures and Efficient Designs for Automotive and Energy-Management Systems

Room - Konferenz 2 1130-1300

Moderator:

C Sebeke, Bosch, DE

G Merrett, Southampton U, UK

Modern systems, including transportation, smart buildings and wearable computing are increasingly distributed and need architecture designs, performance analysis methods, and smart policies striving for energy-efficient operation towards a goal of energy-neutrality. Presentations in this session include energy management algorithms and harvesting system design targeting energy-neutral operation from milliwatts to kilowatts and the timing analysis of Ethernet-based (automotive) architectures.

1130

USING TIMING ANALYSIS FOR THE DESIGN OF FUTURE SWITCHED BASED ETHERNET AUTOMOTIVE NETWORKS

J Rox and R Ernst, TU Braunschweig, DE
P Giusto, General Motors R & D, IT

1200

FAIR ENERGY RESOURCE ALLOCATION BY MINORITY GAME ALGORITHM FOR SMART BUILDINGS

C Zhang, W Wu, H Huang and H Yu,
Nanyang Technological U, SG

1230

ON DEMAND DEPENDENT DEACTIVATION OF AUTOMOTIVE ECUS

C Schmutzler and M Simons, Daimler AG, DE
J Becker, Karlsruhe Institute of Technology, DE

1245

SMART POWER UNIT FOR WIRELESS SENSOR NETWORK WITH ULTRA LOW POWER RADIO TRIGGER CAPABILITIES

M Magno and L Benini, Bologna U, IT
S Marinkovic, E Popovici and B O'Flynn,
U College Cork, IR
D Brunelli, Trento U, IT

IPs

IP1-6, IP1-7, IP1-8

1300

LUNCH BREAK

Physical Design for Low-Power

Room - Konferenz 3 1130-1300

Moderators:

J Teich, Erlangen-Nuremberg U, DE**W Fornaciari**, Politecnico di Milano, IT

The session addresses the issue of reducing the power consumption at the physical level. The first paper discusses the potential benefits of graphene-based power grids. The second one presents a leakage-aware FPGA routing algorithm. The third paper proposes a power-optimized SRAM cell under yield constraints. The last paper describes a new post-synthesis gate-level approach for leakage minimisation.

1130

OFF-PATH LEAKAGE POWER AWARE ROUTING FOR SRAM-BASED FPGAS**K Huang, Y Hu and X Li**,

Chinese Academy of Sciences, CN

B Liu, H Liu and J Gong,

Beijing Institute of Control Engineering, CN

1200

STABILITY AND YIELD-ORIENTED ULTRA-LOW-POWER EMBEDDED 6T SRAM CELL DESIGN OPTIMIZATION**A Makosiej and A Amara**,

Institut Supérieur d'Electronique de Paris, FR

O Thomas, CEA-LETI, MINATEC, FR**A Vladimerescu**, UC Berkeley, US

1215

POST-SYNTHESIS LEAKAGE POWER MINIMIZATION**M M Rahman and C Sechen**, U of Texas at Dallas, US

1230

IR-DROP ANALYSIS OF GRAPHENE-BASED POWER DISTRIBUTION NETWORKS**S Miryala, A Calimera, E Macii and M Poncino**,

Politecnico di Torino, IT

1300

LUNCH BREAK

Optimised Utilisation of Embedded Platforms

Room - Konferenz 4 1130-1300

Moderators:

F Slomka, Ulm U, DE**O Bringmann**, FZI Karlsruhe, DE

This session discusses different issues in embedded software with respect to the underlying hardware architecture. The first paper introduces a methodology for efficiently mapping teams of threads from a thread pool support nesting parallelism. A scalable methodology to map applications onto both homogeneous and heterogeneous platforms during run-time is presented in the second paper. The last paper proposes a new resource-efficient garbage collection policy for optimized usage of solid state disks in embedded applications.

1130

FAST AND LIGHTWEIGHT SUPPORT FOR NESTED PARALLELISM ON CLUSTER-BASED EMBEDDED MANY-CORES

P Burgio, A Marongiu and L Benini, DEIS - Bologna U, IT

1200

A DIVIDE AND CONQUER BASED DISTRIBUTED RUN-TIME MAPPING METHODOLOGY FOR MANY-CORE PLATFORMS

I Anagnostopoulos, G Kathareios, A Bartzas and D Soudris, NTU Athens, GR

1230

DUAL GREEDY: ADAPTIVE GARBAGE COLLECTION FOR PAGE-MAPPING SOLID-STATE DISKS

W-H Lin and L-P Chang, National Chiao-Tung U, TW

IPs

IP1-9, IP1-10

1300

LUNCH BREAK

2.7

**SPECIAL SESSION - HOT TOPIC:
EDA Solutions to New-Defect
Detection in Advanced Process
Technologies**

Room - Konferenz 5 1130-1300

Organiser/Moderator:**E J Marinissen**, IMEC, BE

For decades, EDA test generation tools for digital logic have relied on the Stuck-At fault model, despite the fact that process technologies moved forward from TTL (for which the Stuck-At fault model was originally developed) to nanometer-scale CMOS. Under pressure from their customers, especially in quality-sensitive application domains such as automotive, in recent years EDA tools have made great progress in improving their detection capabilities for new defects in advanced process technologies. For this Hot-Topic Session, we invited the three major EDA vendors to present their recent greatest innovations in high-quality automatic test pattern generation, as well as their lead customers to testify of actual production results.

1130

A CASE STUDY IN FASTER-THAN-AT-SPEED TESTINGG Vandling, Cadence Design Systems, US
S K Goel, TSMC, US

1200

CELL-AWARE LIBRARY CHARACTERIZATION FOR ADVANCED TECHNOLOGY NODES AND PRODUCTION TEST RESULTS FROM A 32NM PROCESSORF Hapke, Mentor Graphics, DE
J Rivers, AMD, US

1230

USING SLACK-BASED TRANSITION PATTERNS FOR ULTRA-HIGH DEFECT COVERAGEN Mittermaier, Synopsys, DE
S Bahl, ST Microelectronics, IT

1300

LUNCH BREAK

SPECIAL SESSION - EMBEDDED TUTORIAL: Beyond CMOS - Benchmarking for Future Technologies

Room - Exhibition Theatre 1130-1300

Moderators:

C M Sotomayor Torres, Catalan Institute of Nanotechnology, ES
W Rosenstiel, Tuebingen U and edacentrum, DE

Organiser:

R Popp, edacentrum, DE

Of key importance is to address the technological challenges posed by the emerging nanoelectronic concepts, of which a selection will be presented within the tutorial. After an overview on emerging technologies and their design aspects the embedded tutorial will present first benchmarking results for beyond CMOS technologies. Parameters to be considered include gain, signal/noise ration, non-linearity, speed, power consumption, architecture and integrability, efficiency, tolerances and manufacturability as well as the timeline of each potential technology.

1130

EMERGING TECHNOLOGIES: MORE MOORE AND MORE THAN MOORE

M Graef, TU Delft, NL

1148

TECHNOLOGY AND DESIGN CHALLENGES IN FUTURE LOW POWER MEMORY DEVICES AND CIRCUITS

P Fantini, Micron Semiconductors, IT

1206

BRIDGING TECHNOLOGY AND DESIGN FOR BEYOND CMOS

P Lugli, TU Munich, DE

1224

BRIDGING TECHNOLOGY AND DESIGN IN MORE THAN MOORE

A Ionescu, EPF Lausanne, CH

1242

BENCHMARKING FOR BEYOND CMOS TECHNOLOGIES

J Ahopelto, VTT, FI

1300

LUNCH BREAK

EXECUTIVE SESSION – How to handle today's design complexity?

Room - Konferenz 3 1430 - 1545

Organiser:

Yervant Zorian,
Synopsys, US

Moderator:

Gary Smith,
Gary Smith EDA, US

Executives:**Doug Aitelli,**

CEO, Calypto, US

Anton Domic,

Senior Vice President & GM, Synopsys, US

Venkata Simhadri,

Senior Vice President, Infotech, US

The widening gap between growing SOC complexity, designer productivity, and embedded software increasingly limits traditional system design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of complex SOC design. Executives from the IC value chain will present the technical and business challenges and the new opportunities in designing today's complex chips.

1545

EXHIBITION BREAK/IP1

3.2

Effective Functional Simulation and Validation

Room - Konferenz 6 1430-1600

Moderators:**P P Sanchez,** Cantabria U, ES**F Fummi,** Verona U, IT

The session covers several aspects of simulation, leading to effective functional validation of complex embedded systems. In particular, the session spans multi-core parallel simulation, accurate TLM simulation, mutation analysis improvement and properties emulation. The session is completed by two IPs on new topics: modeling heterogeneous embedded systems and simulating extensible processor cores.

1430

ACCURATELY TIMED TRANSACTION LEVEL MODELS FOR VIRTUAL PROTOTYPING AT HIGH ABSTRACTION LEVEL

K Lu, TU Munich, DE

1500

OUT-OF-ORDER PARALLEL SIMULATION FOR ESL DESIGN

W Chen, X Han and R Doemer, UC Irvine, US

1530

A PROBABILISTIC ANALYSIS METHOD FOR FUNCTIONAL QUALIFICATION UNDER MUTATION ANALYSISH-Y Lin, C-Y Wang, S-C Chang, H-M Chou, C-Y Huang, Y-C Yang and C-C Shen, National Tsing Hua U, TW
Y-C Chen, Chung Yuan Christian U, TW

1545

APPROXIMATING CHECKERS FOR SIMULATION ACCELERATIONB Mammo, U Michigan, US
D Chatterjee and V Bertacco, U of Michigan, US
D Pidan, A Nahir, A Ziv and R Morad, IBM Research Lab Haifa, IL

IPs

IP1-11, IP1-12, IP1-13

1600

EXHIBITION BREAK/IP1

Industrial Design Methodologies

Room - Konferenz 1 1430-1600

Moderators:

A Jerraya, CEA, FR

R Zafalon, STMicroelectronics, IT

This session presents 2-page papers detailing industrial design methodologies linking applications to hardware technologies.

1430

SYSTEMS ENGINEERING MODELLING GUIDELINES

D Steinbach, Cassidian, DE

1445

SURF ALGORITHM IN FPGA: A NOVEL ARCHITECTURE FOR HIGH DEMANDING INDUSTRIAL APPLICATIONS

N Battezzati, S Colazzo, M Maffione and L Senepa, Skytechnology, IT

1500

NOCEVE: NETWORK ON CHIP EMULATION AND VERIFICATION ENVIRONMENT FOR BILLION CYCLES APPLICATIONS

O Hammami, ENSTA ParisTECH, FR
X Li and M Brault, EVE, FR

1515

INVESTIGATING THE EFFECTS OF INVERTED TEMPERATURE DEPENDENCE (ITD) ON CLOCK DISTRIBUTION NETWORKS

R Goldman, V Melikyan and E Babayan, Synopsys Armenia, AM
S Rinaudo, STMicroelectronics, IT
A Sassone, A Calimera, A Macii, E Macii and M Poncino, Politecnico di Torino, IT

1530

CHALLENGES IN INTEGRATING 3D DESIGN COMPRISING A FIBER GLASS INTERPOSER AND TWO SILICON DIES

C-Y Hung, Venu Pattabhiramayengar and T G Yip, Rambus Inc, US

1545

EXHIBITION BREAK/IP1

Large-Scale Energy and Thermal Management

Room - Konferenz 2 1430-1600

Moderators:

G Palermo, Politecnico di Milano, IT

M Poncino, Politecnico di Torino, IT

Large scale computer systems require sophisticated energy management and low power communication policies. In this session novel approaches for charge distribution in energy storage systems, thermal management, low-power wide area networks, and advanced frequency scaling are presented.

1430

MULTIPLE-SOURCE AND MULTIPLE-DESTINATION CHARGE MIGRATION IN HYBRID ELECTRICAL ENERGY STORAGE SYSTEMS

Y Wang, Q Xie and M Pedram, Southern California U, US
 Y Kim and N Chang, Seoul National U, KR
 M Poncino, Politecnico di Torino, IT

1500

BENEFITS OF GREEN ENERGY AND PROPORTIONALITY IN HIGH SPEED WIDE AREA NETWORKS CONNECTING DATA CENTERS

B Aksanli and T Rosing, UC San Diego, US
 I Monga, Lawrence Berkeley National Laboratory, US

1530

QUANTIFYING THE IMPACT OF FREQUENCY SCALING ON THE ENERGY EFFICIENCY OF THE SINGLE-CHIP CLOUD COMPUTER

A Bartolini, M Sadri and L Benini, Bologna U, IT
 J-N Furst and A Y Coskun, Boston U, US

1545

NEIGHBOR-AWARE DYNAMIC THERMAL MANAGEMENT FOR MULTI-CORE PLATFORM

G Liu, M Fan and G Quan,
 Florida International U Miami, US

IPs

IP1-14

1600

EXHIBITION BREAK/IP1

3.5

PANEL: Key Challenges For The Next Generation of Computing Systems Taming the Data Deluge

Room - Konferenz 3 1430-1600

Organiser/Moderator:

R Riemenschneider, European Commission, BE

Panelists:

L Grasso, Fellow CATRENE/EUREKA, CH

E Ozer, ARM, UK

K Bertels, TU Delft, NL

K De Bosschere, Ghent U, BE

The exponential growth in IT made possible through Moore's law for several decades, however, has been surpassed by the demand for computing. Future high performance computing (HPC) systems are considered an area also relevant for traditional safety-critical embedded systems like automotive and aerospace.

HPC could also benefit from experiences in embedded computing in terms of fault-tolerant run-time environment (RTE) architectures with high degree of reliability and dependability.

The panel objective is to explore interdisciplinary technologies cutting across multi-core computing systems, dependable computing and high performance computing. The panel brings together industry and academia from so far fragmented domains such as real-time embedded system engineering and HPC architectures.

Model-Based Design and Verification for Embedded Systems

Room - Konferenz 4 1430-1600

Moderators:

W Yi, Uppsala U, SE

S Ben Salem, Verimag Laboratory, FR

This session consists of four presentations (2 long and 2 short) covering topics: controller synthesis for optimizing throughput in streaming applications, multitask implementation of synchronous reactive models and analysis of global timing constraints in automotive applications, and assertion-based verification of embedded software. In addition, the sessions contains also three associated interactive presentations addressing industrial design problems and solutions.

1430

PLAYING GAMES WITH SCENARIO AND RESOURCE-AWARE SDF GRAPHS THROUGH POLICY ITERATION

Y Yang, M Geilen, S Stuijk and H Corporaal, TU Eindhoven, NL

T Basten, TU Eindhoven

and Embedded Systems Institute, Eindhoven, NL

1500

VERIFYING TIMING SYNCHRONIZATION CONSTRAINTS IN DISTRIBUTED EMBEDDED ARCHITECTURES

A C Rajeev, S Mohalik and S Ramesh,

General Motors Technical Centre India Pvt, IN

1530

TASK IMPLEMENTATION OF SYNCHRONOUS FINITE STATE MACHINES

M Di Natale, Scuola Superiore S. Anna, IT

H Zeng, General Motors R&D, US

1545

ENABLING DYNAMIC ASSERTION-BASED VERIFICATION OF EMBEDDED SOFTWARE THROUGH MODEL-DRIVEN DESIGN

G Di Guglielmo, L Di Guglielmo, F Fummi

and G Pravadelli, Verona U, IT

IPs

IP1-15, IP1-16, IP1-17

1600

EXHIBITION BREAK/IP1

Improving Reliability and Yield in Advanced Technologies

Room - Konferenz 5 1430-1600

Moderators:

S Nassif, IBM, US

S Khursheed, Southampton U, UK

Papers in this session cover a broad range of solutions to improve reliability and yield. This is achieved by very fast yield and reliability simulations, design flows that handle single event upsets and instruction sets that mitigate NBTI.

1430 NBTI MITIGATION BY OPTIMIZED NOP ASSIGNMENT AND INSERTION

F Firouzi, S Kiamehr and M B Tahoori,
Karlsruhe Institute of Technology (KIT), DE

1500 AN ACCURATE SINGLE EVENT EFFECT DIGITAL DESIGN FLOW FOR RELIABLE SYSTEM LEVEL DESIGN

J Pontes and N Calazans, PUCRS, BR
P Vivet, LETI/CEA, FR

1530 (A) CROSS ENTROPY MINIMIZATION FOR EFFICIENT ESTIMATION OF SRAM FAILURE RATE

A Mohammed, UCLA, US

IPs IP1-18

1600 EXHIBITION BREAK/IP1

SPECIAL SESSION - HOT TOPIC: Design Automation Tools for Engineering Biological Systems

Room - Exhibition Theatre 1430-1600

Moderator/Organiser:
J Madsen, DTU, DK

Engineering of Biology encompasses the synthesis or enhancement of complex biologically based systems to elicit behaviors that do not exist in nature. This engineering perspective can be applied at several hierarchical levels spanning the design of particular proteins to re-engineering a particular cell to enhancing tissues and organism. Engineering biology promises to introduce new biotherapeutic, bioremediation, biosensing, bioenergy, and biomaterials based solutions to a diverse set of grand challenges. Recent examples include engineered bacteria to treat malaria, to invade cancer cells, to produce biofuels such as ethanol and butanol without many of the environmental concerns surrounding traditional petroleum processing, and to develop highly tuned biological agents to sense explosives. This session will cover the potential of synthetic and system biology, followed by design automation tools to support bottom-up construction approaches of synthetic gene regulatory circuits as well as top-down cellular system modeling and analysis methods.

1430 THE POTENTIAL OF SYNTHETIC AND SYSTEM BIOLOGY

J Stelling, ETH Zurich, CH

1500 EXPERIMENTALLY DRIVEN VERIFICATION FOR SYNTHETIC BIOLOGICAL CIRCUITS

D Densmore, E Appleton, R Ganguly, E A Gol,
S B Carr, S Bhatia, T Haddock and C Belta, Boston U, US
B Yordanov, Microsoft Research, UK

TUESDAY

1530

GENETIC/BIO DESIGN AUTOMATION: (RE-)ENGINEERING BIOLOGICAL SYSTEMS

S Hassoun, Tufts U, US

1600

EXHIBITION BREAK/IP1

IP1

Interactive Presentations

Room - Ground Floor 1600-1630

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP1-1

FAST CYCLE ESTIMATION METHODOLOGY FOR INSTRUCTION-LEVEL EMULATOR

D Thach, Y Tamiya, S Kuwamura and A Ike,
Fujitsu Laboratories, JP

IP1-2

VERIFICATION COVERAGE OF EMBEDDED MULTICORE APPLICATIONS

E Deniz and A Sen, Bogazici U, TK
J Holt, Freescale Semiconductor, US

IP1-3

HAZARD DRIVEN FUNCTIONAL VERIFICATION OF MULTITHREADED PROCESSORS

P Singh, Nvidia Inc, US
V Narayanan, Pennsylvania State U, US
D L Landis, Carnegie Mellon U, US

IP1-4

EXTENDING THE LIFETIME OF NAND FLASH MEMORY BY SALVAGING BAD BLOCKS

C Wang and W Fai, National U of Singapore, SG

IP1-5

A CASE STUDY ON THE APPLICATION OF REAL PHASE- CHANGE RAM TO MAIN MEMORY SUBSYSTEM

S Kwon, D Kim, Y Kim, S Yoo and S Lee, POSTECH, KR

IP1-6

A HIGH-PERFORMANCE DENSE BLOCK MATCHING SOLUTION FOR AUTOMOTIVE 6D-VISION

H Sahlbach, S Whitty and R Ernst, TU Braunschweig, DE

IP1-7

OPTIMIZATION INTENSIVE ENERGY HARVESTING

M Rofouei, M A Ghodrat and M Potkonjak, UCLA, US
A Martínez Nova, Centro U de Plasencia, ES

IP1-8

DESIGNING FLEXRAY-BASED AUTOMOTIVE ARCHITECTURES: A HOLISTIC OEM APPROACH

Paul Milbredt, Audi AG, DE
M Glass and J Teich, Erlangen-Nuremberg U, DE
M Lukasiewicz and S Chakraborty, TU Munich, DE
A Steininger, TU Vienna, AT

IP1-9

VIRTUALIZED ON-CHIP DISTRIBUTED COMPUTING FOR HETEROGENEOUS RECONFIGURABLE MULTI-CORE SYSTEMS

S Werner, O Oey, D Goehringer, M Huebner, J Becker,
Karlsruhe Institute of Technology (KIT), DE

IP1-10

VAMV: VARIABILITY-AWARE MEMORY VIRTUALIZATIONL Bathen, N Dutt and A Nicolau, UC Irvine, US
P Gupta, UCLA, US

IP1-11

HYBRID SIMULATION FOR EXTENSIBLE PROCESSOR CORESJ Jovic, S Yakoushkin, L G Murillo, J Eusse,
R Leupers and G Ascheid, RWTH Aachen U, DE

IP1-12

LEVERAGING RECONFIGURABILITY TO RAISE PRODUCTIVITY IN FPGA FUNCTIONAL DEBUGZ Poulos, J Anderson, A Veneris and B Le, Toronto U, CA
Y-S Yang, Vennsa Technologies, CA

IP1-13

MOUSSE: SCALING MODELLING AND VERIFICATION TO COMPLEX HETEROGENEOUS EMBEDDED SYSTEMS EVOLUTIONM Becker, G B Gnokam Defo and W Mueller,
Paderborn U, DE
F Fummi, G Pravadelli and S Vinco, Verona U, IT

IP1-14

RUNTIME POWER GATING IN CACHES OF GPUS FOR LEAKAGE ENERGY SAVINGSY Wang and N Ranganathan, South Florida U, US
S Roy, Advanced Micro Devices, US

IP1-15

AUTOMATIC GENERATION OF FUNCTIONAL MODELS FOR EMBEDDED PROCESSOR EXTENSIONS

F Sun, Tensilica Inc, US

IP1-16

SMARTTESTGEN: AN INTEGRATED TEST GENERATION TOOL FOR ENHANCED COVERAGE OF SIMULINK/STATEFLOW MODELSP Peranandam, S Raviram, A Yeolekar, A Gadkari,
A Satpathy and S Ramesh, General Motors, IN

IP1-17

MODEL DRIVEN RESOURCE USAGE SIMULATION FOR CRITICAL EMBEDDED SYSTEMSM Lafaye, Telecom ParisTech and Thales Avionics, FR
L Pautet and E Borde, Telecom ParisTech, FR
M Gatti and D Faura, Thales Avionics, FR

IP1-18

RAG: AN EFFICIENT RELIABILITY ANALYSIS OF LOGIC CIRCUITS ON GRAPHICS PROCESSING UNITS

M Li and M S Hsiao, Virginia Tech, US

4.1

EXECUTIVE SESSION: Addressing Trends & Challenges of Automotive Chips

Room - Saal 5 1700-1830

Organiser:Yervant Zorian,
Synopsys, US**Moderator:**Peggy Aycinena,
EDA Weekly, US

TUESDAY

Executives:

Joachim Lagenwalter,

Director Automotive Division, Mentor Graphics, DE

Helmut Lang,

Lead Automotive and Industrial Solutions Group, Freescale, DE

Maurizio Peri, General Manager Automotive R&D, STMicroelectronics, IT

While the new chips in the automotive industry keep growing both in functionality and numbers, the requirements for robustness and reliability remain as crucial as always given their safety critical application. The speakers in this executive session will address the current trends and challenges in the automotive

1830

CLOSE

4.2

Routing Solutions for Upcoming NoC Challenges

Room - Konferenz 6 1700-1830

Moderators:

J Flich, UP Valencia, ES

M Palesi, Kore U, IT

In this session, three upcoming challenges in the NoC domain will be addressed: aging effects on NoC routers and links, congestion due to traffic heterogeneity and yield concerns in a 3D environment. All these challenges call for an evolution of routing algorithms as will be documented in the papers of this session.

1700

CONGESTION AWARE TRAPEZOID-BASED ROUTING ALGORITHM FOR ON-CHIP NETWORKS

M Ebrahimi, M Daneshtalab, P Liljeberg, J Plosila and H Tenhunen, Turku U, FI

1730

AN MILP-BASED AGING-AWARE ROUTING ALGORITHM FOR NOCS

K Bhardwaj, K Chakraborty and S Roy, Utah State U, US

1800

AFRA: AN EFFICIENT DEALOCK-FREE RELIABLE ROUTING FOR 3D MESH NOCS

A Shafiee, Sharif U, IR
S Akbari, IUST, IR

IPs

IP2-1, IP2-2

1830

CLOSE

4.3

Industrial Embedded System Design

Room - Konferenz 1 1700-1830

Moderators:

F Clermidy, CEA-LETI, FR**T Simunic Rosing**, UC San Diego, US

This session presents papers dealing with industrial embedded system designs for different application areas, including automotive, energy efficiency and smart systems

1700

SMART SYSTEM DESIGN: INDUSTRIAL CHALLENGES AND PERSPECTIVES

M Lo Presti, **S Rinaudo** and **R Zafalon**,

STMicroelectronics, IT

1730

MIDDLEWARE SERVICES FOR SENSOR NETWORK INTEROPERABILITY IN SMART ENERGY EFFICIENT BUILDINGS

A Cucuccio, STMicroelectronics, IT**E Patti**, **F Abata**, **A Acquaviva**, **A Osello** and **E Macii**,

Politecnico di Torino, IT

M Jahn and **M Jentsch**,

Fraunhofer Institute of Technology, DE

1745

LOW-POWER EMBEDDED SYSTEM FOR REAL-TIME CORRECTION OF FISH-EYE AUTOMOTIVE CAMERAS

M Turturici and **S Saponara**, Pisa U, IT**L Fanucci**, Pisa U and CPR scarl C.so, IT**E Franchi**, R.I.CO srl, IT

1800

MECHATRONIC SYSTEM FOR ENERGY EFFICIENCY IN BUS TRANSPORT

M Donno, MECT S.r.l., IT**A Ferrari**, INTEGRA Renewable Energies S.r.l., IT**A Scarpelli**, ACTA S.r.l., IT**P Perlo**, Centro Ricerche FIAT S.C.p.A., IT**A Bocca**, Politecnico di Torino, IT

1815

INTELLIGENT AND COLLABORATIVE EMBEDDED COMPUTING IN AUTOMATION ENGINEERING

M Al Faruque and **A Candeo**,

Siemens Corporate Research, US

1830

CLOSE

4.4

System-Level Power and Reliability Estimation and Optimisation

Room - Konferenz 2 1700-1830

Moderators:

AK Coskun, Boston U, US**J-J Chen**, Karlsruhe Institute of Technology, DE

TUESDAY

This session presents power and reliability estimations and optimisations in system-level design. The first paper presents the system-level power analysis to extract variation-aware and correlation-inclusive leakage power models for fast and accurate system-level analysis. The second paper develops a power calibration approach by applying on-chip physical thermal sensors. The third paper discusses multicore systems driven by RF-powered smart cards for operational stability, while the last paper proposes an application-specific partitioned cache architecture to extend the lifetime for reliability and maintain the energy benefit.

1700

VARIATION-AWARE LEAKAGE POWER MODEL EXTRACTION FOR SYSTEM-LEVEL HIERARCHICAL POWER ANALYSIS

Y Xu, R Hasholzner and B Rohfleisch,

Intel Mobile Communications, DE

B Li, TU Munich, DE

C Haubelt and J Teich, Erlangen-Nuremberg U, DE

1730

RUNTIME POWER ESTIMATOR CALIBRATION FOR HIGH-PERFORMANCE MICROPROCESSORS

H Wang, S X-D Tan and X-X Liu, UC Riverside, US

R Quintanilla and A Gupta, Intel Co, US

1800

ESTIMATION BASED POWER AND SUPPLY VOLTAGE MANAGEMENT FOR FUTURE RF-POWERED MULTI-CORE SMART CARDS

N Druml, C Steger and R Weiss, TU Graz, AT

A Genser and J Haid, Infineon Technologies Austria AG, AT

1815

APPLICATION-SPECIFIC MEMORY PARTITIONING FOR JOINT ENERGY AND LIFETIME OPTIMIZATION

H Mahmood, E Macii and M Poncino,

Politecnico di Torino, IT

M Loghi, Udine U, IT

IPs

IP2-3, IP2-4

1830

CLOSE

4.5

EMBEDDED TUTORIAL - State-of-the-art Tools and Techniques for Quantitative Modelling and Analysis of Embedded Systems

Room - Konferenz 3 1700-1830

Organiser/Moderator:

A Legay, INRIA/Rennes, FR

The rigorous design of embedded systems radically differs from pure software design in that it should take into account not only functional but also extra-functional specifications regarding the use of resources of the execution platform such as time, memory and energy. Meeting extra-functional specifications is essential for the design of embedded systems.

It requires predictability of the impact of design choices on the overall behaviour of the designed system. It also implies a deep understanding of the interaction between application software and the underlying execution platform. This special session overview some of the well-established/recent tools and techniques developed for the design of rigorous embedded systems. What makes these tools unique is their ability to deal with both timing and stochastic aspects. We will start by introducing the UPPAAL real-time modeling and verification toolset and its underlying theory as well as recent features. Then, we will discuss the MODEST approach, that is a new unifying modeling paradigm allowing to interconnect stochastic and timed analysis tools in a semantically sound manner. Then, the BIP workflow for component-based design will be introduced. One of the major features of BIP is its ability to generate correct code for component coordination. Finally, model-based testing, that is already used in industry, and its potential integration in existing toolsets will be discussed.

1700

THE UPPAAL TOOLSET

K Larsen and A David, Aalborg U, DK
A Legay, INRIA/RENNES, FR

1725

MODEST AND THE TOOLSET

H Hermanns and A Hartmanns, Saarland U, DE

1745

COMPONENT-BASED DESIGN OF AUTONOMOUS SYSTEMS

M Bozga, Verimag Laboratory, FR

1810

MODELS, TESTING, AND MODEL-BASED TESTING

J Tretmans, ESI, Eindhoven, NL

1830

CLOSE

4.6 Compilers and Source-Level Simulation

Room - Konferenz 4 1700-1830

Moderators:

R Rabbah, IBM Research, US

B Franke, Edinburgh U, UK

This session focuses on compilers, both targeting single- and multi-core architectures, and source-level simulation approaches. A diverse range of topics ranging from instruction scheduling for energy minimisation through extraction of task-level parallelism to source-level simulation shedding light on data caches and compiler optimisations are presented. The session finishes with an interactive presentation on parallelisation of industry-relevant languages controlling cyber-physical systems.

1700

HYBRID SOURCE-LEVEL SIMULATION OF DATA CACHES USING ABSTRACT CACHE MODELS

S Stattelmann and O Bringmann, FZI Karlsruhe, DE
G Gerhard and C Cullmann,
Absint Angewandte Informatik GmbH, Saarbruecken, DE
W Rosenstiel, Tuebingen U and edacentrum, DE

1730

ACCURATE SOURCE-LEVEL SIMULATION OF EMBEDDED SOFTWARE WITH RESPECT TO COMPILER OPTIMIZATIONS

Z Wang and J Henkel, Karlsruhe Institute of Technology, DE

TUESDAY

1745 **SCHEDULING FOR REGISTER FILE ENERGY MINIMIZATION IN EXPLICIT DATAPATH ARCHITECTURES**
D She, Y He, B Mesman and H Corporaal,
TU Eindhoven, NL

1815 **MULTI-OBJECTIVE AWARE EXTRACTION OF TASK-LEVEL PARALLELISM USING GENETIC ALGORITHMS**
D Cordes and P Marwedel, TU Dortmund, DE

IPs **IP2-5**

1830 **CLOSE**

4.7

Advances in Test Generation

Room - Konferenz 5 1700-1830

Moderators:

G Mrugalski, Mentor Graphics, PL

S Hellebrand, Paderborn U, DE

This session covers advances in test generation, ranging from improving robustness for testing delay faults to testing for faults in between clock domains.

1700 (A) **RTL ANALYSIS AND MODIFICATIONS FOR IMPROVING AT-SPEED TEST**

K-H Chang and H-Z Chou, Avery Design Systems, US
I L Markov, U of Michigan at Ann Arbor, US

1730 **TEST GENERATION FOR CLOCK-DOMAIN CROSSING FAULTS IN INTEGRATED CIRCUITS**

N Karimi and K Chakrabarty, Duke U, US
P Gupta and S Patil, Intel Corp., US

1800 **A NEW SBST ALGORITHM FOR TESTING REGISTER FILES OF VLIW PROCESSORS**

D Sabena, M Sonza Reorda and L Sterpone,
Politecnico di Torino, IT

1815 **ON THE OPTIMALITY OF K LONGEST PATH GENERATION ALGORITHM UNDER MEMORY LIMITATIONS**

J Jiang and I Polian, Passau U, DE
M Sauer, A Czutro and B Becker, Freiburg U, DE

IPs **IP2-6, IP2-7**

1830 **CLOSE**

WEDNESDAY 14 MARCH, 2012

0730

REGISTRATION and SPEAKERS' BREAKFAST

5.1

E-MOBILITY HOT TOPIC - Embedded Systems and Software Challenges in Electric Vehicles

Room - Saal 5 0830-1000

Organiser/Moderator:

S Chakraborty, TU Munich, DE

The design of electric vehicles requires a complete paradigm shift in terms of embedded systems architectures and software design techniques that are followed within the conventional automotive systems domain. It is increasingly being realized that the evolutionary approach of replacing the engine of a car by an electric engine will not be able to address issues like acceptable vehicle range, battery lifetime performance, battery costs and weight, which are the core issues for the success of electric vehicles. While battery technology has crucial importance in the domain of electric vehicles, how these batteries are used and managed pose new problems in the area of embedded systems architecture and software for electric vehicles. This special session will feature a series of four talks that will outline many of these problems and the state-of-the-art in terms of how they might be addressed.

0830

EMBEDDED SYSTEMS ARCHITECTURE FOR ELECTRIC VEHICLES

M Lukasiewicz,

TUM-CREATE Centre for Electromobility, SG

0850

EMBEDDED SOFTWARE FOR ELECTRIC VEHICLES

C Buckl, Fortiss GmbH, DE

0910

HOW SEMICONDUCTOR REVOLUTIONS WILL ENABLE ELECTRIC VEHICLES?

P Leteinturier and H Adlkofer,

Infineon Technologies AG, DE

0930

HYBRID ELECTRICAL ENERGY STORAGE SYSTEMS

N Chang, S Park and Y Kim, Seoul National U, KR

0950

EXHIBITION BREAK/IP2

PANEL SESSION - Accelerators and emulators: Can they become the platform of choice for hardware verification?

Room - Konferenz 6 0830-1000

Moderator:

B Al-Hashimi, U Southampton, UK

Organiser:

R Morad, IBM Research - Haifa, IL

Panelists:

R Morad, IBM Research - Haifa, IL

B Hoppe, IBM Research & Development, DE

J Kumar, Intel Corp, US

F Schirrmeister, Cadence Design Systems, US

S Mitra, Stanford U, US

L Burgun, EVE, FR

The verification of modern hardware designs requires an enormous amount of simulation resources. A growing trend in the industry is the use of accelerators and emulators to support this effort. Because they are very fast compared to software simulators, accelerators and emulators provide the opportunity to significantly shorten the verification cycle. However, for this to happen challenges in all main aspects of the verification process (test-generation, checking, coverage and debugging) will first need to be solved. In this panel session, experts from both academia and industry (EDA vendors and users) will come together to present their ideas and experiences on how to best utilize accelerators and emulators to enhance the verification process.

1000

EXHIBITION BREAK/IP2

Medical and Healthcare Applications

Room - Konferenz 1 0830-1000

Moderators:

C Van Hoof, IMEC, BE

Y Chen, ETH Zuerich, CH

Biomedical and healthcare applications require multidisciplinary approaches from transistor-level circuit design to system-level design, from algorithmic optimisations to software solutions. In this session, three papers are highlighted focusing on various of these areas starting with a technique for motion artifact suppression in ECG monitoring. Next, the implementation of a compressed sensing method for low-power sensor networks is discussed. Finally, an ASIC in 0.18 um CMOS is suggested for a wearable system recording EMG, ECG, and EEG bio-electric signals.

0830 **A CLOSED-LOOP SYSTEM FOR ARTIFACT MITIGATION IN AMBULATORY ELECTROCARDIOGRAM MONITORING**
 M Shoaib, Princeton U, US
 G Marsh, H Garudadri and S Majumdar, Qualcomm Inc, US

0900 **ENABLING ADVANCED INFERENCE ON SENSOR NODES THROUGH DIRECT USE OF COMPRESSIVELY-SENSED SIGNALS**
 M Shoaib, N K Jha and N Verma, Princeton U, US

0930 **A MULTI-PARAMETER BIO-ELECTRIC ASIC SENSOR WITH INTEGRATED 2-WIRE DATA TRANSMISSION PROTOCOL FOR WEARABLE HEALTHCARE SYSTEM**
 G Yang, J Chen, F Jonsson, H Tenhunen and L-R Zheng, Royal Institute of Technology (KTH), SE

1000 **EXHIBITION BREAK/IP2**

5.4

Microarchitecture

Room - Konferenz 2 0830-1000

Moderators:

M Berekovic, TU Braunschweig, DE

T Austin, U of Michigan, US

This session will present new results in microarchitectural design. The first paper proposes a technique to widen the scope of branch history. The second paper investigates techniques to increase the state available to branch predictors. The third paper proposes an energy and storage frugal prefetcher. The final paper in the session examines an instruction retiming technique to tolerate process variation.

0830 **ENERGY-EFFICIENT BRANCH PREDICTION USING COMPILER-GUIDED HISTORY STACK**
 M Tan, X Liu, Z Xie, D Tong and X Cheng, Peking U, CN

0900 (A) **TOWARD VIRTUALIZING BRANCH DIRECTION PREDICTION**
 M Sadooghi-Alvandi, K Aasaraai and A Moshovos, Toronto U, CA

0930 **S/DC: A STORAGE AND ENERGY EFFICIENT DATA PREFETCHER**
 X Dang, X Wang, D Tong, J Lu, J Yi and K Wang, Peking U, CN

0945 **AN ARCHITECTURE-LEVEL APPROACH FOR MITIGATING THE IMPACT OF PROCESS VARIATIONS ON EXTENSIBLE PROCESSORS**
 M Kamal, A Afzali-Kusha and S Safari, Tehran U, IR
 M Pedram, Southern California U, US

IPs **IP2-8, IP2-9, IP2-10**

1000 **EXHIBITION BREAK/IP2**

Shared Memory Management in Multicore

Room - Konferenz 3 0830-1000

Moderators:

C Silvano, Polimi, IT

M Berekovic, TU Braunschweig, DE

This session presents innovations in shared memory management for multi-cores. The first paper applies a control theoretic approach to probabilistic allocation of the shared cache capacity. The second paper proposes a dynamic directories approach that eliminates a large fraction of on-chip interconnect traffic, reducing power consumption. The third paper designs a dynamic cache management scheme to reduce inter-partition contention in NUCA-based last level caches. The last paper proposes hierarchical barrier synchronisation schemes for shared memory MPSoCs.

0830

PCASA: PROBABILISTIC CONTROL-ADJUSTED SELECTIVE ALLOCATION FOR SHARED CACHES

K Aisopos, Princeton U, US

J Moses, R Illikkal and K Iyer, Intel, US

K Newell, AMD, US

0900

DYNAMIC DIRECTORIES: REDUCING ON-CHIP INTERCONNECT POWER IN MULTICORES

A Das, M Schuchardt, N Hardavellas, G Memik and A Choudhard, Northwestern U, US

0930

DYNAMIC CACHE MANAGEMENT IN MULTI-CORE ARCHITECTURES THROUGH RUN-TIME ADAPTATION

F Hameed, L Bauer and J Henkel,

Karlsruhe Institute of Technology, DE

0945

DESIGN OF A COLLECTIVE COMMUNICATION INFRASTRUCTURE FOR BARRIER SYNCHRONIZATION IN CLUSTER-BASED NANOSCALE MPSoCS

J L Abell, J Fernandez and M E Acacio, Murcia U, IT

D Bortolotti, A Marongiu and L Benini, DEIS - Bologna U, IT

D Bertozzi, Ferrara U, IT

1000

EXHIBITION BREAK/IP2

Scheduling and Allocation

Room - Konferenz 4 0830-1000

Moderators:

G Lipari, Scuola Superiore Sant'Anna, IT

R Kirner, Hertfortshire U, UK

This session presents research related to real-time scheduling and resource allocation on single processors, multi-core architectures and networks. The first paper proposes a novel delay-analysis for non-

preemptive regions scheduling in single processor embedded systems; the second paper proposes an allocation algorithm for partitioned scheduling in multi-core systems; the third paper presents an optimisation method for static scheduling of a time-triggered Network-on-Chip; the fourth paper improves the pessimism when analysing sporadic tasks systems.

0830

PREEMPTION DELAY ANALYSIS FOR FLOATING NON-PREEMPTIVE REGION SCHEDULINGJ Marinho, V Nelis and S M Petters, CISTER/ISEP, PT
I Puaut, Rennes II U, FR

0900

HARMONIC SEMI-PARTITIONED SCHEDULING FOR FIXED-PRIORITY REAL-TIME TASKS ON MULTI-CORE PLATFORM

M Fan and G Quan, Florida International U, US

0930

STATIC SCHEDULING OF A TIME-TRIGGERED NETWORK-ON-CHIP BASED ON SMT SOLVINGJ Huang, J O Blech, A Raabe and C Buckl, fortiss GmbH, DE
A Knoll, TU Munich, DE

0945

FORMAL ANALYSIS OF SPORADIC OVERLOAD IN REAL-TIME SYSTEMS

S Quinton, M Hanke and R Ernst, TU Braunschweig, DE

IPs

IP2-11, IP2-12

1000

EXHIBITION BREAK/IP2

5.7

Testing of Non-Volatile Memories

Room - Konferenz 5 0830-1000

Moderator:

R Aitken, ARM, US

B Tasic, NXP Semiconductors, NL

Papers in this session describe the challenges of testing non-volatile memories in advanced technology nodes. Topics covered are error patterns and interface-faults in flash memories and open defects in heating elements of MRAMs.

0830

ERROR PATTERNS IN MLC NAND FLASH MEMORY: MEASUREMENT, CHARACTERIZATION, AND ANALYSISY Cai, E F Haratsch, O Mutlu and K Mai,
Carnegie Mellon U, US

0900

MODELLING AND TESTING OF INTERFERENCE FAULTS IN THE DECA-NANO NAND FLASH MEMORY

J Zha, X Cui and C L Lee, Peking U, CN

0930

IMPACT OF RESISTIVE-OPEN DEFECTS ON THE HEAT CURRENT OF TAS-MRAM ARCHITECTURESJ Azevedo, A Virazel, A Bosio, L Dililo, P Girard
and A Todri, LIRMM, FR
G Prenat, CEA/SPINTEC, FR
J Herault and K Mackay, CROCUS Technologies, FR

IPs IP2-13

1000 EXHIBITION BREAK/IP2

IP2

Interactive Presentations

Room – Ground Floor 1000-1030

Each Interactive presentation will run on a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the morning. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP2-1 WORST-CASE DELAY ANALYSIS OF VARIABLE BIT-RATE FLOWS IN NETWORK-ON-CHIP WITH AGGREGATE SCHEDULING

F Jafari, A Jantsch and Z Lu,
Royal Institute Of Technology, SE

IP2-2 DYNAMIC-PRIORITY ARBITER AND MULTIPLEXER SOFT MACROS FOR ON-CHIP NETWORKS SWITCHES

G Dimitrakopoulos, Democritus U of Thrace, GR
E Kalligeros, U of the Aegean, GR

IP2-3 LOW POWER AGING-AWARE REGISTER FILE DESIGN BY DUTY CYCLE BALANCING

S Wang, T Jin, C Zheng and G Duan, Nanjing U, CN

IP2-4 POWERADVISER: AN RTL POWER PLATFORM FOR INTERACTIVE SEQUENTIAL OPTIMIZATIONS

A Ranjan, Calypto Design Systems, US
S Das and N Vyargheswarudu, Texas Instruments, US

IP2-5 TOWARDS PARALLEL EXECUTION OF IEC 61131 INDUSTRIAL CYBER-PHYSICAL SYSTEMS APPLICATIONS

A Canedo and A Al Faruque,
Siemens Corporate Research, DE

IP2-6 A SCAN PATTERN DEBUGGER FOR PARTIAL SCAN INDUSTRIAL DESIGNS

K Chandrasekar and S Sengupta, Intel Corporation, US
S K Misra and M S Hsiao, Virginia Tech, US

IP2-7 FAST-GP: AN RTL FUNCTIONAL VERIFICATION FRAMEWORK BASED ON FAULT SIMULATION ON GP-GPUS

N Bombieri, F Fummi and V Guarnieri, Verona U, IT

IP2-8 EXPLOITING BINARY TRANSLATION FOR FAST ASIP DESIGN SPACE EXPLORATION ON FPGAS

S Pomata, P Meloni, G Tuveri and L Raffo, Cagliari U, IT
M Lindwer, Silicon Hive, NL

IP2-9 DESIGN OF A LOW-ENERGY DATA PROCESSING ARCHITECTURE FOR WSN NODES

C Walravens and W Dehaene, KU Leuven, BE

IP2-10 APPLICATION-SPECIFIC POWER-EFFICIENT APPROACH FOR REDUCING REGISTER FILE VULNERABILITY

H Tabkhi and G Schirner, Northeastern U, US

IP2-11

ON-LINE SCHEDULING OF TARGET SENSITIVE PERIODIC TASKS WITH THE GRAVITATIONAL TASK MODEL

R Guerra and G Fohler, TU Kaiserslautern, DE

IP2-12

ONLINE SCHEDULING FOR MULTI-CORE SHARED RECONFIGURABLE FABRICL Chen, T Marconi and T Mitra,
National U of Singapore, SG

IP2-13

SHADOW COMPONENTS: A NEW TECHNIQUE FOR FPGA-BASED FAULT INJECTIONA Mohammadi, M Ebrahimi and A Ejlali,
Sharif U of Technology, IR

6.1

E-MOBILITY PANEL - Role of EDA in the Development of Electric Vehicles

Room - Saal 5 1100-1230

Organiser/Moderator:

O Bringmann,
FZI Karlsruhe, DE

Panellists:

S Jones, AVL List, AT**R Schweiger,** Cadence Design Systems, DE**D Ziegenbein,** ETAS, DE**G Sandmann,** The MathWorks, DE**N Smith,** Mentor Graphics, US**J Stahl,** Synopsys, US

Electric vehicles will only get widely accepted if driving range, comfort and safety do not differ significantly from today's cars with internal combustion engine. Microelectronics will play a remarkable role in implementing e.g. optimized energy management systems using situation-aware recuperation strategies, smart (re-)charging capabilities and advanced driving and operation strategies in upcoming EVs. However, the development process has to be closely interlinked across different domains which results into many new challenges for the EDA community. Therefore, this panel will discuss visions and recent advances within an interdisciplinary field of competence by bringing together leading tool vendors from different domains.

1230

LUNCH BREAK

6.2

EMBEDDED TUTORIAL - Memristor Technology in Future Electronic System Design

Room - Konferenz 6 1100-1230

Moderator:

R Tetzlaff, TU Dresden, DE

WEDNESDAY

Organisers:

R Tetzlaff, TU Dresden, DE

A Bruening, ZMDI AG, Dresden, DE

This special session is about Memristor Technology in Future Electronic System Design. The memristor is a novel nanoelectronic device that is very promising for emerging technologies. Although this device has been postulated 40 years ago, the invention of the crossbar latch by the HP group led by Stanley Williams, provided the first nanoelectronic realization of such device in 2008. Memristors, which are essentially resistors with memory, are able to perform logic operations as well storage information. "Williams expects to see memristors used in computer memory chips within the next few years. HP Labs already has a production-ready architecture for such a chip" (<http://www.hpl.hp.com/news/2010/apr-jun/memristor.html>). Memristors are outstanding candidates for future analog, digital and mixed signal circuits.

1100

BRAINS ARE MADE OF MEMRISTORS

L O Chua, UC Berkeley, US

1145

THE IONIC DRIFT MEMRISTOR - A UNIVERSAL MEMORY AND STORAGE ELEMENT?

S Williams, Hewlett-Packard Laboratories, US

1230

LUNCH BREAK

6.3

Thermal Aware Low Power Design

Room - Konferenz 1 1100-1230

Moderators:

A Macii, Politecnico di Torino, IT

A Garcia-Ortiz, Bremen U, DE

Thermal issues are getting mandatory in modern multicore 3D designs. This session presents four contributions addressing thermal modeling, management and their implications for designing energy efficient systems.

1100

TEMPOMP: INTEGRATED PREDICTION AND MANAGEMENT OF TEMPERATURE IN HETEROGENEOUS MPSOCS

S Sharifi, R Ayoub and T Simunic, UC San Diego, US

1130

THERMAL BALANCING OF LIQUID-COOLED 3D MPSOCS USING CHANNEL MODULATION

M Sabry, A Sridhar and D Atienza, EPF Lausanne, CH

1200

STATISTICAL THERMAL MODELLING AND MITIGATION STRATEGIES CONSIDERING LEAKAGE POWER VARIATIONS

D-C Juan and D Marculescu, Carnegie Mellon U, US
Y-L Chuang, Taiwan Semiconductor Manufacturing Company, TW
Y-W Chang, National Taiwan U, TW

1215

ANALYSIS AND RUNTIME MANAGEMENT OF 3D SYSTEMS WITH STACKED DRAM FOR BOOSTING ENERGY EFFICIENCY

J Meng and A Kivilcim Coskun, Boston U, US

1230

LUNCH BREAK

DATE12

Dresden, Germany

12-16 March 2012

6.4

Basic Techniques for Improving the Formal Verification Flow

Room - Konferenz 2 1100-1230

Moderators:**M Wedler**, Kaiserslautern U, DE**G Cabodi**, Politecnico di Torino, IT

A productive verification flow requires a strong guidance of the verification engineer at different levels of abstraction. The session proposes coverage metrics that provide valuable orientation in assertion-based verification and addresses the issue of verifying designs that are only partially completed. New procedures for diagnosis are also proposed.

1100

A GUIDING COVERAGE METRIC FOR FORMAL VERIFICATION

F Haedicke, D Grosse and R Drechsler, Bremen U, DE

1130

VERIFICATION OF PARTIAL DESIGNS USING INCREMENTAL QBF SOLVING

P Marin, C Miller, M Lewis and B Becker, Freiburg U, DE

1200

NON-SOLUTION IMPLICATIONS USING REVERSE DOMINATION IN A MODERN SAT-BASED DEBUGGING ENVIRONMENT

B Le, H Mangassarian, B Keng and A Veneris, Toronto U, CA

IPs

IP3-1

1230

LUNCH BREAK

6.5

System-on-Chip Composition and Synthesis

Room - Konferenz 3 1100-1230

Moderators:**T Stefanov**, Leiden U, NL**D Sciuto**, Politecnico di Milano, IT

This session addresses the synthesis and composition of System-on-Chip. The first paper addresses resource sharing of event models converted from SDF graphs. The second paper proposes a compositional approach for design space exploration based on pareto regions of individual components. The third paper presents a compositional approach for the integration of components with interface protocol mismatches.

WEDNESDAY

1100 **OPTIMIZING PERFORMANCE ANALYSIS FOR SYNCHRONOUS DATAFLOW GRAPHS WITH SHARED RESOURCES**

D Thiele and R Ernst, TU Braunschweig, DE

1130 (A) **COMPOSITIONAL SYSTEM-LEVEL DESIGN EXPLORATION WITH PLANNING OF HIGH-LEVEL SYNTHESIS**

H-Y Liu, M Petracca and L P Carloni, Columbia U, US

1200 **CORRECT-BY-CONSTRUCTION MULTI-COMPONENT SOC DESIGN**

R Sinha, INRIA, FR

P S Roop and Z Salcic, Auckland U, NZ

S Basu, Iowa State U, US

IPs **IP3-2, IP3-3**

1230 **LUNCH BREAK**

6.6 Timing Analysis

Room - Konferenz 4 1100-1230

Moderators:

P Puschner, TU Wien, AT

S M Petters, CISTER-ISEP, PT

The session focuses on the timing analysis for time-critical systems and presents techniques to make real-time systems time predictable. The first paper uses scenario-aware data flows and Markov chains to model functional and timing properties of applications. The second paper proposes an automatic allocation of instructions to scratchpad memory in order to meet the posed timing requirements. The third and the fourth paper present techniques for building time-predictable MPSoC systems. Paper three introduces a prioritized budgeted scheduling technique for accesses to shared SDRAM memory and paper four, the final paper, discusses synchronization constructs for multi-core applications and evaluates their time predictability.

1100 **MODEL CHECKING OF SCENARIO-AWARE DATAFLOW WITH CADP**

B Theelen, Embedded Systems Institute, NL

J-P Katoen and H Wu, RWTH Aachen U, NL

1130 **AN INSTRUCTION SCRATCHPAD MEMORY ALLOCATION FOR THE PRECISION TIMED ARCHITECTURE**

A Prakash and H Patel, Waterloo U, CA

1200 **BOUNDING WCET OF APPLICATIONS USING SDRAM WITH PRIORITY BASED BUDGET SCHEDULING IN MPSoCs**

H Shah and A Raabe, ForTISS GmbH, DE

A Knoll, TU Munich, DE

1215 **TIME ANALYSABLE SYNCHRONISATION TECHNIQUES FOR PARALLELISED HARD REAL-TIME APPLICATIONS**

M Gerdes, F Kluge and T Ungerer, Augsburg U, DE

C Rochange and P Sainrat, Paul Sabatier U, FR

IPs IP3-4

1230 LUNCH BREAK

6.7

HOT TOPIC - Design for Test and Reliability in Ultimate CMOS

Room - Konferenz 5 1100-1230

Moderator:

L Anghel, TIMA, FR

Organisers:

L Anghel, TIMA, FR**M Nicolaidis**, TIMA, FR

This special session brings together specialists from the DfT, DfY and DfR domains that will address key problems together with their solutions for the 14nm node and beyond, dealing with extremely complex chips affected by high defect levels, unpredictable and heterogeneous timing behavior, circuit degradation over time, including extreme situations related with the ultimate CMOS nodes, where all processor nodes, routers and links of single-chip massively parallel tera-device processors could comprise timing faults (such as delay faults or clock skews); a large percentage of these parts are affected by catastrophic failures; all parts experience significant performance degradations over time; and new catastrophic failures occur at low MTBF.

1100 DFT AND DFY FOR 14NM AND BEYOND

Y Zorian, Synopsys, US

1130 DESIGNING RELIABLE PROCESSOR CORES

T Karnik, J Tschanz, J Kulkarni, K Bowman, M Khellah, A Raychowdhury, C Tokunaga, S-L Lu and V De, Intel, US

1200 DESIGNING SINGLE-SHIP MASSIVELY PARALLEL PROCESSORS AFFECTED BY EXTREME FAILURE RATES

M Nicolaidis, L Anghel, N-E Zergainoh and D Avresky, TIMA, FR and INRIANC, DE

1230 LUNCH BREAK

6.1.2

LUNCHTIME KEYNOTE AND AWARDS

Room - Saal 5 1340-1400 Awards and 1400-1430 Keynote

1340 Awards Moderator: **Z Peng**, Linkoping U, SE

Awards: Presentation of the DATE 11 Best Paper Awards

BEST PAPER - RUN-TIME DEADLOCK DETECTION IN NETWORKS-ON-CHIP USING COUPLED TRANSITIVE CLOSURE NETWORKS

R Al-Dujaily, T Mak, F Xia and A Yakovlev, Newcastle U, UK

M Palesi, Kore U, IT

BEST IP - A FAULT TOLERANT DEADLOCK FREE ADAPTIVE ROUTING FOR ON-CHIP INTERCONNECTS

F Chaix, N-E Zergainoh and M Nicolaidis, TIMA Laboratory, FR
D Avresky, IRIANC, FR

Presentation of the EDAA Outstanding Dissertation Awards

1400

Moderator:

W Rosenstiel, Tuebingen U and edacentrum, DE

Keynote Speaker:

Dr Max Lemke, Deputy Head of Unit Embedded Systems & Control
European Commission, Directorate General Information Society and Media

Research and Innovation on Advanced Computing – an EU Perspective

Abstract: Under 'Components and Systems' in FP7-ICT, over the period 2007–2012, the EU has so far invested about 100M€ on Computing Systems research. Building on the industrial constituencies and activities of the Joint Technology Initiative ARTEMIS and complementing research on embedded systems and control, research and innovation on Computing Systems covers a broad spectrum of issues from multi-core scalability and mastering parallelism to hardware/software co-design and low energy/low cost chips. With the convergence of computing technologies, work covers the broad spectrum of computing systems from customised computing via data servers to high performance systems. Work builds on and expands from European industrial strengths in embedded and mobile computing with low cost and energy efficiency being key drivers.

After a short overview of the research supported, some major trends in computing systems and their role in our society will be discussed. First ideas of new funding opportunities under Advanced Computing Systems in ICT Work Programme 2013 will be outlined. An outlook towards the next Framework Programme for Research and Innovation "Horizon 2020" and an overview of recommendations received from consultation activities with the constituencies in the broad context of Computing will conclude the presentation.

1430

END OF SESSION

7.1

E-MOBILITY HOT TOPIC - Optimal Energy Management and Recovery for FEV

Room - Saal 5 1430-1600

Moderator:

K Knoedler, Robert Bosch GmbH, Heilbronn, DE

Organiser:

E Kural, AVL LIST GmbH, Graz, AT

New control, operation, and driving strategies are needed significantly to increase the efficiency, driving range, and safety of electric vehicles. This is to be achieved by the development of an intelligent energy management and recovery system, integrating existing

subsystems with on-board and off-board sensors. A particular focus will lie on an optimal cooperation between the electric drivetrain and the regenerative braking system, supported by data from radar, video, satellite navigation, car-to-infrastructure and car-to-car. This will consequently reduce the "range anxiety" that drivers of fully electric vehicles experience, through the realization of a longer, predictable and clearly displayed remaining electric driving range, with the use of highly innovative controller software algorithms.

1430

DEVELOPMENT OF A NEW CONCEPT FOR FEV AND THE INTEGRATION OF ADAS FUNCTIONALITIES

S Laversanne, Centre Technique de Velizy PSA Peugeot Citroen Velizy Villacoublay, FR

D Sanchez, Electronics, HMI and ITS Centro Tecnológico de Automoción de Galicia Vigo, ES

K Knoedler and J Steinmann, Robert Bosch GmbH, DE

1500

SIMULATION ENVIRONMENT DEVELOPMENT FOR THE OPTIMIZED ENERGY MANAGEMENT FOR FEV

S Jones and E Kural, AVL LIST GmbH, AT

J Zimmermann and O Bringmann,

FZI Research Center for Information Technology, DE

1530

SUBSYSTEM ASSESSMENT, SYSTEM INTEGRATION AND TEST METHODOLOGY

D Sanchez, Electronics, HMI and ITS Centro

Tecnológico de Automoción de Galicia Vigo, ES

S Laversanne, Centre Technique de Velizy PSA Peugeot Citroen Velizy Villacoublay, FR

1600

EXHIBITION BREAK/IP3

7.2

HOT TOPIC - Virtual Platforms: Breaking New Grounds

Room - Konferenz 6 1430-1600

Moderator:

S A Huss, TU Darmstadt, DE

Organiser:

R Leupers, RWTH Aachen U, DE

The case for developing and using virtual platforms (VPs) has now been made. If developers of complex HW/SW systems are not using VPs for their current design, complexity of next generation designs demands for their adoption. In addition, the users of these complex systems are asking either for virtual or real platforms in order to develop and validate the software that runs on them, in context with the hardware that is used to deliver some of the functionality. A key requirement is to keep pace with Moore's Law and the ever increasing embedded SW complexity by providing novel simulation technologies in every product release. The focus in this special session is on the latest applications and latest use cases for VPs. It gives an overview of where this technology is going and the impact on complex system design and verification.

- 1430** **MORE REAL VALUE FOR VIRTUAL PLATFORMS**
R Leupers, RWTH Aachen U, DE
- 1445** **CONFIGURABLE PROCESSOR-CENTRIC VIRTUAL PLATFORMS – NEW DOMAINS AND NEW USES**
G Martin, Tensilica, US
- 1500** **ARCHITECTURE-LEVEL HARDWARE/SOFTWARE DESIGN SPACE EXPLORATION FOR MULTICORES**
A Herkersdorf, TU Munich, DE
- 1515** **VIRTUAL PLATFORMS AND THEIR ECOSYSTEM**
F Schirrmeister, Cadence, US
- 1530** **SOFTWARE-DRIVEN VERIFICATION**
T Kogel, Synopsys, DE
- 1545** **VIRTUAL PLATFORMS FOR AUTOMOTIVE**
M Vaupel, Robert Bosch GmbH, DE
- 1600** **EXHIBITION BREAK/IP3**

7.3 Multimedia and Consumer Applications

Room - Konferenz 1 1430-1600

Moderators:

T Theocharides, Cyprus U, CY

F Kienle, TU Kaiserslautern, DE

The session on multimedia and consumer applications includes four papers, all dealing with hardware acceleration of complex applications onto FPGA prototypes. Three applications are from the multimedia domain: cortical object classification, error-resilient H.264/AVC coding and disparity estimation in stereoscopic vision. The fourth paper, from the finance mathematical domain, presents an efficient hardware implementation for option pricing.

- 1430** **AN FPGA-BASED ACCELERATOR FOR CORTICAL OBJECT CLASSIFICATION**
M Park, S Kestur, J Sabarad, V Narayanan and M J Irwin, Penn State U, US
- 1500** **POWER-EFFICIENT ERROR-RESILIENCY FOR H.264/AVC CONTEXT-ADAPTIVE VARIABLE LENGTH CODING**
M Shafique, B Zatt, S Rehman, F Kriebel and J Henkel, Karlsruhe Institute of Technology (KIT), DE
- 1530** **TOWARDS ACCURATE HARDWARE STEREO CORRESPONDENCE: A REAL-TIME FPGA IMPLEMENTATION OF A SEGMENTATION-BASED ADAPTIVE SUPPORT WEIGHT ALGORITHM**
C Ttofis and T Theocharides, Cyprus U, CY
- 1545** **AN FPGA-BASED PARALLEL PROCESSOR FOR BLACK-SCHOLES OPTION PRICING USING FINITE DIFFERENCES SCHEMES**
G Chatziparaskevas, TU Crete, GR
I Papaefstathiou and A Brokalakis, Synelixis Solutions Ltd, GR

IPs

IP3-5

1600

EXHIBITION BREAK/IP3

7.4

Nanoelectronic Devices

Room - Konferenz 2 1430-1600

Moderators:

S Garg, Toronto U, CA

C Nicopoulos, Cyprus U, CY

This session comprises three papers. The first one discusses optimisation of polymorphic circuits. The Second paper discusses all optical reversible binary adder. We conclude the session by a novel Cantilever NEMs based switch for logic computation.

1430

A SAT-BASED FITNESS FUNCTION FOR EVOLUTIONARY OPTIMIZATION OF POLYMORPHIC CIRCUITS

Z Vasicek and L Sekanina, TU Brno, CZ

1500

MACH-ZEHNDER INTERFEROMETER BASED DESIGN OF ALL OPTICAL REVERSIBLE BINARY ADDER

S Kotiyal, H Thapliyal and N Ranganathan, South Florida U, US

1530

WEIGHTED AREA TECHNIQUE FOR ELECTROMECHANICALLY ENABLED LOGIC COMPUTATION WITH CANTILEVER-BASED NEMS SWITCHES

S Patil, M Jang, D J Lilja and S Campbell, Minnesota U, US

IPs

IP3-6, IP3-7, IP3-8

1600

EXHIBITION BREAK/IP3

7.5

High Level and Statistical Design of Mixed-Signal Systems

Room - Konferenz 3 1430-1600

Moderators:

C Dehollain, EPF Lausanne, CH

D Morche, CEA-LETI, FR

The session concerns itself with two of the hottest topics in system level mixed-signal modeling and variability aware design. The first two papers apply SystemC and its analog extensions to high level modelling and design space exploration of multi-domain systems. The next two papers are focused on efficient yield and variability analysis of large analog circuits, whereas the final paper addresses the challenges related to topology synthesis.

1430

RESPONSE SURFACE BASED DESIGN SPACE EXPLORATION AND OPTIMISATION OF A WIRELESS SENSOR NODE POWERED BY A TUNABLE ENERGY HARVESTER

L Wang, T J Kazmerski, B M Al-Hashimi and M Aloufi, Southampton U, UK
J Wenninger, TU Vienna, AT

1500

HOLISTIC MODELLING OF HETEROGENEOUS EMBEDDED SYSTEMS WITH HIGH MULTI-DISCIPLINE FEEDBACK: APPLICATION TO A PRECOLLISION MITIGATION BRAKING SYSTEM

A Leveque, F Pecheux, M-M Louerat and A Aboushady, UPMC, LIP6, FR
F Cenni and S Scotti, STMicroelectronics, FR
A Massouri and L Clavier, IRCICA - FR CNRS 3024 - IEMN UMR CNRS 8520, FR

1515 (A)

HIERARCHICAL ANALOG CIRCUIT RELIABILITY ANALYSIS USING MULTIVARIATE NONLINEAR REGRESSION AND ACTIVE LEARNING SAMPLE SELECTION

E Maricau, D De Jonghe and G Gielen, KU Leuven, BE

1530

A FAST ANALOG CIRCUIT YIELD ESTIMATION METHOD FOR MEDIUM AND HIGH DIMENSIONAL PROBLEMS

B Liu, J Messaoudi and G Gielen, KU Leuven, BE

1545

FAST ISOMORPHISM TESTING FOR A GRAPH-BASED ANALOG CIRCUIT SYNTHESIS FRAMEWORK

M Meissner, O Mitea, L Luy and L Hedrich, Goethe-U Frankfurt, DE

IPs

IP3-9, IP3-10, IP3-11

1600

EXHIBITION BREAK/IP3

Advances in Dataflow Modelling and Analysis

Room - Konferenz 4 1430-1600

Moderators:

C Haubelt, Rostock U, DE
L S Indrusiak, York U, UK

This session addresses open problems in scheduling, synchronisation and design space exploration of streaming applications. The applied models of computation include (parametric) synchronous dataflow, Kahn Process Networks, and the synchronous paradigm.

1430

DESIGN OF STREAMING APPLICATIONS ON MPSOCS USING ABSTRACT CLOCKS

A Gamatie, CNRS/LIFL, FR

1500

SPDF: A SCHEDULABLE PARAMETRIC DATA-FLOW MOC

P Fradet, A Girault and P Poplavko, INRIA Rhone-Alpes, FR

1530

MODELLING STATIC-ORDER SCHEDULES IN SYNCHRONOUS DATAFLOW GRAPHS

M Damavandpeyma, S Stuijk, M Geilen
and H Corporaal, TU Eindhoven, NL
T Basten, TU Eindhoven
and Embedded Systems Institute, NL

1545

DESIGN SPACE PRUNING THROUGH HYBRID ANALYSIS IN SYSTEM-LEVEL DESIGN SPACE EXPLORATION

R Piscitelli and A Pimentel, Amsterdam U, NL

IPs

IP3-12

1600

EXHIBITION BREAK/IP3

7.7

Test and Repair of New Technologies

Room - Konferenz 5 1430-1600

Moderators:

J Tyszer, TU Poznan, PL

H-J Wunderlich, Stuttgart U, DE

This session focuses on test issues related to NoCs, 3D ICs and memristor-based RRAMs. The first paper deals with the efficient distribution of test data over a network on chip, while the second paper uses a lightweight network as a repair infrastructure for TSV-based 3D chips. Finally, the third paper presents a DFT and test strategy for resistive open detection in RRAMs.

1430

TEST PIN COUNT REDUCTION FOR NOC-BASED TEST DELIVERY IN MULTICORE SOCS

M Richter, Potsdam U, DE
K Chakrabarty, Duke U, US

1500

ON EFFECTIVE TSV REPAIR FOR 3D-STACKED ICS

L Jiang, F Yuan and Q Xu, The Chinese U of Hong Kong, CN
W Eklow, Cisco Systems, US

1530

DFT SCHEMES FOR MEMRISTOR-BASED RRAMS

N Haron and S Hamdioui, TU Delft, NL

IPs

IP3-13

1600

EXHIBITION BREAK/IP3

7.8

**SPECIAL SESSION - HOT TOPIC:
New Directions in Timing
Modeling and Analysis of
Automotive Software**

Room - Exhibition Theatre 1430-1600

Organiser/Moderator:

W Mueller, Paderborn U, DE

WEDNESDAY

Architecture, design, implementation, and analysis of automotive systems is a fairly complex process. Though the process is in general well understood, scaling and composing subsystems is critical with respect to various real-time requirements. This special session reviews the state-of-the-art in timing modeling and analysis in automotive systems development and gives a perspective to future directions. The first presentation summarizes different timing representations in the AUTOSAR standard and identifies perspectives on potential future extensions. The second presentation addresses the hot topic of probabilistic timing specification and analysis; and the third one illustrates a case study from automotive industry with focus on timing. The final presentation closes with an overview of timing analysis tools.

1430

TIMING MODELLING WITH AUTOSAR - CURRENT STATE AND FUTURE DIRECTIONS

S Kuntz, Continental Automotive, DE
M-A Peraldi-Frati, INRIA, CNRS, FR
H Blom and D Karlsson, Volvo Technology, SE

1500

CHALLENGES AND NEW TRENDS IN PROBABILISTIC TIMING ANALYSIS

S Quinton and R Ernst, TU Braunschweig, DE
D Bertrand and P Meumeu, INRIA, FR

1530

TIMING MODELLING & ANALYSIS IN THE AUTOMOTIVE DEVELOPMENT PROCESS - AN INDUSTRIAL CASE STUDY

A Hamann, Robert Bosch GmbH, DE

1545

TIMING ANALYSIS TOOLS FOR AUTOMOTIVE DESIGN - A COMPREHENSIVE OVERVIEW

S Schliecker, Syntavision, DE
W Ramisch, Inchron, DE
R Heckmann, Absint, DE
U Kiffmeier, dSPACE, DE
J Migge, RealTime-at-Work, FR

1600

EXHIBITION BREAK/IP3

IP3

Interactive Presentations

Room – Ground Floor 1600-1630

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP3-1

QBF-BASED BOOLEAN FUNCTION BI-DECOMPOSITION

H Chen and J Marques-Silva, U College Dublin, IE
M Janota, INESC-ID, Lisbon, PT

IP3-2

AUTOMATIC TRANSITION BETWEEN STRUCTURAL SYSTEM VIEWS IN A SAFETY RELEVANT EMBEDDED SYSTEMS DEVELOPMENT PROCESS

C Ellen, C Etzien and M Oertel, OFFIS, DE

- IP3-3** **TOWARDS NEW APPLICATIONS OF MULTI-FUNCTION LOGIC: IMAGE MULTI-FILTERING**
L Sekanina and V Salajka, TU Brno, CZ
- IP3-4** **MEMORY-MAP SELECTION FOR FIRM REAL-TIME SDRAM CONTROLLERS**
S Goossens, T Kouters, B Akesson and K Goossens, TU Eindhoven, NL
- IP3-5** **REAL-TIME IMPLEMENTATION AND PERFORMANCE OPTIMIZATION OF 3D SOUND LOCALIZATION ON GPUS**
Y Liang, Z Cui, S Zhao, K Rupnow, Advanced Digital Science Center, SG
Y Zhang, Sun Yat-sen U, CN
D L Jones and D Chen, Illinois U, US
- IP3-6** **IMPACT OF TSV AREA ON THE DYNAMIC RANGE AND FRAME RATE PERFORMANCE OF 3D-INTEGRATED IMAGE SENSORS**
A Xhakoni and G Gielen, KU Leuven, BE
D San Segundo Bello, IMEC, BE
- IP3-7** **MINIMIZING THE LATENCY OF QUANTUM CIRCUITS DURING MAPPING TO THE ION-TRAP CIRCUIT FABRIC**
M J Dousti and M Pedram, Southern California U, US
- IP3-8** **VOLTAGE PROPAGATION METHOD FOR 3-D POWER GRID ANALYSIS**
C Zhang, V F Pavlidis and G De Micheli, EPF Lausanne, CH
- IP3-9** **YIELD OPTIMIZATION FOR RADIO FREQUENCY RECEIVER AT SYSTEM LEVEL**
A Iouditski, S Nazin and R Hildebrand, LJK-UJF, Grenoble, FR
D Morche and A Reinhardt, CEA-LETI MINATEC, Grenoble, FR
- IP3-10** **PARALLEL STATISTICAL ANALYSIS OF ANALOG CIRCUITS BY GPU-ACCELERATED GRAPH-BASED APPROACH**
X-X Liu, S X-D Tan and H Wang, UC Riverside, US
- IP3-11** **AUTOMATED CRITICAL DEVICE IDENTIFICATION FOR CONFIGURABLE ANALOGUE TRANSISTORS**
R Rudolf, P Taatizadeh, R Wilcock and P Wilson, Southampton U, UK
- IP3-12** **ANALYSIS OF MULTI-DOMAIN SCENARIOS CAPTURING POWER AND PERFORMANCE CHARACTERISTICS FOR OPTIMIZED DYNAMIC POWER MANAGEMENT**
J Zimmermann and O Bringmann, FZI Karlsruhe, DE
W Rosenstiel, Tuebingen U and edacentrum, DE
- IP3-13** **PUF-BASED SECURE TEST WRAPPER DESIGN FOR CRYPTOGRAPHIC SOC TESTING**
U Kocabas, TU Darmstadt (CASED), DE
A Das, KU Leuven, BE

E-MOBILITY HOT TOPIC - Robustness Challenges in Automotive Electronics for Electric Vehicles

Room - Saal 5 1700-1830

Organiser/Moderator:**J Lau**, Infineon, DE

This special session addresses robustness challenges for electronic design in the era of electric vehicles, posed for instance by the complexity increase through electrification, or the combination of high and low voltage electronics. Solutions are discussed across the entire supply-chain beginning at the car manufacturer down to development and fabrication of microelectronic circuits, in order to build a seamless design for robustness methodology. Designing for robustness in this context means to translate the electronics' requirements coming from a mission profile into design constraints, which can be maintained and checked by EDA software for microelectronic products. In order to assess the robustness with respect to a given mission profile, solutions for cross-domain simulation are to be presented, which will go beyond classical design verification.

1700

COMPLEXITY, QUALITY AND ROBUSTNESS - THE CHALLENGES OF TOMORROW'S AUTOMOTIVE ELECTRONICS

U Abelein, SQA Electronics, Audi AG, DE

1730

DESIGN FOR ROBUSTNESS – A TIER 1 PERSPECTIVE

G Jerke and J Breibach, Robert Bosch GmbH, DE

1800

MEASURING AND IMPROVING THE ROBUSTNESS OF AUTOMOTIVE SMART POWER MICROELECTRONICS

T Nirmaier, V Meyer zu Bexten, M Tristl, M Harrant, M Kunze, M Rafaila, G Pelz and J Lau, Infineon, DE

1830

CLOSE

PANEL SESSION - What is EDA Doing for Trailing Edge Technologies?

Room - Konferenz 6 1700-1830

Moderator:**P Rolandi**, STMicroelectronics, IT**Organiser:****M Casale-Rossi**, Synopsys, US**Panellists:****A Bruening**, ZMDI, DE**A Domic**, Synopsys, US**R Kress**, Infineon, DE**J Sawicki**, Mentor Graphics, US**C Sebeke**, Robert Bosch, DE

Over the last decade, the semiconductor industry has advanced CMOS technology from 90nm to 20nm, and the EDA industry has developed a great deal of software tools and semiconductor IP to help design at the leading edge. However, in 2010 approximately 75% of design starts and 25% of wafers were fabricated using 130nm or greater CMOS technologies, at the so called trailing edge. There are possibly more designers working at the trailing edge than at the leading edge, and there is certainly much more to electronics than just "more of Moore". What is EDA doing – or what should EDA do – in order to better help design at the trailing edge of CMOS technology?

1830

CLOSE

8.3

Innovative Reliable Systems and Applications

Room - Konferenz 1 1700-1830

Moderators:

J Ayala, Madrid Complutense U, ES

MD Santambrogio, Politecnico di Milano, IT

The contributions in this track will illustrate the state-of-the-art in breaking-through solutions, which will provide viable solutions in tomorrow's silicon and embedded systems from the reliability perspective. The session is devoted to presentation and discussion of innovative reliable systems and applications with a high degree of industrial relevance.

1700

RELI: HARDWARE/SOFTWARE CHECKPOINT AND RECOVERY SCHEME FOR EMBEDDED PROCESSORS

T Li and S Parameswaran, New South Wales U, AU
R Ragel, Peradeniya, LK

1730

A CROSS-LAYER APPROACH FOR NEW RELIABILITY-PERFORMANCE TRADE-OFFS IN MLC NAND FLASH MEMORIES

C Zambelli, P Olivo and D Bertozzi, Ferrara U, IT
S Di Carlo, M Fabiano, M Indaco and P Prinetto, Politecnico di Torino, IT

1800

A RESILIENT ARCHITECTURE FOR LOW LATENCY COMMUNICATION IN SHARED-L1 PROCESSOR CLUSTERS

M Kakoe, I Loi and L Benini, DEIS - Bologna U, IT

1815

PERFORMANCE-RELIABILITY TRADEOFF ANALYSIS FOR MULTITHREADED APPLICATIONS

I Oz and O Tosun, Bogazici U, TR
H R Topcuoglu, Marmara U, TR
M Kandemir, Pennsylvania State U, US

IPs

IP4-1, IP4-2, IP4-3

1830

CLOSE

Advances in Formal SoC Verification

Room - Konferenz 2 1700-1830

Moderators:

D Grosse, Bremen U, DE

F Rahim, Atrenta, F

Increasing the scope of formal methods when dealing with complex systems requires employing non-traditional formalisms in well-selected application domains. In this session the formalisms of computer algebra are extended to deal with complex data paths. New ideas are proposed in order to prove liveness properties and to determine response times in communicating systems. New concepts of counterexample analysis are presented for efficient debugging.

1700

EFFICIENT GROEBNER BASIS REDUCTIONS FOR FORMAL VERIFICATION OF GALOIS FIELD MULTIPLIERS

J Lv and **P Kalla**, Utah U, US

F Enescu, Georgia State U, US

1730

DEADLOCK-FREEDOM VERIFICATION IN CREDIT-BASED FLOW-CONTROL NETWORKS

S Ray and **R K Brayton**, UC Berkeley, US

1800

FORMAL METHODS FOR RANKING COUNTEREXAMPLES THROUGH ASSUMPTION MINING

S Mitra, IIT Kharagpur, IN

P Dasgupta, IIT Karagpur, IN

A Banerjee, Indian Statistical Institute, IN

IPs

IP4-4

1830

CLOSE

Variability and Delay

Room - Konferenz 3 1700-1830

Moderators:

S Sapatnekar, Minnesota U, US

J Cortadella, UP Catalunya, ES

This session covers different aspects of PVT variability and delays. The first two papers propose models to analyse gate delays considering variability. The third paper proposes a novel clock skew scheduling scheme to optimize the performance of resilient circuits. The session will conclude with two interactive presentations on practical experiences on designing circuits with GALS and multiple clock domains.

1700 (A)

TRANSISTOR-LEVEL GATE MODEL BASED STATISTICAL TIMING ANALYSIS CONSIDERING CORRELATIONS

Q Tang, **A Zjajo**, **M Berkelaar** and **N van der Meijs**,

TU Delft, NL

1730

CURRENT SOURCE MODELLING FOR POWER AND TIMING ANALYSIS AT DIFFERENT SUPPLY VOLTAGES

C Knoth, H Jedda and U Schlichtmann, TU Munich, DE

1800

CLOCK SKEW SCHEDULING FOR TIMING SPECULATIONR Ye, F Yuan and Q Xu, The Chinese U of Hong Kong, CN
H Zhou, Northwestern U, US

IPs

IP4-5, IP4-6

1830

CLOSE

8.6

System-Level Optimisation of Embedded Real-Time Systems

Room - Konferenz 4 1700-1830

Moderators:**J Teich**, Erlangen-Nuremberg U, DE**J-J Chen**, Karlsruhe Institute of Technology, DE

This session presents three approaches to the system-level mapping problem. The first paper addresses uncertainties in the early stages through optimisation of robustness and flexibility. The second paper shows how hard real-time scheduling theory can be applied to get very fast mapping decisions for streaming systems. The third paper optimises the amount of FPGA resources needed to meet security constraints.

1700

ROBUST AND FLEXIBLE MAPPING FOR REAL-TIME DISTRIBUTED APPLICATIONS DURING THE EARLY DESIGN PHASES

J Gan, F Gruian, P Pop and J Madsen, TU Denmark, DK

1730

A METHODOLOGY FOR AUTOMATED DESIGN OF HARD-REAL-TIME EMBEDDED STREAMING SYSTEMS

M Bamakhrama, J T Zhai, H Nikolov and T Stefanov, Leiden U, NL

1800

CO-DESIGN TECHNIQUES FOR DISTRIBUTED REAL-TIME EMBEDDED SYSTEMS WITH COMMUNICATION SECURITY CONSTRAINTS

K Jiang, P Eles and Z Peng, Linkoping U, SE

IPs

IP4-7

1830

CLOSE

8.7

On-Line Test for Secure Systems

Room - Konferenz 5 1700-1830

Moderators:**X Vera**, Intel Labs Barcelona, ES**J Abella**, Barcelona Supercomputing Center, ES

Possible faults affecting secure systems are analysed and innovative approaches to test them on-line are proposed.

1700

LOGIC ENCRYPTION: A FAULT ANALYSIS PERSPECTIVEJ Rajendran, R Karri and O Sinanoglu, New York U, US
Y Pino, Air Force Research Labs, US

1730

LOW-COST IMPLEMENTATIONS OF ON-THE-FLY TESTS FOR RANDOM NUMBER GENERATORS

F Veljkovic, V Rozic and I Verbauwhe, KU Leuven, BE

1800

POST-DEPLOYMENT TRUST EVALUATION IN WIRELESS CRYPTOGRAPHIC ICSY Jin and D Maliuk, Yale U, US
Y Makris, U of Texas at Dallas, US

1830

CLOSE

8.8

EMBEDDED TUTORIAL - Batteries and Battery Management Systems

Room - Exhibition Theatre 1700-1830

Moderators/Organisers:

L Fanucci, Pisa U, IT

H Gall, austriamicrosystems, AT

This special session will cover the main issues that arise in the design and management of a battery for an electric vehicle. An insight into lithium technology along with the most interesting modeling approaches for predicting the battery performance is initially provided. Afterwards, the audience will understand the demanding requirements and standards that apply to ICs and systems for battery management. Then, focus will be on the architectures for Battery Management System (BMS) and on the main techniques for state of charge estimation and charge balancing. Finally, an innovative design and implementation of a BMS to be integrated in an electric vehicle will be presented. It includes the first almost fully-integrated active charge equalizer.

1700

BATTERY TECHNOLOGY AND MODELLINGA Thaler, M Cifrain and W Prochazka,
Virtual Vehicle Research and Test Center, AT

1715

REQUIREMENT AND STANDARDS FOR ICS AND SYSTEMS IN BATTERY MONITORING AND MANAGEMENT

M Brandl, austriamicrosystems, AT

1730

BMS ARCHITECTURES AND TECHNIQUES FOR STATE-OF-CHARGE ESTIMATION AND CHARGE EQUALIZATIONF Baronti, G Fantechi, L Fanucci, R Roncella,
R Saletti and S Saponara, U Pisa, IT

1800

BMS DESIGN AND INTEGRATION IN ELECTRIC VEHICLESM Wenger, V Lorentz and M Giegerich,
Fraunhofer IISB, DE

1830

CLOSE

Special Day More-than-Moore

THURSDAY 15 MARCH, 2012

0730

REGISTRATION and SPEAKERS' BREAKFAST

9.1

MORE THAN MOORE Embedded Tutorial – Setting the Scene: What is “More-than-Moore”?

Room - Saal 5 08:30 – 10:00

Organiser/Moderator:**M Brillouët**, CEA-Leti, FR

This session aims to introduce the More-than-Moore (MtM) domain.

In a first talk M Graef will explain what MtM is, what are the specificities of this field and through which methodology a MtM roadmap can be developed. More specifically he will detail the ongoing effort in the ITRS which diversified in the recent years from pure digital devices and technologies towards non-digital functions.

S Monfray will address the long term perspective in MtM technologies looking at emerging and innovative approaches which could enhance significantly the performance of existing MtM devices.

Finally H Lakner will sketch application perspectives of MtM technologies and how they will change the living and working environment in the nearby future, making human-machine cooperation more efficient

0830

ROADMAPPING ‘MORE THAN MOORE’

M Graef, TU Delft University, NL

0900

EMERGING MORE-THAN-MOORE TECHNOLOGIES

S Monfray, STMicroelectronics, FR

0930

FUTURE HUMAN-MACHINE COOPERATION – APPLICATION PERSPECTIVES OF MORE-THAN-MOORE TECHNOLOGIES

H Lakner, Fraunhofer Institute for Photonic Microsystems IPMS, Dresden, DE

J Pelka, Fraunhofer Group for Microelectronics, DE

1000

EXHIBITION BREAK/IP4

9.2

HOT TOPIC - Multi-Core Design: From Ultra-Low-Power Design to Exascale Computing

Room - Konferenz 6 0830-1000

Moderators:**R Hermida**, UCM Madrid, ES**T Simunic Rosing**, UCSD, US

Organiser:**D Atienza**, EPFL Lausanne, CH

This special session includes four papers that cover the whole design spectrum of multi-core design from ultra-low-power embedded systems to large-scale computing servers. The first paper discusses the latest advances in intelligent and energy-secure system architecture for "Green" server design. The second paper presents Platform 2012 (P2012), which is a significant step forward in programmable accelerator architectures for next-generation data-intensive embedded applications. The third paper explores the design of near-threshold ultra-low-power multi-core architectures for real-time bio-signals analysis. The fourth paper proposes novel multi-level co-scheduling techniques to minimize the energy consumption of parallel workloads in future multi-core processors of computing clusters.

0830

POWER MANAGEMENT OF CHIP MULTIPROCESSORS: CHALLENGES AND PITFALLS

P Bose, A Buyuktosunoglu, H Jacobson, M Gupta, J Darringer, M Healy, J Shin and A Weger, IBM, US

0900

PLATFORM 2012: BUILDING AN ECOSYSTEM FOR A SCALABLE, MODULAR AND HIGH-EFFICIENCY EMBEDDED COMPUTING ACCELERATORL Benini, STMicroelectronics, FR and Bologna U, IT
D Melpignano and E Flamand, STMicroelectronics, FR

0930

MULTI-CORE ARCHITECTURE DESIGN FOR ULTRA-LOW-POWER WEARABLE HEALTH MONITORING SYSTEMS

A Y Dogan, J Constantin, M Ruggiero, A P Burg and D Atienza, EPF Lausanne, CH

0945

REDUCING THE ENERGY COST OF COMPUTING THROUGH EFFICIENT SCHEDULING OF PARALLEL WORKLOADS

A K Coskun and C Hankendi, Boston U, US

1000

EXHIBITION BREAK/IP4


9.3 Architecture and Building Blocks for Secure Systems

Room - Konferenz 1 0830-1000

Moderators:**F Regazzoni**, ALaRI, CH**R Cheung**, City U of Hong Kong, CN

Making systems secure encompasses many levels of design, including security evaluations and countermeasures. This session presents solutions for trusted computing in possibly malicious hardware as well as latest ASIC implementations of the next hashing algorithm standard (SHA-3).

0830

SAFER PATH: SECURITY ARCHITECTURE USING FRAGMENTED EXECUTION AND REPLICATION FOR PROTECTION AGAINST TROJANED HARDWAREM Beaumont, B Hopkins and T Newby,
Defence Science and Technology Organisation, AU

0900 **ASIC IMPLEMENTATIONS OF FIVE SHA-3 FINALISTS**
X Guo, M Srivastav, S Huang, D Ganta, M B Henry,
L Nazhandali and P Schaumont, Virginia Tech, US

0930 **CONCLUDING THE SIDE CHANNEL ANALYSIS OF THE
SHA-3 FINALISTS**
M Zohner, M Kasper and M Stoettinger, CASED, DE

1000 **EXHIBITION BREAK/IP4**

9.4

Advances in High-Level Synthesis

Room - Konferenz 2 0830-1000

Moderators:

G Coutinho, ICL, UK

P Coussy, Bretagne-Sud U, FR

The three papers of this session address important problems in High-Level Synthesis using new practical approaches: the first two attack the issue of module selection; the last paper applies machine learning to explore a High-Level Synthesis design space.

0830 **COMBINING MODULE SELECTION AND REPLICATION
IN STREAMING PROGRAMS**
J Cong, M Huang, B Liu, P Zhang and Y Zou, UCLA, US

0900 **EXPLOITING AREA/DELAY TRADEOFFS IN HIGH-LEVEL
SYNTHESIS**
A Kondratyev, L Lavagno, M Meyer and Y Watanabe,
Cadence Design Systems, US

0930 **PREDICTING BEST DESIGN TRADE-OFFS: A CASE STUDY
IN PROCESSOR CUSTOMIZATION**
M Zuluaga, ETH Zurich, CH
E Bonilla, NICTA, AU
N Topham, Edinburgh U, UK

IPs **IP4-8**

1000 **EXHIBITION BREAK/IP4**

9.5

Supply Voltage and Circuitry Based Power Reductions

Room - Konferenz 3 0830-1000

Moderators:

M Lopez-Vallejo, UP Madrid, ES

W Nebel, Oldenburg U and OFFIS, DE

The session first focuses on low power research on 8T SRAMs and reversible circuits. Then voltage supply related issues as core based power gating and DVS as well as energy storage techniques are discussed.

THURSDAY

0830 **AUTOMATIC DESIGN OF LOW-POWER ENCODERS USING REVERSIBLE CIRCUIT SYNTHESIS**

R Wille, R Drechsler, C Osewold and A Garcia-Ortiz, Bremen U, DE

0900 **ULTRA LOW POWER LITHO FRIENDLY LOCAL ASSIST CIRCUITRY FOR VARIABILITY RESILIENT 8T SRAM**

V Sharma, KU Leuven and Holst Centre/IMEC, BE
S Cosemans and W Dehaene, KU Leuven and IMEC, BE
M Ashouei and J Huisken, Holst Centre/IMEC, BE
F Catthoor, IMEC and KU Leuven, BE

0915 **SLIDING-MODE CONTROL TO COMPENSATE PVT VARIATIONS IN DUAL CORE SYSTEMS**

H Pourshaghghi, TU Eindhoven, NL
H Fatemi, NXP Semiconductors, NL
J Pineda de Gyvez, NXP Semiconductors and TU Eindhoven, NL

0930 **MEMORY MISS POWER GATING**

R Strong, S H Kang, T Rosing and A Kahng, UC San Diego, US

0945 **STATE OF HEALTH-AWARE CHARGE MANAGEMENT IN HYBRID ELECTRICAL ENERGY STORAGE SYSTEMS**

Q Xie, X Lin, Y Wang and M Pedram, Southern California U, US
D Shin and N Chang, Seoul National U, KR

IPs

IP4-9, IP9-10

1000

EXHIBITION BREAK/IP4

9.6 Creation and Processing of System-Level Models

Room - Konferenz 4 0830-1000

Moderators:

E Villar, Cantabria U, ES

J Haase, TU Wien, AT

This session deals with automated abstraction of TLM models from RTL, refining UML specifications of distributed embedded systems, and checking the consistency of UML models.

0830 **AUTOMATED, RTL SIMULATIONS BASED APPROACH FOR CONSTRUCTING A CYCLE-APPROXIMATE, TRANSACTION LEVEL MODEL OF A MEMORY CONTROLLER**

V Todorov and H Reinig, Intel Mobile Communications, DE
D Mueller-Gritschneider and U Schlichtmann, TU Munich, DE

0900 **REFINEMENT OF UML/MARTE MODELS FOR THE DESIGN OF NETWORKED EMBEDDED SYSTEMS**

E Ebeid, F Fummi, D Quaglia and F Stefanni, Verona U, IT

0930 **DEBUGGING OF INCONSISTENT UML/OCL MODELS**

R Wille, M Soeken and R Drechsler, Bremen U, DE

IPs IP4-11

1000 EXHIBITION BREAK/IP4

9.7

Test and Monitoring of RF and Mixed-Signal ICs

Room - Konferenz 5 0830-1000

Moderators:

S Sattler, Erlangen-Nuremberg U, DE

H Stratigopoulos, IMAG / CNRS, FR

The session will discuss approaches for measuring IQ imbalances in RF transceivers, for inferring implicitly the performance of RF blocks using non-intrusive built-in sensors and for monitoring on-line the degradation due to aging of analogue filters that are part of safety-critical automobile electronics.

0830 AN ANALYTICAL TECHNIQUE FOR CHARACTERIZATION OF TRANSCEIVERS IQ IMBALANCES IN THE LOOP-BACK MODE

A Nassery and S Ozev, Arizona State U, US

0900 TESTING RF CIRCUITS WITH TRUE NON-INTRUSIVE BUILT-IN SENSORS

L Abdallah, H Stratigopoulos and S Mir,

TIMA Laboratory, FR

J Altet, UP Catalunya, ES

0930 MONITORING ACTIVE FILTERS UNDER AUTOMOTIVE AGING SCENARIOS WITH EMBEDDED INSTRUMENT

J Wan, U Twente / CTIT, NL

H G Kerkhoff, Twente U / CTIT, NL

IPs IP4-12

1000 EXHIBITION BREAK/IP4

IP4

Interactive Presentations

Room - Ground Floor 1000-1030

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the morning. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP4-1 ANALYSIS OF INSTRUCTION-LEVEL VULNERABILITY TO DYNAMIC VOLTAGE AND TEMPERATURE VARIATIONS

A Rahimi and R K Gupta, UC San Diego, US

L Benini, Bologna U, IT

IP4-2

CRASHTESTING SWAT: ACCURATE, GATE-LEVEL EVALUATION OF SYMPTOM-BASED RESILIENCY SOLUTIONS

A Pellegrini, T Austin and V Bertacco, U of Michigan, US
 J Jiang, Stanford U, US
 R Smolinski, S. Hari and S Adve,
 Illinois U at Urbana Champaign, US
 L Chen, Intel Co, US
 X Fu, Kansas U, US

IP4-3

A HYBRID HW-SW APPROACH FOR INTERMITTENT ERROR MITIGATION IN STREAMING-BASED EMBEDDED SYSTEMS

M M Sabry and D Atienza, EPF Lausanne, CH
 F Catthoor, IMEC, BE

IP4-4

PROBABILISTIC RESPONSE TIME BOUND FOR CAN MESSAGES WITH ARBITRARY DEADLINES

P Axer, M Sebastian and R Ernst, TU Braunschweig, DE

IP4-5

MOONRAKE CHIP -- EXPLORING PAUSIBLE CLOCKING BASED GALS DESIGN FOR 40-NM SYSTEM INTEGRATION

X Fan, M Krstic and E Grass, IHP Microelectronics, DE
 B Sanders and C Heer, Intel Mobile Communications, DE

IP4-6

STATIC ANALYSIS OF ASYNCHRONOUS CLOCK DOMAIN CROSSINGS

S Chaturvedi, Advanced Micro Devices (AMD) Inc, US

IP4-7

A SCALABLE GPU-BASED APPROACH TO ACCELERATE THE MULTIPLE-CHOICE KNAPSACK PROBLEM

B Suri, U D Bordoloi and P Eles, Linköping U, SE

IP4-8

ENHANCING NON-LINEAR KERNELS BY AN OPTIMIZED MEMORY HIERARCHY IN A HIGH LEVEL SYNTHESIS FLOW

S Mancini and F Rousseau, TIMA Laboratory, FR

IP4-9

WORKLOAD-AWARE VOLTAGE REGULATOR OPTIMIZATION FOR POWER EFFICIENT MULTI-CORE PROCESSORS

A A Sinkar, H Wang and N S Kim, Wisconsin Madison U, US

IP4-10

AN ENERGY EFFICIENT DRAM SUBSYSTEM FOR 3D INTEGRATED SOCS

C Weis and N Wehn, TU Kaiserslautern, DE
 I Loi and L Benini, DEIS - Bologna U, IT

IP4-11

ELIMINATING INVARIANTS IN UML/OCL MODELS

M Soeken, R Wille and R Drechsler, Bremen U, DE

IP4-12

A LOW OVERHEAD ON-CHIP SOURCE SYNCHRONOUS INTERFACE TIMING TEST SCHEME WITH CALIBRATION

H Kim and J A Abraham, The U of Texas at Austin, US

10.1

MORE-THAN-MOORE - Technologies

Room - Saal 5 1100-1230

DATE12

Dresden, Germany

12-16 March 2012

Organiser/Moderator:

M Brillouët, CEA-Leti, FR

This session describes more in depth some MtM technologies, namely analogue, rf and power.

H Graeb will address the challenges encountered in analogue design. Structure and symmetry analysis, analogue placement, design for aging, discrete sizing, sizing with in-loop layout, and performance space exploration will be detailed.

D Morche et al. will present the potential offered by new UWB pulse radio transceiver designs. An optimised architecture allows to reach state of the art performances both in energy efficiency and ranging accuracy for application in localisation and powered radio link for ambient intelligent.

Finally L Frey will show how renewable energy systems, smart grid, and e-mobility will benefit from power electronic systems with improved efficiency, high power density, and at low cost using new power devices and modules.

1100

ITRS 2011 ANALOG EDA CHALLENGES AND APPROACHES

H Graeb, TU Munich, DE

1130

UWB TECHNOLOGY: ENABLING ULTRA LOW POWER COMMUNICATIONS

D Morche, CEA-Leti, FR

M Pelissier, CEA-Leti, FR

G Masson, CEA-Leti, FR

P Vincent, CEA-Leti, FR

1200

POWER ELECTRONICS – NEW APPLICATIONS AND NEW CHALLENGES

L Frey, Fraunhofer-IISB, DE

1230

EXTENDED LUNCH AND EXHIBITION BREAK

10.2

HOT TOPIC - Pathways to Servers of the Future

Room - Konferenz 6 1100 - 1230

Organiser/Moderator:

G Fettweis, TU Dresden, DE

The Special Session on "Pathways to Servers of the Future" outlines a new research program set up at Technische Universität Dresden addressing the increasing energy demand of global internet usage and the resulting ecological impact of it. The program pursues a novel holistic approach that considers hardware as well as software adaptivity to significantly increase energy efficiency, while suitably addressing application demands. The session presents the research challenges and industry perspective.

THURSDAY

- 1100** **INTRODUCTION: PATHWAYS TO SERVERS OF THE FUTURE**
G Fettweis, TU Dresden, DE
- 1115** **ENERGY-ADAPTIVE HIGH-SPEED COMPUTING PLATFORM**
W Nagel, TU Dresden, DE
- 1130** **ENERGY-ADAPTIVE COMPUTING MANAGEMENT**
W Lehner, TU Dresden, DE
- 1145** **HARDWARE PLATFORMS OF THE FUTURE**
K-D Schubert, IBM, DE
- 1200** **OPERATING SYSTEMS FOR FUTURE COMPUTING**
C Schlaeger, AMD Dresden, DE
- 1215** **SEMICONDUCTOR TECHNOLOGY FOR FUTURE COMPUTING PLATFORMS**
G Teepe, GLOBALFOUNDRIES Dresden, DE
- 1230** **EXTENDED LUNCH AND EXHIBITION BREAK**

10.3

Side-Channel Analysis and Protection of Secure Embedded Systems

Room - Konferenz 1 1100 - 1230

Moderators:

F Regazzoni, ALaRI, CH

R Cheung, City U of Hong Kong, CN

Organisers:

P Schaumont, Virginia Tech, US

Side-Channel Attacks exploit physical leakage of cryptographic devices to reveal their secret information and pose a major security threat for embedded systems. This session focuses on several aspects of this problem. The presented papers range from a low-cost countermeasure for the AES blockcipher to novel attack techniques, including electromagnetic attacks as well as the exploitation of high-dimension leakage models.

- 1100 (A)** **AMPLITUDE DEMODULATION-BASED EM ANALYSIS OF DIFFERENT RSA IMPLEMENTATIONS**
G Perin, P Maurine, P Benoit and L Torres, LIRMM, FR
- 1130** **RSM: A SMALL AND FAST COUNTERMEASURE FOR AES, SECURE AGAINST FIRST- AND SECOND-ORDER ZERO-OFFSET SCAS**
M Nassar, Bull TrustWay - TELECOM ParisTech, FR
S Guilley, J-L Danger and Y Souissi, TELECOM ParisTech, FR
- 1200** **REVEALING SIDE-CHANNEL ISSUES OF COMPLEX CIRCUITS BY HIGH-DIMENSIONAL LEAKAGE MODELS**
A Heuser and M Stoettinger, TU Darmstadt, DE
W Schindler, Bundesamt fuer Sicherheit in der Informationstechnik (BSI), DE
- 1230** **EXTENDED LUNCH AND EXHIBITION BREAK**

10.4 Topics in High-Level Synthesis

Room - Konferenz 2 1100 - 1230

Moderators:

K Bertels, TU Delft, NL

P Brisk, UC Riverside, US

The first paper integrates physical design with High-Level Synthesis for 3D integrated circuits. The second focuses on pipelining of asynchronous systems. The last paper of the session attacks the problem of Multiple Constant Multiplications in the case of FIR filters on FPGAs.

1100

3DHLS: INCORPORATING HIGH-LEVEL SYNTHESIS IN PHYSICAL PLANNING OF THREE-DIMENSIONAL (3D) ICS

Y Chen, G Sun, Q Zou and Y Xie, Penn State U, US

1130

MULTI-TOKEN RESOURCE SHARING FOR PIPELINED ASYNCHRONOUS SYSTEMS

J Hansen and M Singh, UNC-Chapel Hill, US

1200

DESIGN OF LOW-COMPLEXITY DIGITAL FINITE IMPULSE RESPONSE FILTERS ON FPGAS

L Aksoy, INESC-ID, PT

E Costa, UCPEL, BR

P Flores and J Monteiro, INESC-ID/IST TU Lisbon, PT

1230

EXTENDED LUNCH AND EXHIBITION BREAK

10.5 Modelling of Complex Analogue and Digital Systems

Room - Konferenz 3 1100 - 1230

Moderators:

T Kazmierski, Southampton U, UK

N van der Meijs, TU Delft, NL

This session addresses a range of difficult topics in modelling and simulation of analog, digital and mixed circuits. The first paper presents a novel methodology for identification of dynamical models of multiport structures. The remaining three papers are concerned with modelling and design issues of VCO's and monolithic inductors.

1100

AN EFFICIENT FRAMEWORK FOR PASSIVE COMPACT DYNAMICAL MODELLING OF MULTIPORT LINEAR SYSTEMS

Z Mahmood and L Daniel, MIT, US

R Suaya, Mentor Graphics, US

1130

ANALYSIS AND DESIGN OF SUB-HARMONICALLY INJECTION LOCKED OSCILLATORS

A Neogy and J Roychowdhury, UC Berkeley, US

THURSDAY

1200 **DESIGN OF AN INTRINSICALLY-LINEAR DOUBLE- VCO BASED ADC WITH 2ND-ORDER NOISE SHAPING**
P Gao, X Xing and G Gielen, KU Leuven, BE
J Craninckx, IMEC-SSET-Wireless, BE

1215 **LARGE SIGNAL SIMULATION OF INTEGRATED INDUCTORS ON SEMI-CONDUCTING SUBSTRATES**
W Schoenmaker and B De Smedt, MAGWEL NV, BE
M Matthies, S Baumanns and C Tischendorf, Cologne U, DE
R Janssen, NXP Semiconductors, NL

IPs **IP5-1, IP5-2**

1230 **EXTENDED LUNCH AND EXHIBITION BREAK**

10.6 Cyber-Physical Systems

Room - Konferenz 4 1100 - 1230

Moderators:

P Eles, Linkoping U, SE

R Ernst, TU Braunschweig, DE

Cyber-physical systems are embedded systems involving a tight interaction between computational (cyber) and physical entities. They involve jointly designing embedded controllers and computation/communication architectures. This session contains four papers addressing different aspects of cyber-physical systems design, covering application areas ranging from automotive architectures and software, to biofluidics. It also features 3 interactive presentations.

1100 **TIME-TRIGGERED IMPLEMENTATIONS OF MIXED-CRITICALITY AUTOMOTIVE SOFTWARE**
D Goswami, M Lukasiewicz, R Schneider and S Chakraborty, TU Munich, DE

1130 **TIMING ANALYSIS OF CYBER-PHYSICAL APPLICATIONS FOR HYBRID COMMUNICATION PROTOCOLS**
A Masrur, D Goswami and S Chakraborty, TU Munich, DE
J-J Chen, KIT, DE
A Annaswamy, MIT, US
A Banerjee, ISICAL, IN

1200 **A CYBERPHYSICAL SYNTHESIS APPROACH FOR ERROR RECOVERY IN DIGITAL MICROFLUIDIC BIOCHIPS**
Y Luo and K Chakrabarty, Duke U, US
T-Y Ho, National Cheng Kung U, TW

1215 **PREDICTIVE CONTROL OF NETWORKED CONTROL SYSTEMS OVER DIFFERENTIATED SERVICES LOSSY NETWORKS**
D Quaglia, Department of Computer Science, U Verona, IT
R Muradore and P Fiorini, U Verona, IT

IPs **IP5-3, IP5-4, IP5-5**

1230 **EXTENDED LUNCH AND EXHIBITION BREAK**

10.7

On-Line Test and Fault Tolerance

Room - Konferenz 5 1100-1230

Moderators:**D Gizopoulos**, Athens U, GR**M Nicolaidis**, TIMA Laboratory, FR

New approaches for on-line test and fault tolerance of logic and memory are proposed, together with system level reliability and yield evaluation solutions.

1100

INPUT VECTOR MONITORING ON LINE CONCURRENT BIST BASED ON MULTILEVEL DECODING LOGIC

I Voyiatzis, TEI of Athens, GR

1130

HIGH PERFORMANCE RELIABLE VARIABLE LATENCY CARRY SELECT ADDITION

K Du and P Varman, Rice U, US

K Mohanram, Pittsburgh U, US

1200

SALVAGING CHIPS BEYOND REPAIRS

H Hsiung, B Cha and S Gupta, Southern California U, US

1215

MITIGATING LIFETIME UNDERESTIMATION: A SYSTEM-LEVEL APPROACH CONSIDERING TEMPERATURE VARIATIONS AND CORRELATIONS BETWEEN FAILURE MECHANISMS

K-C Wu and D Marculescu, Carnegie Mellon U, US

M-C Lee and S-C Wang, National Tsing Hua U, TW

IPs

IP5-6, IP5-7, IP5-8

1230

EXTENDED LUNCH AND EXHIBITION BREAK

10.8

EMBEDDED TUTORIAL - Moore Meets Maxwell

Room - Exhibition Theatre 1100-1230

Organiser/Moderator:**R Camposano**, Nimbic Inc, US

Moore's Law has driven the semiconductor revolution enabling over four decades of scaling in frequency, size, complexity, and power. However, the limits of physics are preventing further scaling of speed, forcing a paradigm shift towards multicore computing and parallelization. In effect, the system is taking over the role that the single CPU was playing: high-speed signals running through chips but also packages and boards connect ever more complex systems. In this tutorial, we navigate through the often confusing terminology and concepts behind field solvers, show how advances in field solvers enable integration into EDA flows, present novel methods for model generation and passivity assurance in large systems, and demonstrate the power of cloud computing in enabling the next generation of scalable Maxwell solvers and the next generation of Moore's Law scaling of systems. We intend to show the truly symbiotic growing relationship between Maxwell and Moore!

THURSDAY

1100

NAVIGATING FIELD SOLVERS FOR EDA

V Jandhyala, U Washington, US

1130

PARALLELIZED, MULTICORE, AND CLOUD ALGORITHMS FOR FIELD SOLVERS

D Gope, Nimbic Inc, US

1200

FROM FIELDS TO CIRCUIT SIMULATION THROUGH PASSIVE MACROMODELLING

S Grivet-Talocia, Politecnico di Torin, IT

1230

EXTENDED LUNCH AND EXHIBITION BREAK

11.1

MORE-THAN-MOORE - Heterogeneous Integration

Room - Saal 5 14:00 – 15:30

Organiser/Moderator:

M Brillouët, CEA-Leti, FR

Systems need a heterogeneous integration of MtM technologies. The session will detail this topic with an emphasis on 2.5D and 3D integration.

Future 3D stacking solutions will require a combination of design, technology and reliability techniques with a strong emphasis on cost, size and performance. TSV and interposer technologies among others are hot topics which will be addressed by J Wolf et al. and M Scannell showing examples from the Dresden and Grenoble areas.

G Sun et al. will discuss the evolving memory hierarchy design with embedded NVMs, using dedicated circuit/architecture level models and presenting a holistic study of using NVM as on-chip/off-chip storage.

E J Marinissen will finally address the complex issue of testing 2.5D and 3D ICs, for which solutions are only emerging. These test challenges will be considered in terms of test flows, test contents, and test access.

1400

3D HETEROGENEOUS INTEGRATION – TOWARDS NEXT PACKAGING

J Wolf and K-D Lang, Fraunhofer IZM, DE

1415

UPDATE ON 3D ACTIVITIES AT CEA

M Scannell, CEA-Leti, FR

1430

EXPLORING MEMORY HIERARCHY DESIGN WITH EMERGING NON-VOLATILE MEMORIES

G Sun, Peking U, CN

C Xu and Y Xie, Pennsylvania State U, US

X Dong, Qualcomm, US

1500

CHALLENGES AND EMERGING SOLUTIONS IN TESTING TSV-BASED 2.5D- AND 3D-STACKED ICs

E J Marinissen, IMEC, BE

1530

BREAK/IP5

11.2 The Quest for NoC Performance

Room - Konferenz 6 1400-1530

Moderators:

D Bertozzi, Ferrara U, IT

C Seiculescu, EPF Lausanne, CH

This session contains two papers that reduce the time to set up circuits, by using parallelism and separate configuration infrastructures. The third paper uses inter-router links that are reversible in direction, in combination with packet splitting, to dynamically improve NoC performance.

1400

A TDM NOC SUPPORTING QOS, MULTICAST, AND FAST CONNECTION SET-UP

R Stefan and K Goossens, TU Eindhoven, NL

A Molnos, TU Delft, NL

J Ambrose, New South Wales U, AU

1430

PARALLEL PROBING: DYNAMIC AND CONSTANT TIME SETUP PROCEDURE IN CIRCUIT SWITCHING NOCS

S Liu, A Jantsch and Z Lu,

Royal Institute of Technology, SE

1500

A FLIT-LEVEL SPEEDUP SCHEME FOR NETWORK-ON-CHIPS USING SELF-RECONFIGURABLE BIDIRECTIONAL CHANNELS

Z Qian, Y Teh and C-Y Tsui,

The Hong Kong U of Science and Technology, CN

1530

BREAK/IP5

DATE12

Dresden, Germany

12-16 March 2012

11.3 Emerging Memory Technologies (1)

Room - Konferenz 1 1400-1530

Moderators:

G Sun, Peking U, CN

Y Liu, Tsinghua U, CN

This session includes three papers on emerging memory technologies. The first paper proposes spintronic memristor design for thermal sensors; The second paper presents a block mapping method for emerging 3D flash memory; The last paper in this session discusses the design implication of asymmetry of MTJ switching in STT-RAM designs.

1400

SPINTRONIC MEMRISTOR BASED TEMPERATURE SENSOR DESIGN WITH CMOS CURRENT REFERENCE

X Bi, C Zhang and H Li, Polytechnic Institute of New York U, US

Y Chen, Pittsburgh U, US

R E Pino, Air Force Research Lab, US

1430

3D-FLASHMAP: A PHYSICAL-LOCATION-AWARE BLOCK MAPPING STRATEGY FOR 3D NAND FLASH MEMORY

Y Wang and Z Shao, The Hong Kong Polytechnic U, CN

L A D Bathen and N D Dutt, UC Irvine, US

THURSDAY

1500

ASYMMETRY OF MTJ SWITCHING AND ITS IMPLICATION TO THE STT-RAM DESIGNS

Y Zhang, Y Li, A K Jones and Y Chen, Pittsburgh U, US
X Wang, Seagate Tech, US

IPs

IP5-9, IP5-10, IP5-11, IP5-12

1530

BREAK/IP5

11.4

Physical Anchors for Secure Systems

Room - Konferenz 2 1400-1530

Moderators:

L Torres, LIRMM, FR

V Fischer, Hubert Curien Laboratory, FR

Physically uncloneable functions, hardware Trojan detection and true random number generators, are particularly important to ensure security into systems. All these mechanisms, inserted at design time, have to be robust and efficient. This session will give an overview of these techniques, mainly addressing physical effects.

1400

COMPARATIVE ANALYSIS OF SRAM MEMORIES USED AS PUF PRIMITIVES

G-J Schrijen and V van der Leest, Intrinsic-ID, NL

1430

COMPARISON OF SELF-TIMED RING AND INVERTER RING OSCILLATORS AS ENTROPY SOURCES IN FPGAS

A Cherkaoui, V Fischer and A Hubert,
Hubert Curien Laboratory, FR
L Fesquet, TIMA Laboratory, FR

1500

A SENSOR-ASSISTED SELF-AUTHENTICATION FRAMEWORK FOR HARDWARE TROJAN DETECTION

M Li and A Davoodi, U Wisconsin - Madison, US
M Tehranipoor, U Connecticut, US

IPs

IP5-13

1530

BREAK/IP5

11.5

Analogue Design Validation

Room - Konferenz 3 1400-1530

Moderators:

M Zwolinski, Southampton U, UK

J Raik, TU Tallin, EE

This session is devoted to validation of analogue designs. The first paper proposes a technique based on fuzzy differential equations to simplify the verification of analogue circuits by reducing the computational complexity of the models. The second paper presents

a methodology for the evaluation of process variability impact on SRAM voltage level control assist techniques. The third paper proposes a parallelisable envelope following method for the transient analysis of switching power converter circuits. The fourth paper proposes a method for improving the calculation of limit cycle of oscillators in simulations using a novel integration formula. The session includes an interactive presentation proposing a new simulation algorithm using operational matrices for simulation of linear and fractional differential models.

1400

TOWARDS IMPROVING SIMULATION OF ANALOG CIRCUITS USING MODEL ORDER REDUCTION

H Aridhi and S Tahar, Concordia U, CA
M Zaki, British Columbia U, CA

1430

EFFICIENCY EVALUATION OF PARAMETRIC FAILURE MITIGATION TECHNIQUES FOR RELIABLE SRAM OPERATION

E I Vatajelu and J Figueras, UP Catalunya, ES

1500

A GPU-ACCELERATED ENVELOPE-FOLLOWING METHOD FOR SWITCHING POWER CONVERTER SIMULATION

X-X Liu, S Tan and H Wang, UC Riverside, US
H Yu, Nanyang Technological U, CN

1515

SIMULATION OF THE STEADY STATE OF OSCILLATORS IN THE TIME DOMAIN

H Brachtendorf, U of Applied Sciences of Upper Austria, AT
K Bittner, U of Applied Sciences of Upper Austria, AT
R Laur, Bremen U, DE

IP

IP5-14

1530

BREAK/IP5

11.6

Techniques and Technologies Power Aware Reconfiguration

Room - Konferenz 4 1400-1530

Moderators:

M Platzner, Paderborn U, DE

D Goehring, Fraunhofer Institute, DE

The papers in this session describe techniques and technologies to optimize power consumption in reconfigurable systems. The first paper describes a potentially disruptive technology that combines MEMS-based relays with programmable logic to realize significant power reduction. The second paper promotes a state-based predication to achieve low power in coarse grain reconfigurable architectures. The third paper present an energy-aware ultra-fast controller for managing runtime reconfiguration. The last paper presents a power-aware design space exploration for reconfigurable architectures.

1400

NANO-ELECTRO-MECHANICAL RELAYS FOR FPGA ROUTING: EXPERIMENTAL DEMONSTRATION AND A DESIGN TECHNIQUE

S Lee, R Parsa, S Chong, J Provine, J Watt, R T Howe,
H-S P Wong and S Mitra Stanford U, US

THURSDAY

1430 STATE-BASED FULL PREDICATION FOR LOW POWER CGRA ARCHITECTURE

K Han, S Park and K Choi, Seoul National U, KR

1500 POWER-AWARE ULTRA-RAPID RECONFIGURATION CONTROLLER

H Pham, R Bonamy, S Pillement and D Chillet, CAIRN IRISA/INRIA, U of Rennes 1, FR

1515 USING MULTI-OBJECTIVE DESIGN SPACE EXPLORATION TO ENABLE RUN-TIME RESOURCE MANAGEMENT FOR RECONFIGURABLE ARCHITECTURES

G Mariani, ALaRI - Lugano U, CH
V-M Sima and K Bertels, TU Delft, NL
G Palermo, V Zaccaria and C Silvano, Politecnico di Milano, IT

IP IP5-15

1530 BREAK/IP5

11.7 Rise and Fall of Layout

Room - Konferenz 5 1400-1530

Moderators:

R Otten, TU Eindhoven, NL

P Groeneveld, Magma Design Automation, US

For problem formulation in layout synthesis, one often resorts to mathematical programming. Yet many aspects require heuristic "post-synthesis" steps, that might diminish certain layout "qualities". In this session all these are addressed:

1. a rigorous treatment of placement legalisation,
2. power reduction by flip-flop merging and
3. the introduction of a new layout regularity metric.

1400 PHYSICAL SYNTHESIS: A SILICON REALITY CHECK

P Groeneveld, Magma Design Automation, US

1430 VLSI LEGALIZATION WITH MINIMUM PERTURBATION BY ITERATIVE AUGMENTATION

U Brenner, Bonn U, DE

1500 AGGLOMERATIVE BASED FLIP-FLOP MERGING FOR POWER OPTIMIZATION

S-Y Liu, C-J Lee and H-M Chen, National Chiao Tung U, TW

1515 FOCSI: A NEW LAYOUT REGULARITY METRIC

M Pons, UP Catalunya, ES
M Morgan and C Piguet, CSEM SA, CH

IPs IP5-16, IP5-17, IP5-18

1530 BREAK/IP5

11.8

HOT TOPIC - Programmability and Performance Portability Aspects of Heterogeneous Multi-/Manycore Systems

Room - Exhibition Theatre 1400-1530

Moderator:

C Kessler, Linköping U, SE

The general trend towards heterogeneity in multi-/manycore systems brings huge problems for software design, optimization and maintenance. Current programming systems are either platform-specific or are portable but have a low level of abstraction, such as OpenCL that requires explicit coding of data transfer, kernel launch etc., and re-optimization when migrating to a new device configuration. The main challenges are programmability of heterogeneous multi-/many-core systems, i.e., raising the level of abstraction and leveraging modern software engineering technology, and performance portability, i.e., best-effort automated adaptation of code to the underlying architecture. This special session presents three complementary approaches towards these goals.

1400

FLEXIBLE RUNTIME SYSTEM SUPPORT FOR HYBRID PARALLEL EXECUTION OF GENERIC COMPONENTS ON HETEROGENEOUS MULTICORE SYSTEMS: THE SKEPU-STARPU INTEGRATION

R Namyst and S Thibault,
INRIA and Bordeaux U, FR
U Dastgeer, Linköping U, SE

1430

THE OFFLOAD-C++ LANGUAGE AND COMPILER FOR PROGRAMMING OF HETEROGENEOUS MULTICORE SYSTEMS

P Keir, A Richards and U Dolinsky, Codeplay Inc., UK

1500

THE PEPPHER COMPONENT SYSTEM AND COORDINATION LANGUAGE FOR PERFORMANCE-PORTABLE PROGRAMMING OF HETEROGENEOUS MULTI-/MANYCORE SYSTEMS

S Benkner and S Pllana, U Vienna, AT
J L Traeff, TU Vienna, AT
U Dastgeer and C Kessler, Linköping U, SE

1530

BREAK/IP5

DATE12

Dresden, Germany

12-16 March 2012

Room - Ground Floor 1530-1600

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP5-1 **EFFICIENT VARIATION-AWARE EM-SEMICONDUCTOR COUPLED SOLVER FOR THE TSV STRUCTURES IN 3D IC**
Y Xu, L Jiang and N Wong, The U of Hong Kong, CN
W Yu, Tsinghua U, CN
Q Chen, UC San Diego, US

IP5-2 **VERIFYING JITTER IN AN ANALOG & MIXED SIGNAL DESIGN USING DYNAMIC TIME WARPING**
R Narayanan, A Daghar, M H Zaki and S Tahar,
 Concordia U, CA

IP5-3 **MEDS: MOCKUP ELECTRONIC DATA SHEETS FOR AUTOMATED TESTING OF CYBER-PHYSICAL SYSTEMS USING DIGITAL MOCKUPS**
B Miller and F Vahid, UC Riverside, US
T Givargis, UC Irvine, US

IP5-4 **COMPONENT-BASED AND ASPECT-ORIENTED METHODOLOGY AND TOOL FOR REAL-TIME EMBEDDED CONTROL SYSTEMS DESIGN**
R Hamouche and R Kocik, Paris-Est U - ESIEE, FR

IP5-5 **CYBER-PHYSICAL CLOUD COMPUTING: THE BINDING AND MIGRATION PROBLEM**
H Chen, R Hansen, J Huan, E Pereira, R Sengupta, R Swick and D Vizzini, UC Berkeley, US
C Kirsch, F Landolt, A Rottmann and R Trummer, Salzburg U, AT

IP5-6 **AN ADAPTIVE APPROACH FOR ONLINE HARD/SOFT FAULT MANAGEMENT IN MANY-CORE ARCHITECTURES**
C Bolchini, A Miele and D Sciuto,
 Politecnico di Milano, IT

IP5-7 **AN HYBRID ARCHITECTURE TO DETECT TRANSIENT FAULTS IN MICROPROCESSORS: AN EXPERIMENTAL VALIDATION**
S Campagna and M Violante,
 Politecnico di Torino - DAUIN, IT

IP5-8 **EVALUATION OF A NEW RFID SYSTEM PERFORMANCE MONITORING APPROACH**
G Fritz, V Beroulle, O Aktouf and D Hély,
 Grenoble INP - LCIS, FR

IP5-9 **A FRAMEWORK FOR SIMULATING HYBRID MTJ/CMOS CIRCUITS: ATOMS TO CIRCUITS APPROACH**
G Panagopoulos, C Augustine and K Roy, Purdue U, US

- IP5-10** **A BLOCK-LEVEL FLASH MEMORY MANAGEMENT SCHEME FOR REDUCING WRITE ACTIVITIES IN PCM-BASED EMBEDDED SYSTEMS**
D Liu, T Wang, Y Wang, Z Qin and Z Shao,
The Hong Kong Polytechnic U, CN
- IP5-11** **ARCHITECTING A COMMON-SOURCE-LINE ARRAY FOR BIPOLAR NON-VOLATILE MEMORY DEVICES**
B Zhao, J Yang and Y Zhang, Pittsburgh U, US
Y Chen, Pittsburgh, US
H Li, Polytechnic Institute of NYU, US
- IP5-12** **LAYOUT-AWARE OPTIMIZATION OF TWO-TERMINAL STT MRAMS**
S K Gupta, S P Park, N N Mojumder and K Roy,
Purdue U, US
- IP5-13** **CHARACTERIZATION OF THE BISTABLE RING PUF**
Q Chen, P Lugli, U Schlichtmann and U Röhrmair,
TU Munich, DE
G Csaba, Notre Dame U, US
- IP5-14** **AN OPERATIONAL MATRIX-BASED ALGORITHM FOR SIMULATING LINEAR AND FRACTIONAL DIFFERENTIAL CIRCUITS**
Y Wang, H Liu, G K H Pang and N Wong,
The U of Hong Kong, CN
- IP5-15** **A FLEXIBLE AND FAST SOFTWARE IMPLEMENTATION OF THE FFT ON THE BPE PLATFORM**
T Cupaiuolo, STMicroelectronics, IT
D Lo Iacono, STMicroelectronics, IT
- IP5-16** **HIERARCHICAL PROPAGATION OF GEOMETRIC CONSTRAINTS FOR FULL-CUSTOM PHYSICAL DESIGN OF ICS**
M Mittag and G Jerke, Robert Bosch GmbH, DE
A Krinke, TU Dresden, DE
W Rosenstiel, Tuebingen U and edacentrum, DE
- IP5-17** **DOUBLE-PATTERNING FRIENDLY GRID-BASED DETAILED ROUTING WITH ONLINE CONFLICT RESOLUTION**
I S Abed, Mentor Graphics, EG
A G Wassal, Cairo U, EG
- IP5-18** **DESIGN AND ANALYSIS OF VIA-CONFIGURABLE ROUTING FABRICS FOR STRUCTURED ASICS**
H-P Tsai, L-C Lai and R-B Lin, Yuan Ze U, TW

12.1

MORE-THAN-MOORE - Applications

Room - Saal 5 1600-1730

Organiser/Moderator:

M Brillouët, CEA-Leti, FR

This final session will give some examples of applications where MtM technologies are central.

THURSDAY

S Menezzo et al. will describe how silicon photonics allows higher data rates with reduced power consumption and increased port density in High Performance Computing, backplane server interconnects, Storage Area Network & Local Area Network applications. She will review the generic photonic building blocks that have recently been developed, and the strategy/challenges for their integration with electronics and for a high density integration.

C Coutier will show some examples as MEMS tactile sensor arrays for robotic applications which exemplifies the growing role of sensors in diversified applications.

Finally S Krone et al. will outline the importance of high-speed wireless solutions with reduced energy consumption per transmitted bit in healthcare. He will detail potential applications, showing the present limitations of the technology for a wireless medical smart card.

1600

SI PHOTONICS

S Menezzo and L Fulbert, CEA-Leti, FR

1630

MEMS SENSING: TACTILE SENSOR ARRAY FOR ROBOTIC APPLICATIONS

C Courtier, CEA-Leti, FR

1700

TOWARDS A WIRELESS MEDICAL SMART CARD

S Krone, B Almeroth, F Guderian and G Fettweis, TU Dresden, DE

1730

CLOSE

12.2

The Frontier of NoC Design

Room - Konferenz 6 1600-1730

Moderators:

K Goossens, TU Eindhoven, NL

S Murali, IMEC India, CH

Clocking is one main concern of nanoscale designs. This session presents advanced techniques that cope with this issue in the NoC domain, ranging from architecture co-design with high-speed clock distribution to the optimization of clockless architectures. The last paper focuses on a different technology platform and deals with calibration techniques for the microring resonators that build up most optical NoCs.

1600

A FAST, SOURCE-SYNCHRONOUS RING-BASED NETWORK-ON-CHIP DESIGN

A Mandal, S Khatri and R Mahapatra, Texas A&M U, US

1630

AREA EFFICIENT ASYNCHRONOUS SDM ROUTERS USING 2-STAGE CLOS SWITCHES

W Song, D Edwards, J Garside and W J Bainbridge, Manchester U, UK

1700

POWER-EFFICIENT CALIBRATION AND RECONFIGURATION FOR ON-CHIP OPTICAL COMMUNICATION

Y Zheng, Tsinghua U, CN and UC Santa Barbara, US
P Lisherness, M Gao, J Bovington and K-T Cheng, UC Santa Barbara, US
S Yang, Tsinghua U, CN

1730

CLOSE

12.3

Emerging Memory Technologies (2)

Room - Konferenz 1 1600-1730

Moderators:

H Li, NYU, US**Z Shao**, The Hong Kong Polytechnic U, CN

This session has three papers on emerging memory technologies. The first paper presents the modeling and design exploration of using FBDRAM as on-chip memory; the second paper proposes a wear leveling for PCRAM; the last paper presents a nonvolatile processor using FeRAM.

1600

MODELLING AND DESIGN EXPLORATION OF FBDRAM AS ON-CHIP MEMORY**G Sun**, Peking U, CN**C Xu and Y Xie**, Pennsylvania State U, US**Z Lv**, Micron Technology Inc, US

1630

BLOOM FILTER-BASED DYNAMIC WEAR LEVELING FOR PHASE CHANGE RAM**J Yun, S Lee and S Yoo**, POSTECH, KR

1700

A COMPRESSION-BASED AREA-EFFICIENT RECOVERY ARCHITECTURE FOR NONVOLATILE PROCESSORS**Y Wang, Y Liu, Y Liu, D Zhang and H Yang**, Tsinghua U, CN**B Sai and M Chiang**, Rohm Co Ltd, JP

1730

CLOSE

12.4

Digital Communication Systems

Room - Konferenz 2 1600-1730

Moderators:

F Kienle, TU Kaiserslautern, DE**F Clermidy**, CEA-LETI, FR

In this session new architectures for digital communication systems are proposed to improve flexibility, energy efficiency or area. Three specific applications are addressed. The first paper presents a network- on-chip-based channel decoder architecture, which provides high flexibility. The second paper introduces a low power adaptive channel estimator. The third paper proposes high performance FFT architecture.

1600

A NETWORK-ON-CHIP-BASED HIGH THROUGHPUT TURBO/LDPC DECODER ARCHITECTURE**C Condo, M Martina and G Masera**,

Politecnico di Torino, IT

1630

A COMPLEXITY ADAPTIVE CHANNEL ESTIMATOR FOR LOW POWER**Z Yu and C H van Berkel**, TU Eindhoven, NL**H Li**, NXP Semiconductors, NL

1700

A HIGH PERFORMANCE SPLIT-RADIX FFT WITH CONSTANT GEOMETRY ARCHITECTURE

J Kwong and M Goel, Texas Instruments, US

1730

CLOSE

12.5

Architecture and Networks for Adaptive Computing

Room - Konferenz 3 1600-1730

Moderators:**F Ferrandi**, Politecnico di Milano, IT**S Niar**, Valenciennes U, FR

The papers in this session deal with different architectures or networks to support adaptive computing. The first paper explores hardware specialization using domain-specific data paths. The second paper considers the Reorder Buffer design in FPGA-based superscalar processors. The third paper proposes placement and routing algorithms for reconfigurable accelerator augmentation to processors. The fourth paper develops heuristics for congestion-aware scheduling of NoCs based systems.

1600

SELECTIVE FLEXIBILITY: BREAKING THE RIGIDITY OF DATAPATH MERGING

M Stojilovic and L Saranovac, Belgrade U, RS

P Brisk, UC Riverside, US

D Novo and P Ienne, EPF Lausanne, CH

1630

AN OUT-OF-ORDER SUPERSCALAR PROCESSOR ON FPGA: THE REORDER BUFFER DESIGN

M Rosière, J-I Desbarbieux, N Drach and F Wajsbürt, UPMC - LIP6, FR

1700

PARTIAL ONLINE-SYNTHESIS FOR MIXED-GRAINED RECONFIGURABLE ARCHITECTURES

A Grudnitsky, L Bauer and J Henkel,

Karlsruhe Institute of Technology, DE

1715

CONGESTION-AWARE SCHEDULING FOR NOC-BASED RECONFIGURABLE SYSTEMS

H-L Chao, S-Y Tong and P-A Hsiung,

National Chung Cheng U, TW

Y-R Chen and S-J Chen, National Taiwan U, TW

1730

CLOSE

12.6

Boolean Methods in Logic Synthesis

Room - Konferenz 4 1600-1730

Moderators:**M Berkelaar**, TU Delft, NL**J Monteiro**, INESC-ID/TU Lisbon, PT

The session includes various papers on Boolean methods for logic synthesis. The first paper proposes a novel method for multi-error

logic rectification. The second paper presents new results on wire removal. The third paper evaluates the impact of introducing direct wires between LUTs in FPGAs. The fourth paper introduces new decompositions for index-generation functions. Finally, the fifth paper proposes a strategy to design on-chip sensors to track process variations

1600 MULTI-PATCH GENERATION FOR MULTI-ERROR LOGIC RECTIFICATION BY INTERPOLATION WITH COFACTOR REDUCTION

K-F Tang, P-K Huang, C-N Chou and C-Y Huang,
National Taiwan U, TW

1630 ALMOST EVERY WIRE IS REMOVABLE: A MODELLING AND SOLUTION FOR REMOVING ANY CIRCUIT WIRE

X Ying, X Ying, X Ying, T-K Lam, W-C Tang
and Y-L Wu, The Chinese U of Hong Kong, CN

1645 MAPPING INTO LUT STRUCTURES

A Mishchenko, S Ray, N Een and R Brayton,
UC Berkeley, US
S Jang and C Chen, Agate Logic Inc, US

1700 ROW-SHIFT DECOMPOSITIONS FOR INDEX GENERATION FUNCTIONS

T Sasao, Kyushu Institute of Technology, JP

1715 CUSTOM ON-CHIP SENSORS FOR POST-SILICON FAILING PATH ISOLATION IN THE PRESENCE OF PROCESS VARIATIONS

M Li and A Davoodi, Wisconsin - Madison U, US
L Xie, Cadence, US

1730 CLOSE

12.7 Impact of Modern Technology on Layout

Room - Konferenz 5 1600-1730

Moderators:

J Lienig, TU Dresden, DE

P Groeneveld, Magma Design Automation, US

Modern technology adds complexity to layout synthesis. The three contributions in this session are devoted to research in scavenging unused resources by redistributing wire segments, retargeting for yield, and robustness in carbon nanotube standard cells.

1600 ON EFFECTIVE FLIP-CHIP ROUTING VIA PSEUDO SINGLE REDISTRIBUTION LAYER

H-W Hsu, M-L Chen and H-M Chen, NCTU, TW
H Chen, Global UniChip, TW

1630 AIR (AERIAL IMAGE RETARGETING) : A NOVEL TECHNIQUE FOR IN-FAB AUTOMATIC MODEL-BASED RETARGETING-FOR-YIELD.

A Y Hamouda, Mentor Graphics and Waterloo U, CA
M Anis, The American U Cairo, EY
K S Karim, Waterloo U, CA

1700

LAYOUT-DRIVEN ROBUSTNESS ANALYSIS FOR MISALIGNED CARBON NANOTUBES IN CNTFET-BASED STANDARD CELLS

M Beste, Chair of Dependable Nano Computing, Karlsruhe Inst, DE
 M Tahoori, Karlsruhe Institute of Technology, DE

1730

CLOSE

12.8

EMBEDDED TUTORIAL - Advances in Variation-Aware Modelling, Verification and Testing of Analogue ICs

Room - Exhibition Theatre 1600-1730

Organiser:**T McConaghy**, Solido Design Automation, CA

This session describes novel approaches for variation-aware modelling, verification, fault simulation, and testing of analogue/custom ICs. The first speaker will present an approach for nonlinear, variation-aware behavioral modeling, via data mining and model-order reduction. The second speaker will present machine learning techniques to enable new industrial tools for fast, accurate PVT / statistical / high-sigma verification. The third speaker will describe an industrially-oriented approach to analog fault simulation that also applies to variation-aware design. The final speaker will present an analog test technique that addresses process variability and leverages adaptive test techniques.

1600

VARIATION-AWARE BEHAVIORAL MODELLING OF ANALOG CIRCUITS

D De Jonghe, G Gielen and E Maricau, K.U. Leuven, BE

1622

INDUSTRIAL VARIATION-AWARE DESIGN AND VERIFICATION OF CUSTOM ICS

T McConaghy, Solido Design Automation, CA

1644

FAST FAULT SIMULATION ALGORITHM FOR FAULT AND MONTE-CARLO SIMULATIONS

B Tasic, NXP, NL

1706

ADVANCES IN VARIATION-AWARE TESTING OF ANALOG ICS

H Stratigopoulos, TIMA Laboratory, FR

1730

CLOSE

friday workshops

DATE12

Dresden, Germany

12-16 March 2012

Co-Chairs:

Lorena Anghel, TIMA Laboratory, FR

Nicola Nicolici, McMaster University, CA

The DATE Friday's Workshops initiative was first introduced in 2003 and, since then, the workshops topics have diversified and the participation has increased to over 250 researchers and designers attending eight workshops at DATE 2011.

This initiative has now become an integral part of the conference, offering workshops on current and emerging important issues in design, test, EDA and software to complement the regular conference programme running throughout the week. They provide a unique opportunity for the various research and design communities to spend a day discussing the latest and the best, sharing their experiences and visions.

The Friday's programme for DATE 2012 includes nine workshop themes ranging from embedded systems to 3D integration. The broad embedded systems field, of growing interest to the DATE community, is covered by three workshops focused on embedded parallel computing platforms, cyber physical systems, and hardware/software considerations for improving energy efficiency in buildings. Two additional workshops are focused on methods for system-level design, in particular on virtual platforms and OS/CI/Accellera. Building on the success from the previous three years, the 3D integration workshop covers a broad spectrum of topics from technology and test to chip package and board co-design challenges. For attendees interested in the variability and dependability aspects in nano-scale circuits and systems, two workshops will discuss the lessons learned from large multi-institutional research programs. Finally, for the first time at DATE, the CANDE group of the IEEE Circuits and Systems Society will hold its yearly workshop to discuss new/emerging areas relevant to the electronic design automation community.

Friday's Workshops attendees should choose in advance one of W1, W2, W3, W4, W5, W6, W7, W8 or W9. The workshops run from 0815 until 1700. The individual timetables for each workshop may vary and for the detailed version of the workshop programmes, visit

<<http://www.date-conference.com/conference/friday-at-a-glance>>.

W1 Improving energy efficiency in buildings: from hardware to software aspects

Room – Seminar 1 0830 - 1600

Organisers:

Georges Gielen, Katholieke Universiteit Leuven, BE

Enrico Macii, Politecnico di Torino, IT

Description: Energy has become scarce and expensive. CO2 footprint is another major concern in the light of global warming.

FRIDAY

Buildings (including ICT infrastructure, lighting, heating, etc.) are among the largest energy consumers. This workshop focuses on smart techniques to improve energy efficiency in buildings. New solutions will be presented, as arising from recent European research projects like SEEMPubS, addressing both the hardware, middleware and software aspects. Smart control of appliances allows optimizing energy efficiency usage without compromising comfort or convenience. Sensor networks can provide the necessary measurement data. Service-oriented middleware for embedded systems create services and applications across heterogeneous devices to develop a real-time energy-aware platform. The workshop will highlight the most recent research results and will outline avenues for future research in this area.

The workshop program contains the following elements :

- Two invited keynote presentations
- Technical research presentations
- A panel session

For the detailed version of the program, please check :
<http://www.date-conference.com/conference/workshop-w1>

0830

SESSION 1

Moderator: Andrea Acquaviva, Politecnico di Torino, IT

Welcome address

0845

Keynote Presentation: Opportunities for energy savings in buildings

Davide Brunelli, University of Trento, IT

0930

The Seempubs project

Enrico Macii - Politecnico di Torino, IT

1000

Wireless sensor networks for smart and energy efficient public spaces

Edoardo Patti, Andrea Acquaviva, Francesco Abate, Enrico Macii, Politecnico di Torino, IT

1030

BREAK

1100

PR-UWB-based ultra-low-power sensor networks

Valentijn De Smedt, Wim Dehaene, Georges Gielen - Katholieke Universiteit Leuven, BE

1130

Exploiting occupancy information in context-aware energy-efficient buildings

Riccardo Tomasi, Istituto Superiore Mario Boella, IT

1200

LUNCH BREAK

1300

SESSION 2

Moderator : Georges Gielen - Katholieke Universiteit Leuven, BE

1315

Keynote Presentation: Smart plugs and energy savings in buildings

Francesco Gennaro - ST Microelectronics, IT

1400

Dynamic simulations for evaluating different strategies of an HVAC and lighting controller

J. Virgone, J. Savoyat, A. Pellegrino, L. Blaso,
G.V. Fracastoro, C. Aghemo,
UCBL and Politecnico di Torino, IT

1430

BREAK

1500

PANEL DISCUSSION**"Is ICT able to save energy ?"****Moderator:****Georges Gielen**, Katholieke Universiteit Leuven, BE**Panel members:****Enrico Macii** - Politecnico di Torino, IT**Riccardo Tomasi** - Istituto Superiore Mario Boella, IT**Francesco Gennaro** - ST Microelectronics, IT**Daide Brunelli**, University of Trento, IT

1600

CLOSE

W2

Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow

Room – Konferenz 1 0845 -1615

Organisers:**Rainer Leupers**, RWTH Aachen University, DE**Christian Haubelt**, University of Rostock, DE**Achim Rettberg**, Carl von Ossietzky University Oldenburg, DE**Kim Grüttner**, OFFIS – Institute for Information Technology, DE

Description: Nowadays, the deployment of Virtual Platform models is an industry-proven technique in a wide variety of design tasks from pre-silicon software development to performance analysis and exploration. With the increasing complexity, both in terms of the applications and the target platforms (e.g. increasing number of cores, more complex memory hierarchies), the Virtual Platform per se is not an answer to all of today's design challenges. But by adding further abstraction to the models, an increasing need for automated mapping, refinement, and model transformations is needed. Formal, static, and dynamic analysis methods are increasingly dependent on platform details, requiring traceability during all design phases.

This workshop aims to bring together developers, researchers, and managers from industry and academia to develop a perspective for the future use of Virtual Platforms by exchanging knowledge about current and future requirements and their possible solutions.

Questions to be addressed during the workshop are:

- How to efficiently generate a Virtual Platform for new applications and HW platforms?
- How to close the implementation/refinement gap?
- Which properties of a real system can be captured?
- What are the requirements for future Virtual Platforms?

FRIDAY

- How can Virtual Platforms support the development of future real-time applications for MPSoCs?

In this workshop, different points of view will be discussed by

- potential users of Virtual Platforms from different domains
- tool vendors already offering Virtual Platform tools and modeling techniques, and
- academic research institutes from around the world showing recent progress in Virtual Platform synthesis and core technologies

For the detailed version of the program, please check <http://qvvp12.offis.de>

0845

Welcome and Introduction

Rainer Leupers – RWTH Aachen University, DE

SESSION 1: System Synthesis – From System-Level Models to (Virtual) Platforms

0900

Recoding Embedded Applications into Flexible System-Level Models

Rainer Dömer – University of California, Irvine, US

0930

Actor-Based Virtual Prototype Generation

Jürgen Teich – University of Erlangen-Nuremberg, DE

1000

MPSoC Platforms for mobile devices: HW and SW development based on the Nucleus methodology

Torsten Kempf – RWTH Aachen University, DE

1030

Poster Session & coffee break

(list of poster can be found on the workshop's website)

SESSION 2: Virtual Platform Techniques – State of the Art and Beyond

1100

Scalable Transaction Level Modeling Methodology for Function, Communication, Timing and Power

Yossi Veller – Mentor Graphics, IL

1130

Task Modeling and HW/SW partitioning for System Performance Optimization

Tim Kogel – Synopsys, DE

1200

LUNCH BREAK

1300

HW/SW Verification from an Open SystemC virtual prototype through simulation, emulation, and FPGA prototyping

Leonard Drucker – Cadence, US

1330

High-Level Synthesis, TLM Power State Machines, and advanced tracing for Virtual Platforms

Philipp A. Hartmann – OFFIS –

Institute for Information Technology, DE

SESSION 3: Implementing Virtual Platforms on Multi Application Multi-Core Platforms

1400

Computation Architecture and Platform for Smart Grid Applications

Moritz Neukirchner – TU Braunschweig, DE

1430

Poster Session & coffee break

(list of posters can be found on the workshop's website)

1500

CoMPSoC: A Composable and Predictable Execution Platform

Kees Goossens – Eindhoven University of Technology (TU/e), NL

1530

Cross-Domain Reference Architecture for Embedded Systems

Roman Obermaisser – University of Siegen, DE

1600

Closing Remarks

Christian Haubelt – University of Rostock, DE

1615

CLOSE

W3

Fourth Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools and Applications

Room – Konferenz 2 0830 -1615

Organisers:**Cristina Silvano**, Politecnico di Milano, IT – General Co-Chair**Giovanni Agosta**, Politecnico di Milano, IT - General Co-Chair**João Cardoso**, Universidade do Porto, PT - General Co-Chair**Maurizio Palesi**, Kore University, IT - Architectures Posters Session Chair**Chantal Ykman-Couvreux**, IMEC, BE - Design Tools Posters Session Chair**Diana Göhringer**, Fraunhofer IOSB, DE - Applications Posters Session Chair**Jürgen Becker**, Karlsruhe Inst. of Technology, DE - Panel Session Co-Chair**Michael Hübner**, Karlsruhe Inst. of Technology, DE - Panel Session Co-Chair**Sotirios Xydis**, National Technical University of Athens, GR - Web Chair**Dimitris Mpekiaris**, National Technical University of Athens, GR -
Posters Submission Chair

Description: Embedded computing is shifting to multi/many-core designs to boost performance due to unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence, embedded system designers are increasingly faced with several big challenges, namely: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant design issues:

- How can applications that exploit the underlying (parallel) architecture be written without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the mapping process should/could be automated?

How should we design and optimize the underlying architectures?

FRIDAY

This workshop brings together researchers and practitioners actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

The workshop will have three main topic areas:

- **Architectures:** on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- **Design tools:** on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- **Applications:** on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

For the detailed version of the program, please check the Workshop web site:

<http://conferenze.dei.polimi.it/depcp/>

0830

Opening Session by General Co-Chairs

0845

Introduction to Poster Sessions:

0900

Session on: "Many-Core Architectures and Compilers" -

Invited Talk: "Platform 2012 Many-Core Programmable Accelerator: Status and Perspectives"

Eric Flamand/Diego Melpignano,
STMicroelectronics, Grenoble, France

0945

Invited Talk: "Compiler optimization techniques to help in automatically parallelize code"

Bilha Mendelson, IBM Research Lab in Haifa, Israel

1030

Architectures -- Posters Session - COFFEE BREAK (Posters program will be posted online)

1100

Panel on: "Designing and Programming Heterogenous Many-core Platforms: Challenges and Trends"

Panel Organizers and Moderators: Juergen Becker and Michael Huebner, Karlsruhe Inst. of Technology

1200

Lunch

1300

Session on "Design Tools and Applications for Many-Core Embedded Computing"

Invited Talk: "Rendering FPGAs to Multi-Core Embedded Computing --- Status, Results and Perspectives"

Pedro C. Diniz, INESC-ID, Lisboa, Portugal

1345

Invited Talk: "Dynamic Memory Management Techniques for Many-Core Architectures",

Dimitrios Soudris, National Technical University of Athens (NTUA), Athens, Greece.

1430

Design Tools -- Posters Session - COFFEE BREAK
(Posters program will be posted online)

1500

Invited Talk "Smart vision based components and applications for embedded computing platforms"
Volker Hahn, Fraunhofer-Institut, Darmstadt, Germany

1545

Applications -- Posters Session -
(Posters program will be posted online)

1615

Final Wrap up

Variability modelling and mitigation techniques in current and future technologies (VAMM)

Room – Konferenz 3 0815 - 1700

Organisers:

Antonio Rubio, Universitat Politècnica de Catalunya, ES

Martin Elhøj, Nangate, DK

Jan van Gerwen, NXP Semiconductors, NL

Description: The influence of process variations is becoming extremely critical for nanoCMOS technology nodes, due to geometric tolerances and manufacturing non-idealities (such as edge or surface roughness, or the fluctuation of the number of doping atoms). As a result, production yields and figures of merit of a circuit such as performance, power, and reliability have become extremely sensitive to uncontrollable statistical process variations. Although some kind of variability has always existed and been taken into account for designing integrated circuits, the largest impact of variability and the greater influence of random or spatial aspects are setting up a completely new challenge. On top of those difficulties, the deficiency of design techniques and EDA methodologies for tackling PVs makes that challenge even more critical. Variability has a huge economic impact in terms of yield loss or overdesign that is increasing with each technology generation. Without design countermeasures to reduce the impact of process variations, the cost advantage of technology scaling will be overrun by losses due to an increasing gap between designed and actual performances and therefore technology scaling will not be sustainable.

The objective of this Friday Workshop is to present advances in design or analysis techniques to counteract the problem of variability. Techniques range from the device level, to layout design, to architecture design. They include the use of redundancy, regularity and reconfiguration at different description levels.

The workshop program contains the following elements.

- Two invited keynote addresses
- Two invited talks
- Three interactive presentation sessions
- A panel session

The interactive presentation format consists in a short public presentation for each paper followed by a poster discussion.

FRIDAY

For the detailed version of the program including the list of selected papers, please check <http://www.synaptic-project.eu/vamm12>

0815

SESSION 1: OPENING

Welcome Address

0830

Keynote 1: "The Battle against Variability: the Designer Front"

Yves Laplanche, ARM Ltd., UK

0915

Keynote 2: "Variability in emerging technologies"

Asen Asenov, University of Glasgow, UK

1000

SESSION 2: SRAM Variability

Moderator: Antonio Rubio,
Universitat Politècnica de Catalunya, ES

Invited Talk: "SRAM scalability assessment in view of variability: a technology perspective"

Miguel Miranda Corbalan, IMEC, BE

1030

BREAK

1100

SESSION 3: Interactive presentations – Variability at device and layout levels

Moderator: Francesc Moll,
Univ. Politècnica de Catalunya, ES

1200

LUNCH

1300

SESSION 4: Subthreshold CMOS

Moderator: Jan van Gerwen, NXP Semiconductors, NL

Invited Talk: "Variability Effects in MOSFET's operating in Sub-threshold region"

Paolo Magnone, IUNET, U. Bologna, IT

1330

SESSION 5: Interactive Presentations – Variability at circuit level

Moderator: André Reis,
Univ. Federal do Rio Grande do Sul, BR

1430

BREAK

1500

SESSION 6: Interactive Presentations – Variability at architecture level

Moderator: Fabrizio Ferrandi, Politecnico di Milano, IT

1600

PANEL: A forward look on variability

Panelists:

Xavier Vera, Intel, ES

Davide Pandini, STMicroelectronics, IT

Nigel Woolaway, Leading Edge, IT

Martin Elhøj, Nangate, DK

Antonio Rubio, Univ. Politècnica de Catalunya, ES

1700

CLOSE

3D Integration – Applications, Technology, Architecture, Design, Automation, and Test

Room – Saal 5 0830 - 1640

Organisers:

Sandeep K. Goel, TSMC, US

Qiang Xu, The Chinese University of Hong Kong, HK

Saqib Khursheed, University of Southampton, UK

Description: 3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. But in order to produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges.

The last three editions of this workshop took place in conjunction with:

DATE 2009 (<http://www.date-conference.com/date09/conference/workshop-W5>),

DATE 2010 (<http://www.date-conference.com/date10/conference/workshop-W5>),

DATE 2011 (<http://www.date-conference.com/date11/conference/workshop-W5>).

The workshop program contains the following elements.

- One invited keynote address
- Two invited talks
- Two sessions with in total twelve regular presentations
- Two poster sessions
- One panel session

For the detailed version of the program, please see <http://www.date-conference.com/conference/session/W5>

0830

SESSION 1: OPENING

Moderator: Stephan Eggensglüß – German Research Center for Artificial Intelligence, DE

Welcome Address

0840

Keynote Address: Design of 3D Specific Systems: Prospective and Interface Requirements

Paul Franzon – North Carolina State U, US

0925

Invited Talk: 3D IC Test Challenges and Emerging Solutions

Steve Pateras – Mentor Graphics, US

1000

SESSION 2: POSTERS

Posters (see list on web) - coffee + tea break

1030

SESSION 3: Design, Automation and Test of 3D-ICs

Moderator: Andreas Hansson – ARM, UK

Fabrication Cost Analysis for 2D, 2.5D, and 3D IC Design

Chao Zhang, Guangyu Sun – Peking U, CN

1045

Performance and Efficiency of 3D Stacked DRAM in a Multicore SystemSachin Idgunji – ARM, US
Djordje Jevdjic – EFPL, CH
Dragomir Milojevic – IMEC, BE
Emre Ozer – ARM, US

1100

Designing a 3D Stacked Vector CacheRyusuke Egawa – Tohoku U/JST CREST, JP
Yusuke Endo – Tohoku U, JP
Jubei Tada – Yamagata U, JP
Hiroyuki Takizawa, Hiroaki Kobayashi –
Tohoku U/JST CREST, JP
Gensuke Goto – Yamagata U, JP

1115

Quality Inspection Strategy in 3D-Chip Formation ProcessWolfram Steller, Stephan Dobritz, Juliane Krause –
Fraunhofer IZM – ASSID, DE

1130

TSV Cost Aware Circuit Partitioning for 3D-SOCsAmit Kumar, Sudhakar Reddy – U of Iowa, US
Irith Pomeranz – Purdue U, US
Bernd Becker – Albert-Ludwigs-U, DE

1145

Dynamic Thermal Optimization for 3D NOCRa'ed Al-Dujaily, Terrence Mak, Fei Xia, Alex Yakovlev –
Newcastle U, UK
Kai-Pui Lam, The Chinese U of Hong Kong, HK
Chi-Sang Poon,
Massachusetts Institute of Technology, US

1200

LUNCH BREAK

1300

SESSION 4: Efficient 3D System-in-Package: Reliability, Failure Analysis and Test (ESiP)

Moderator: U. Ingelsson, EIS by Semcon AB, SE

System-in-Package: Need for a Coherent Chip-Package-Board View

Klaus Pressel – Infineon, DE

1315

Adapting WLP technologies for packaging of MEMS-SiP

Heikki Kuisma and Sami Nurmi – VTI, FI

1330

Failure analysis of open TSV interconnectsFrank Altmann – Fraunhofer Institute
for Mechanics of Materials IWM, DE
Franz Schrank – austriamicrosystems AG, AT

1345

Defect analysis in wafer bonded interfaces for 3D integration

Matthias Petzold – Fraunhofer Institute for Mechanics of Materials IWM, DE
Cathal Cassidy – austriamicrosystems AG, AT

1400

Aspects of probing fine pitch structures in 3D using dedicated probe tools

Thomas Thaerigen – Cascade Microtech, DE
Peter Hanaway – Cascade Microtech, US
Stojan Kanev – Cascade Microtech, DE
Erik Jan Marinissen – IMEC, BE

1415

Contact-less testing platform based on capacitive coupling: I/O pad and probe-card design considerations

Roberto Canegallo – ST Microelectronics, IT
Eleonora Franchi – U of Bologna, IT
Cristian Gozzi – Technoprobe, IT
Andrea Santomartino – SPEA, IT

1430

SESSION 5: POSTERS

Posters (see list on web) – coffee + tea break

1500

SESSION 6: INVITED TALK

Moderator: Erik Jan Marinissen, IMEC, BE

“Design, Implementation, and Test of 3D-MAPS – a Many-Core Processor Using 3-D Integration Technology”

Hsien-Hsin S. Lee – Georgia Tech., US

1540

SESSION 7: PANEL DISCUSSION**“Chip package and board co-design challenges and solution for 3D ICs”**

Moderator: Jochen Reisinger – Infineon, AT

Panellists:

Peter Schneider – Fraunhofer IIS – EAS, DE
Rainer Kress – Infineon, DE
Keith Felton – Cadence, US
Martin Schrems, austriamicrosystems, AT
Ridha Hamza, DOCEA Power, F

1640

CLOSE

W6

European SystemC User's Group Workshop: OSCI and Accellera Core Technologies for the Next Generation of System-Level Design

Room – Konferenz 4 0830 - 1650

Organiser:

Axel Braun, European SystemC User's Group/University of Tübingen, DE

FRIDAY

Description: The merger of the Open SystemC Initiative (OSCI) and Accellera to the Accellera Systems Initiative (ASI) unifies trend-setting standardization activities in the Electronic Design Automation (EDA) world and opens a wide range of new perspectives and synergies. The standards that are established and promoted by OSCI and Accellera cover a broad spectrum of today's and tomorrow's Electronic System Level (ESL) modeling and verification strategies.

This workshop is focused on the core technologies from both the OSCI and the Accellera world, and gives an outlook on how techniques may collaborate and converge. The format of the workshop includes four invited sessions from Doulos, Synopsys, Cadence, and ARM—providing a substantiated overview of the technologies and their future way—providing a practical guide on how those technologies can be successfully applied for improving a companies' design strategy. Five user sections from XMOS, Sonics and Lantiq, the University of Bremen, Bosch, and the Worcester Polytechnic Institute complement these core sections. They provide insights into the application and the development in research and industrial domains.

For a detailed version of the program, please check:
<http://www.date-conference.com/conference/session/W6>

0830

Welcome & Opening

Wolfgang Rosenstiel,
Tuebingen U and edacentrum, DE

0840

Core Section 1: Doulos IEEE 1666-2011 SystemC Standard

John Aynsley, Doulos, U.K.

0940

User Section 1: Using SystemC with XMOS Devices

David Lacey, XMOS, U.K.

1010

Coffee Break

1030

Core Section 2: Synopsys TLM-2.0 Technology for Off-Chip Interfaces

Victor Reyes, Synopsys, US

1130

User Section 2: SoC performance evaluation using high performance SystemQ and TLM models for communications SoCs

Rocco Jonack, Sonics, US Bernhard Keppler, Lantiq, DE Renate Henftling, Lantiq, DE

1200

Lunch Break

1300

Core Section 3: Cadence Virtual Prototypes for Embedded Software Verification

Markus Winterholer, Cadence, DE,
Leonard Drucker, Cadence, US

1400

User Section 3: SystemC-based ESL Verification Flow Integrating Property Checking and Automatic Debugging

Hoang M. Le, Daniel Große, Rolf Drechsler,
University of Bremen and DFKI, DE

1430

Coffee Break

1450

Core Section 4: ARM Virtual Platforms and Programmer's View Models for Software Development

Robert Kaye, ARM, U.K.

1550

User Section 4: Using IP-XACT to ease system development with SystemC/TLM The Transparent TLM (TTLM) Approach

Simon Hufnagel, Bosch, DE, Christoph Grimm, Vienna University of Technology, AT

1620

User Section 5: System-Level Post-Manufacturing Testing

Zainalabedin Navabi, Worcester Polytechnic Institute, US

1650

Closing

Wolfgang Rosenstiel, Tuebingen U and edacentrum, DE



Facing dependability challenges at nanoscale: from devices to systems

Room – Konferenz 5 0830 - 1645

Organisers:**Mehdi Tahoori**, Karlsruhe Institute of Technology**Joerg Henkel**, Karlsruhe Institute of Technology**Andreas Herkersdorf**, Technical University of Munich**Wolfgang Rosenstiel**, Tuebingen U and edacentrum**Oliver Bringmann**, FZI Karlsruhe**Norbert Wehn**, University of Kaiserslautern**Sani Nassif**, IBM

Description: Improvements in chip manufacturing technology have propelled an astonishing growth of embedded systems which are integrated into our daily lives. However, this trend is facing serious challenges, both at device and system levels. As the minimum feature size continues to shrink, a host of vulnerabilities influence the robustness, reliability, and availability of embedded and critical systems. Some of these factors are caused by the stochastic nature of the nanoscale manufacturing process (e.g., process variability, sub-wavelength lithographic inaccuracies), while other factors appear because of high frequencies and nanoscale features (e.g. RLC noise, on-chip temperature variation, increased sensitivity to radiation and transistor aging).

The objective of this workshop is to bring the attention of design automation community to the multi-level reliability challenges and solutions and possible paradigm shift to consider reliability throughout the design flow, from devices to systems and applications. In addition, this workshop tries to introduce and promote various existing coordinated research programs on dependability which are currently underway in Europe, Asia, and USA to deal with multi-level reliability challenges. We plan to review the overlap and synergy among these programs in order to explore how they can complement each other. The goal is to have further collaborations among these programs such that the overall design and test automation community can benefit more from the outcomes of these programs.

FRIDAY

0830

Session 1: OPENING

Welcome Address

Mehdi Tahoori, KIT, DE

0845

Keynote Address - Why Resilience Matters

Sani Nassif, IBM Research, Austin, US

0930

Session 2: COORDINATED DEPENDABILITY PROGRAMS - PART I

German Research Foundation (DFG) priority program on "Dependable Embedded Systems"

Joerg Henkel, KIT, DE

1000

Japan Science and Technology Agency (JST) program on "Dependable VLSI platform Project"

Hidetoshi Onodera, Kyoto U, JP

1030

Break

1100

Session 3: COORDINATED DEPENDABILITY PROGRAMS - PART II

US National Science Foundation (NSF) program on "Variability Expeditions"

Nikil Dutt, UCI, US

1130

EU COST Action on "Manufacturable and Dependable Multicore Architectures at Nanoscale"

Marco Ottavi, U Roma, IT

1200

Lunch Break

1300

Session 4: DEVICE, CIRCUIT, AND ARCHITECTURE RELIABILITY

Device reliability: The never-ending challenge

Christian Schluender, Infineon, DE

1330

Design efforts and time zero screening methods to ensure high end processor reliability

Dieter Wendel, IBM, DE

1400

Workload Dependencies of Aging Effects

Rob Aitken, ARM, US

1430

Coffee Break + Poster Session

1500

Session 5: SYSTEM AND APPLICATION DEPENDABILITY

Error Resilience in Wireless Communication Systems

Norbert Wehn, U Kaiserslautern, DE

1530

Dependability issues in automotive electronics

Werner Kanert, Infineon Technologies, DE

1600

Session 6: PANEL DISCUSSION**An inter-continental approach to solve dependability challenges****Panelists:**

Nikil Dutt, UCI, US
 Joerg Henkel, KIT, DE
 Sani Nassif, IBM, US
 Hidetoshi Onodera, Kyoto U, JP
 Marco Ottavi, U Roma, IT

1645

Concluding Remarks

Computer Aided NETWORK Design (CANDE) Workshop 2012

Room – Konferenz 6 0835 - 1645

Organisers:

Priyank Kalla, University of Utah, US
Farinaz Koushanfar, Rice University, US
Gi-Joon Nam, IBM, US
Deming Chen, University of Illinois, US
Azadeh Davoodi, University of Wisconsin, US
Subhasish Mitra, Stanford University, US

CANDE (Computer-Aided Network Design) is a technical committee of the IEEE Circuits and Systems Society and a member of the IEEE Council on Electronic Design Automation. It acts as a working group for electronic computer-aided design. CANDE holds a yearly workshop to discuss advanced issues relevant to the CAD community, bringing together practitioners, researchers, and managers from industry and academia.

CANDE community members actively participate in identifying topics in new/emerging areas where Design Automation may find potential application, and also on contemporary topics where EDA needs to be improved. The workshop is a working meeting where informal and open discussions are encouraged, and no proceedings are published. Attendance is open to all EDA/CAD professionals. For more information on CANDE, visit: www.cande.net. For program updates and details, please visit <http://www.date-conference.com/conference/workshop-w8>

Workshop Program: Talks are 35 mins long, (approx. 25+ mins talk and 10- mins Q & A). Keynote talks ~55 mins. (45 + 10 min Q + A).

0835

Opening Remarks & Intro to CANDE

0845

Session I: Topic area: System Design and Verification

“25 Years Digital Design Mainstream using RTL Synthesis – Will there be additional 25 Years?”
 Speaker: Wolfgang Ecker, Infineon, DE

0920

“Is P = NP in the Cloud – Are we Designing the Right Verification Algorithms?”

Speaker: Rolf Drechsler, University of Bremen, DE

FRIDAY

0945

Session II: Automotive Systems: Can EDA Help, or Not?

0955

“Is there Life Beyond the Chip Borders? An Automotive System Perspective”

Speaker: Georg Pelz, Infineon, DE

1030

Break

1100

Session III: Keynote Talk I

“System-Level Design: What are the Roadblocks and Opportunities?”

Speaker: Alberto Sangiovanni Vincentelli, University of California, Berkeley, US

1155

Lunch Break

1300

Session IV: Keynote Talk II

Aging in the Age of CMOS

Speaker: Sachin Sapatnekar, University of Minnesota, US

Session V: Next Generation Lithography Techniques: Are you ready?

1355

“Double Patterning: The Good, The Bad and the Ugly: An EDA Perspective Techniques”

Speaker: J Andres Torres, Mentor Graphics, US

1430

Break

1500

Session V Contd.

“Lithograph Challenges and the Impact on Design-Flow under 22nm Technology Node”

Speaker: Gi-Joon Nam, IBM, US

1535

Session VI: Embedded Systems

“Dependable Embedded Software for Undependable Hardware”

Speaker: Jörg Henkel, Karlsruhe Institute of Technology, DE

1610

“Requirements and Tools for Embedded Platform Mapping in Communication Systems”

Praveen Raghavan, IMEC, BE

1645

CLOSE

W9

Cyber Physical Systems (CPS) for Smart Mobility: Design, Architectures and Applications

Room – Seminar 3 0830 - 1700

Organisers:

Jürgen Becker, Karlsruhe Institute of Technology - KIT, DE

Manfred Broy, Technical University of Munich, TUM, DE

The term Cyber Physical Systems (CPS) is used to describe software-intensive embedded systems that are connected to services available around the world through global networks such as the Internet, as parts of devices, buildings, vehicles, routes, production plants, logistics and management processes etc. that use sensors and actuators to gather physical data directly and to directly affect physical processes. This includes the real-time connectivity to digital networks (wireless, wired, local, global) using globally available data and services. Such systems can be found in all smart mobility domains like automotive, avionics, and railway. Moreover Cyber Physical Systems will be the basis for smart mobility comprising the characteristics intermodality, efficiency, safety, mixed criticality and the like.

Multicore and (heterogenous incl. reconfigurable hardware etc.) are a promising solutions to provide the sufficient performance/power ratios.

The purpose of this workshop is to evaluate strategies for future system design for hardware architectures, design tools and methods and applications, especially facing the challenges of CPS in the automotive and avionics application domains.

The workshop program contains the following elements.

One invited keynote address

Three sessions with in total eleven regular presentations

For the detailed version of the program, please check

<http://www.date-conference.com/conference/workshop-w9>

0830

SESSION 1: OPENING

Moderator: Jürgen Becker - KIT, DE
and Manfred Broy – TUM, DE

0900

Welcome Address

Keynote Address:
Cyber-Physical Systems and Beyond: the Future is in our Minds
Alberto Sangiovanni-Vincentelli, UC Berkeley, US

1000

CPS in Wireless Sensor Networks

Magdy Bayoumi, Louisiana State University - Lafayette, US

1030

BREAK

1100

SESSION 1: CYBER PHYSICAL SYSTEMS FOR SMART MOBILITY

Moderator: Michael Hübner,
Karlsruhe Institute of Technology – KIT

FRIDAY

1100

CPS for the Automotive Domain

Andreas Herkersdorf,
Technical University of Munich – TUM, DE

1130

Smart Environments enabling Smart Mobility

Jürgen Hairbucher, Director Intel Lab Munich, DE

1200

LUNCH BREAK

1300

SESSION 2: CPS SOLUTIONS IN AUTOMOTIVE AND AVIONICS

Moderator: Andreas Herkersdorf,
Technical University of Munich – TUM, DE

Dependable CPS Systems in the Avionic Domain

Heinrich Daembkes, Ottmar Bender, Cassidian - Ulm, DE

1330

Multicore and Virtualization – Enabler for an future oriented electronics architecture in Automotive?

Hans-Ulrich Michel, BMW Forschung und Technik GmbH - Munich, DE

1400

Multicores as Enablers for Future Automotive E/E-Architectures

Hermann von Hasseln, Daimler, DE

1430

BREAK

1500

SESSION 3: SECURITY AND TOOLS

Moderator: Oliver Sander,
Karlsruhe Institute of Technology – KIT, DE

Security for Cyber Physical Systems

Ingrid Verbauwhede, KU Leuven, BE

1530

Security for Automotive with Multicore-based Embedded Systems

Claudia Eckert, FhG Institute AISEC - Munich, DE

1600

Skylab-based High Level Design Flow for Low Power CPS

Nikos Voros, University of Mesologhi, GR

1630

FLEXIBLES : Self adaptive heterogeneous manycore based on Flexible Tiles

Fabrice Lemonnier, THALES Research & Technology - STI Group, FR

1700

CLOSE

FRINGE MEETINGS

fringe technical meetings

A number of specialist interest groups will be holding their meetings at DATE. Currently, the following meetings are scheduled but a full list of fringe meetings with description of content will be found on the DATE web portal – www.date-conference.com

Day	Time	Meeting & Contact	Room	Type
Mon	1900-2100	EDAA PhD Forum Peter Marwedel <peter.marwedel@tu-dortmund.de>	Terrasse	Open
Tues	1830-1930	EDAA General Assembly Norbert Wehn <wehn@eit.uni-kl.de>	Seminar 4	Open
Tues	1830-2000	ETTTC Meeting Matteo Sonza Reorda <matteo.sonzareorda@polito.it>	Konferenz 3	Open
Tues	1830-2045	IEEE P1076.1 Working Group on VHDL-AMS Ernst Christen <christen.1858@comcast.net>	Konferenz 4	Open
Tues	1830-2100	SystemC User's Group Axel Braun <axel.braun@informatik.uni-tuebingen.de>	Konferenz 2	Open
Thurs	0900-1800	ArtistDesign European NoE: Showcase of the Main Results Bruno Bouyssounouse <Bruno.Bouyssounouse@imag.fr>	Seminar 1	Open

PhD FORUM

PhD forum

Monday: Room – Terrasse – 1900-2100

Organiser:

Peter Marwedel, TU Dortmund, DE

The EDAA/ACM PhD Forum at the Design, Automation and Test in Europe (DATE) Conference is a poster session and a buffet dinner organised and hosted by ACM SIGDA and the European Design and Automation Association (EDAA). The EDAA Best Dissertation Awards will be presented during the Wednesday lunch-time keynote session.

The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work. More information is available on the web – www.date-conference.com

UNIVERSITY BOOTH

university booth demonstrations

DATE 12 will feature the University Booth where system and VLSI CAD tools developed in Universities and Research Institutes are demonstrated as well as circuits in their working environment. This provides an alternative and more direct way of communicating CAD research results and displaying working silicon to the interested specialists. The University Booth will be located in the Exhibition Hall and will be furnished with popular workstations. A rotating schedule will operate throughout the three days.

Contacts: Jens Lienig <jens@ieee.org>
Andreas Voerg <voerg@edacentrum.de>

EXHIBITION THEATRE

exhibition programme

This is a programme of free events open to all attendees at DATE 12 in the Exhibition Theatre

exhibition theatre

Chair:

Juergen Haase, edacentrum, DE

In addition to the conference programme during DATE 12, there will be a presentation theatre from Tuesday 13 March to Thursday 15 March 2012. Attendees will profit from having an industry forum in the midst of Europe's leading electronic systems design event. The theatre is located on the show floor to thus afford for conference delegates during the morning, lunchtime and afternoon exhibition breaks.

For the fourth time, open Special Conference Sessions from Track 8 (full details are contained in the main conference programme pages) will take place in the Exhibition Theatre. These sessions are open to conference delegates as well as to exhibition visitors and are as follows:

2.8	Embedded Tutorial Beyond CMOS - Benchmarking for Future Technologies	Tuesday 1130-1300
3.8	Hot Topic Design Automation Tools for Engineering Biological Systems	Tuesday 1430-1545
7.8	Hot Topic New Directions in Timing Modeling and Analysis of Automotive Software	Wednesday 1430-1600
8.8	Embedded Tutorial Batteries and Battery Management Systems	Wednesday 1700-1830
10.8	Embedded Tutorial Moore meets Maxwell	Thursday 1100-1230
11.8	Hot Topic Programmability and Performance Portability Aspects of Heterogeneous Multi-/Manycore Systems	Thursday 1400-1530
12.8	Hot Topic Advances in Variation-Aware Modelling, Verification, and Testing of Analog ICs	Thursday 1600-1730

Additionally there will be many testimonials providing valuable experience on recent results of leading companies in application of advanced design methodologies and of new tools.

Please see presented overleaf information on confirmed first-class panels and a first-class keynote as highlights of the Exhibition Theatre Programme. the full programme containign details of all other exhibition session slots is available on the DATE web portal and in the Event Guide.

Panel Session - Exhibition Theatre

Tuesday March 13, 1700 - 1830

Modeling and Simulation Challenges in Automotive Electric System Design

- Organiser:** Joachim Haase, Fraunhofer IIS/EAS Dresden, DE
- Moderator:** Dirk Friebel, Dirk W. Friebel Interim Management, US
- Panellists:** Ewald Hessel, Hella KGaA Hueck & Co Lippstadt, DE
Karsten Einwich, Fraunhofer IIS/EAS Dresden, DE
Joachim Haase, Fraunhofer IIS/EAS Dresden, DE
Olaf Hädrich, ANSYS Germany GmbH, DE

Abstract: Electronic and electrical systems in automobiles become more and more complex. This has been a development for many years that has been supported by better tools and approaches for the design of components. Handling the growing complexity during the integration of the components in the car is one of the challenges that become more and more important. Investigation of interactions between analog circuits, digital hardware, ECU software, mechanics, and car environment in different time-scales and the detection of critical situations at a very early stage saves time and costs. The session at the exhibition theatre will start with a presentation of the spokesman of the Working group AK30 "Mixed simulation with VHDL-AMS" of the German Association for Research in Automobile Technology (FAT) within the Association of the Automotive Industry (VDA). Ewald Hessel will present experiences and requirements concerning the electric system design in the automotive industries. Technical as well as organizational requirements resulting from the different players as OEM, TIER-1, and TIER-2 and their different tool environments will be touched. The subsequent presentations will focus on special items in this context. New ideas and achievements applying SystemC AMS for real-time modeling and Hardware-In-the-Loop simulation will be demonstrated by ongoing design examples. Opportunities and constraints of model exchange and model exchange requirements based on the Hardware Description Language VHDL-AMS will be figured out afterwards. The session will be concluded by a contribution that shows options and expectations of an EDA vendor that is active in the area. Last but not least, the audience is expected to promote the activities in this area by their feedback.

DATE12

Dresden, Germany

12-16 March 2012

Panel Session - Exhibition Theatre

Wednesday March 14, 1100 - 1230

Foundry Design Practices

- Organiser/
Moderator:** Gerd Teepe, GLOBALFOUNDRIES, DE
- Panellists:** Rob Aitken, ARM, UK
Christoph Heer, Intel Mobile Communications, DE
Christian Malter, Cadence, DE
Ronald Niederhagen, Synopsys, DE
Jörg Winkler, GLOBALFOUNDRIES, DE

Abstract: IC Design has evolved over time along the accelerating EDA-roadmap. As the primary driver, the number of transistors monolithically integrated into an IC follows Moore's Law of exponential complexity increase.

A secondary driver is of equal impact to the design complexity: as technologies are increasingly complex to manufacture and Design-Manuals describing the technologies grow thicker, the Semiconductor Industry is transferring process complexity into the design-space. As these two drivers of EDA-complexity superimpose, the need for powerful EDA-tools is imminent and necessitates deeper and more intense cooperation between the partners of the design ecosystem. Designing ICs for foundry manufacturing requires specific design practices for successful product developments, which are timely and economic and meet the quality requirements set forth. On this panel, among others, the focus topics will be to look at the economic boundary conditions, the design enablement requirements, the role of 3rd party IP, as well as design services. IP-handling issues and Quality will be covered as well.

Exhibition Keynote - Exhibition Theatre

Thursday March 15, 1330 - 1400

Key Success Factors 2012 for Design

**Organiser/
Moderator:** Jürgen Haase, edacentrum, DE

Speaker: Andreas Brüning, Silicon Saxony/ZMDI, DE

Abstract: What issues, technologies and trends are important in 2012? Where is the development of innovative products and solutions? Companies and engineers need to respond flexibly to market conditions and adapt their skills. Listen to the identified trends and recommendations ...In 2012 the growth will continue across all industries. But the clouds on the horizon are identified, and the many self-appointed prophets will reinforce this trend. Therefore the requirements for efficiency and competitiveness in product development are growing. Companies invest in growth through innovation by developing new products and solutions. At the same time they are aware of the volatile market situation and thus provide their development teams worldwide as lean and efficiently as possible. Many industries are changing very quickly and solid. Software and IT are the main drivers of innovation. Software-intensive systems as used in automobiles, aircraft, medical, transportation, utility and industrial technology will deliver today 50-70 percent of the value of these systems. The products and solutions to meet increasing quality requirements, but also develop cost-efficiently, can be easily adapted and effectively exploit the advantages of modern platforms. At the same time constantly pushing new competitors with new solutions on the market and the technology landscape is increasingly cluttered. Companies that have stagnated in this period of change and growth will fall behind. Fast, effective and yet flexible to operate in 2012 is therefore a clear priority for development teams and business units. However, the executives are unsure whether the measures taken are sustainable enough, and how the rising pressure for innovation can be managed. They are expecting proposals from product development about reducing short-term costs as well as about setting the right priorities for new developments.

vendor exhibition

DATE 12 Exhibitors and Sponsors include:

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Test Generation, Simulation and Diagnosis

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Test for Mixed-Signal, Analog, RF, MEMS

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Awards Ceremony	26, 55
DATE At A Glance	12-16
DATE Executive Committee	115
DATE Party	6
e-Mobility Special Day	8
Event Overview	11
Executive Sessions	7
Exhibition Theatre	112
Friday Workshops	93
Fringe Meetings	111
General Information	6
Interactive Presentations	6
Keynote Addresses	4, 5
More than Moore Special Day	9
PhD Forum	111
Plenary Session	4
Programme Guide	2
Secretariat Contact	11
Site Plan	120
Special Sessions	10
Sponsors	119
Technical Programme	26-92
Tutorials	17
University Booth Demonstrations	111
Vendor Exhibition	115
Venue	6
Welcome	3

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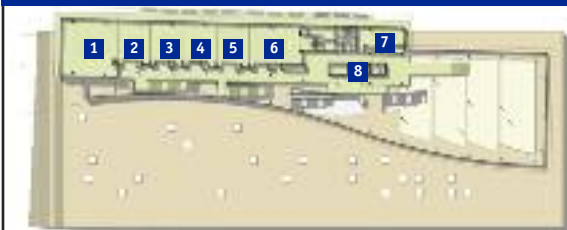
IEEE Solid-State Circuits Society (SSCS)

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Conference level



1 - 6 Conference Rooms **7** AV HQ/Practice **8** Press Lounge

Seminar level



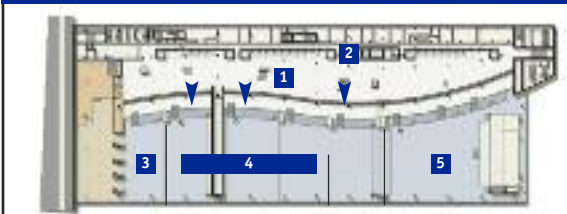
1 - 7 Seminar/Meeting Rooms

Terrace level



1 Main Entrance **2** Registration/Bags **3** Speakers' Breakfast/Delegate Lunch

Ground (Saal) floor



1 IP Sessions **2** Cloaks **3** Conference Room (Saal 5)
4 Exhibition/Exhibition Theatre/Delegate Coffee
5 Opening Session (Tues)/DATE Party (Wed)