event guide

EVENT GUIDE

DATE 11

Alpes Congrès, Grenoble, France
March 14 - 18, 2011

Design, Automation & Test in Europe




The European System Design Show

From Systems-on-Chip to Embedded Computing

www.date-conference.com

WWW.DATE-CONFERENCE.COM

Welcome to DATE 11

In this exhibition guide you will find listings of exhibitors contact details and their products being demonstrated on the exhibition floor. The classified product finder will help you locate the right solution within the show; maps and plans of Alpexpo, exhibition hall and additional exhibition space will also help you to get around.

FREE - ENTRY to KEYNOTE SESSIONS & EXHIBITION THEATRE (see p.8) & SPECIAL EVENTS!

OPENING PLENARY KEYNOTES –

0830-1030, Tuesday 15 March, Auditorium Dauphine

Biologically-inspired massively-parallel architectures– computing beyond a million processors

S Furber, ICL Professor of Computer Engineering,School of Computer Science, Manchester U, United Kingdom

How technology R&D leadership brings a competitive advantage in the fields of multimedia convergence and power applications

Philippe Magarshack, Group Vice-President, Technology R&D - General Manager, Central CAD and Design Solutions, STMicroelectronics, France

LUNCH AND LEARN SESSION SPONSORED BY MENTOR GRAPHICS

1300-1400, Tuesday 15 March, Auditorium Dauphine

Grenoble EDA Ecosystem - From Research to Market

SPECIAL DAY KEYNOTE - WIRELESS INNOVATIONS FOR SMARTPHONES

1400-1430, Wednesday 16 March, Room Oisans

Hannu Kauppinen, Director, Head of Radio Systems Laboratory, Nokia Research Center, Finland

SPECIAL DAY KEYNOTE - SMART ENERGY AT ST

1330-1400, Thursday 17 March, Room Oisans

Carmelo Papa, Executive VP Industrial and Multisegment, STMicroelectronics, Italy

CONTENTS contents

Exhibition Opening Times:

Tuesday 15 March
1000 - 1830*
(*Evening Reception offered by the City of Grenoble from 1830 – 1930hrs)

Wednesday 16 March
1000 - 1800

Thursday 17 March
1000 - 1700

Entrance to the Exhibition is FREE

DATE Event Secretariat
European Conferences
3 Coates Place
Edinburgh EH3 7AA, UK

T: +44 (0)131 225 2892
E: sue.menzies@ec.u-net.com or
E: claire.cartwright@ec.u-net.com
W: www.date-conference.com

tuesday 15 march

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1030-1130 Exhibition Break, 1300-1430 Lunch, 1600-1700 Exhibition Break (1600-1630 IP1)
0830	1.1 PLENARY: OPENING, KEYNOTE ADDRESSES AND AWARDS PRESENTATION, Auditorium Dauphine		

	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1130 to 1300	2.1 EXECUTIVE SESSION – Ideas on Future of EDA and IP Industry	2.2 System-Level Techniques to Handle Performance, Reliability and Thermal Issues	2.3 Modelling and Simulation of Interconnects	2.4 PANEL AND EMBEDDED TUTORIAL SESSION – Logic Synthesis and Place and Route: After 20 Years of Engagement, Wedding in View	2.5 Transient Faults and Soft Errors	2.6 Networked Embedded Systems	2.7 Design of Energy-Efficient and Automotive Systems	2.8 EMBEDDED TUTORIAL – Addressing Critical Power Management Verification Issues in Low Power Designs
1400	3.0 SPECIAL LUNCH-TIME SESSION 1300-1400 Grenoble EDA Ecosystem Session - From Research to Market sponsored by Mentor Graphics, Auditorium Dauphine							
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1430 to 1600	3.1 EXECUTIVE SESSION – 22nm Challenges and Wealth/Knowledge Creation Opportunities	3.2 Power Optimisation of Multi-Core Architectures	3.3 Core Algorithms for Formal Verification Engines	3.4 Predicting Bugs and Generating Tests for Validation	3.5 Timing Related Issues in Test	3.6 Performance and Timing Analysis	3.7 Implementations for Digital Baseband Processing	3.8 PANEL SESSION – Power Formats: Beyond UPF and CPF
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1700 to 1830	4.1 EXECUTIVE SESSION – System Level Complexity and Innovation	4.2 Robust and Low Power Systems	4.3 Formal Verification Techniques and Applications	4.4 System Level Simulation and Validation	4.5 Advances in Analogue, Mixed Signal and RF Testing	4.6 Design Automation Methodologies and Architectures for Three-Dimensional ICs	4.7 Resource Management for QoS Guaranteed NoCs	SEE WEB OR EVENT GUIDE FOR LATEST EXHIBITION PROGRAMME
1830	Evening Reception Offered by the City of Grenoble							

wednesday 16 march

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP2), 1230-1340 Lunch, 1600-1700 Exhibition Break (1600-1630 IP3)

	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
0830 to 1000	5.1 SMART DEVICES EMBEDDED TUTORIAL –Smart Devices for the Cloud Era	5.2 An Encyclopedia of Routing	5.3 Temperature and Variation Aware Design in Low Power Systems	5.4 Advanced NoC Tooling and Architectures	5.5 INDUSTRIAL 1	5.6 Analysis, Compilation and Runtime Techniques	5.7 EMBEDDED TUTORIAL – Architectures for Online Error Detection and Recovery in Multicore Processors	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1100 to 1230	6.1.1 SMART DEVICES HOT TOPIC/EMBEDDED TUTORIAL – Ultra Low Power Smart Devices	6.2 Placement and Floorplanning	6.3 Power Modelling, Analysis and Optimisation	6.4 Design and Test of Fault Resilient NoC Architectures	6.5 New Techniques for Diagnosis and Debug	6.6 Embedded Software for Parallel Architectures	6.7 HOT TOPIC – Virtual Manycore Platforms: Moving Towards 100+ Processor Cores	6.8 PANEL SESSION – Embedded Software Debug and Test
1340	6.1.2 SPECIAL DAY KEYNOTE AND AWARDS 1340-1400 Awards and 1400-1430 Keynote, Room – Oisans							
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1430 to 1600	7.1 SMART DEVICES HOT TOPIC – Smart Medical Implants	7.2 Emerging Memory Technologies	7.3 Architectural Optimisation for Low Power Systems	7.4 Advanced Technologies for NoC Implementation	7.5 Emerging Test Solutions for Advanced Technologies, RF and MEMS Devices	7.6 Innovative Power-Aware Systems for a Green and Healthy Society	7.7 HOT TOPIC – Foundations of Component-Based Design for Embedded Systems	7.8 EMBEDDED TUTORIAL – Predictable System Integration
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1700 to 1830	8.1 SMART DEVICES PANEL SESSION – Integrating the Real World Interfaces	8.2 System-Level Design Techniques for Automotive Systems	8.3 Power/Error Tradeoffs	8.4 Memory System Architectures	8.5 Testing and Designing SRAM Memories	8.6 Cryptanalysis, Attacks and Countermeasures	8.7 HOT TOPIC – Flows, Application and Future of Component-based Design for Embedded Systems	8.8 EMBEDDED TUTORIAL – Communication Networks in Next Generation Automobiles

thursday 17 march

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP4), 1230-1330 Lunch, 1530-1600 Break (1530-1600 IP5)

	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
0830 to 1000	9.1 INTELLIGENT ENERGY MANAGEMENT TUTORIAL – Energy Transfer, Generation and Power Electronics	9.2 Design Automation Methodologies for Emerging Technologies	9.3 System Modelling	9.4 Modelling and Verification of Analogue and RF Circuits	9.5 INDUSTRIAL 2	9.6 Embedded System Resource Allocation and Management	9.7 EMBEDDED TUTORIAL – Sub-Wave Length Lithography and Variability Aware Test and Characterisation Methods	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1100 to 1230	10.1.1 INTELLIGENT ENERGY MANAGEMENT – Smart Energy Generation: Design Automation and the Smart-Grid	10.2 Advanced Algorithms and Applications for Reconfigurable Computing	10.3 System Optimisations and Adaptivity	10.4 Design and Simulation of Mixed-Signal Systems	10.5 Advances in Test Generation and Fault Simulation	10.6 Model Based Verification and Synthesis of Embedded Systems	10.7 EMBEDDED TUTORIAL – Die Stacking Goes Mobile and Embedded	10.8 PANEL SESSION –State of the Art Verification Methodologies in 2015
1330	10.1.2 SPECIAL DAY KEYNOTE, 1330-1400 Keynote, Room – Oisans							
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1400 to 1530	11.1 INTELLIGENT ENERGY MANAGEMENT – Smart Energy Utilisation: From Circuits to Consumer Products	11.2 Architectural Innovations for Reconfigurable Computing	11.3 Asynchronous Circuits and Advanced Timing Issues in Logic Synthesis	11.4 High Level Synthesis	11.5 New Directions in Testing	11.6 Hardware Design for Multimedia Applications	11.7 HOT TOPIC – New Frontiers in Embedded Systems Design: Technology and Applications	11.8 HOT TOPIC – Stochastic Circuit Reliability Analysis in Nanometer CMOS
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1600 to 1730	12.1 INTELLIGENT ENERGY MANAGEMENT PANEL SESSION – The Role of the EDA Community	12.2 Design and Run-Time Support for Dynamic Reconfigurability	12.3 Reliability and Error Tolerance in Logic Synthesis	12.4 Reliability and Error Tolerance in Logic Synthesis	12.5 Error Correction and Resilience	12.6 Security Modules from Layout to Network-on-Chip	12.7 HOT TOPIC – Sustainability through Massively Integrated Computing...	12.8 HOT TOPIC – Synthesis Supported Increase of Efficiency in Analogue Design

monday 14 march

0730	TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS			
BREAKS	1100-1130 Morning, 1300-1430 Lunch, 1600-1630 Afternoon.			
0930 to 1800	A (Room - Belle-Etoile)	B (Room – Chartreuse)	C (Room – Les Bans)	
	Low Power SOC Design: Best Practice – and what's next?	Electronic System Level Design and Verification	Manufacturing, CAD and Thermal-Aware Design for 3D System-on-Chip Design	
0930 to 1300	D1 (Room – Meije 3)	E1 (Room – 7 Laux 4)	F1 (Room – 7 Laux 5)	G1 (Room – Room Meije 2)
	MPSoC Hardware/Software Architectural and Design Challenges/Solutions	On-chip interconnect for new generation of SoC	Renewable energy: solar power generation, conversion and delivery	Power-Aware Testing and Test Strategies for Low Power Devices
1430 to 1800	D2 (Room – Meije 3)	E2 (Room – 7 Laux 4)	F2 (Room – 7 Laux 5)	G2 (Room – Meije 2)
	Model-based MPSoC Architecture Synthesis for Highly-demanding Embedded Applications	Design and Verification Challenges for Automotive Electronics	Overcoming CMOS Reliability Challenges: From Devices to Circuits and Systems	Testing TSV-Based 3D Stacked Ics
1800	Welcome Reception			

plenary session

Tuesday, March 15, 2011, 0830 – 1030 • Opening Address – Awards – Keynote Speakers

first keynote address

Biologically-inspired massively-parallel architectures – computing beyond a million processors

S Furber, ICL Professor of Computer Engineering, School of Computer Science, Manchester U, UK

Moore's Law continues to deliver ever-more transistors on an integrated circuit, but discontinuities in the progress of technology mean that the future isn't simply an extrapolation of the past. For example, design cost and complexity constraints have recently caused the microprocessor industry to switch to multi-core architectures, even though these parallel machines present programming challenges that are far from solved. Moore's Law now translates into ever-more processors on a multi-, and soon many-core chip. The software challenge is compounded by the need for increasing fault-tolerance as near-atomic-scale variability and robustness problems bite harder.

We look beyond this transitional phase to a future where the availability of processor resource is effectively unlimited and computations must be optimised for energy usage rather than load balancing, and we look to biology for examples of how such systems might work. Conventional concerns such as synchronisation and determinism are abandoned in favour of real-time operation and adapting around component failure with minimal loss of system efficacy.

second keynote address

How technology R&D leadership brings a competitive advantage in the fields of multimedia convergence and power applications

Philippe Magarshack, Group Vice-President, Technology R&D - General Manager, Central CAD and Design Solutions, STMicroelectronics, France

From 1985 to 1989, Magarshack designed microprocessors arithmetic blocks at AT&T Bell Labs in New Jersey, Pennsylvania and California. In 1989, he joined Thomson-CSF in Grenoble, France, as libraries and ASIC Manager. In 1994, Magarshack joined the Central R&D of SGS-THOMSON Microelectronics (now STMicroelectronics), where he held several Program Management roles in advanced CMOS Design Platforms. Since 2005, Magarshack heads ST's Central Library, IP and CAD organisation, which defines and provides design solutions to all ST Product Groups in CMOS, embedded NVM and BCD processes, ranging from 0.35um to

20nm technologies.

In his current role, Magarshack oversees ST's EDA vendor strategy, setting up and managing joint R&D programs to address ST's future design needs. Magarshack is ST's Enablement Executive at the IBM ISDA CMOS Bulk Alliance in 32/28nm and 22/20nm.

Philippe Magarshack was born in London, UK, and graduated with an engineering degree in Physics from Ecole Polytechnique in Palaiseau, France in 1983 and with an Electronics Engineering degree from Ecole Nationale Supérieure des Télécommunications in Paris, France in 1985.

WIRELESS NETWORK for LAPTOP USERS

Access will be FREE throughout the exhibition area for all attendees

tuesday 15 march

Mentor Graphics®

LUNCH AND LEARN SESSION SPONSORED BY MENTOR GRAPHICS -

Grenoble EDA Ecosystem - From Research to Market – Time: 1300 - 1400

Location / Auditorium Dauphine

Moderator: Mark Croft, Mentor Graphics, UK

Three views of the value of European Research to EDA and Semiconductors: CEA-LETI, ST and Mentor Graphics speak of the value of close cooperation in the EU.

1300 FROM RESEARCH TO MARKET Laurent Malier, CEO, CEA-LETI, FR

With its research centers, university campus, 500 foreign companies and 40,000 scientists, engineers and technicians employed in the area, the Grenoble-Isere region, otherwise known as France's Silicon Valley, mixes world-class intellectual and scientific dynamism with exceptional quality of life. It is the ideal sprinboard for Academia-Industry collaboration. This presentation details collaboration schemes between Industry and research institutes and industry happening in Grenoble. This often involves long-term projects based on sharing research costs and requires joint technical programs with a predeterminable timetable, with specific technology transfer and operating conditions.

1320 SUCCESSFUL R&D COLLABORATIONS AS A COMPETITIVE ADVANTAGE

Philippe Magarshack, Group Vice-President, Technology R&D - General Manager, Central CAD and Design Solutions, STMicroelectronics, FR

STs Grenoble center was born as a spin-off from a Grenoble research lab several decades ago. Since then we have continued to maintain our innovation leadership with long-term Public-Private Partnerships in Grenoble, France and Europe. Starting in 1992, ST has partnered with its competitors to build its 200mm and 300 mm R&D centers and fabs in Crolles, near Grenoble. In 2008, ST joined ISDA alliance in Fishkill NY to collaborate to its 32/28nm and 20nm CMOS processes. More recently, ST has reinforced and enlarged the scope of its local R&D partnership to Design and Design Automation. This complete eco-system is now bringing valuable innovation to our products and our customers.

1340 INVESTING IN THE TOP TALENT FOR EDA

Eric Selosse, Vice President and General Manager, Emulation Division, Mentor Graphics, FR

Mentor Graphics has a long track record of investing in Europe for R&D expertise. Over the last year, despite the economic conditions, we have continued to recruit in France, the UK and Poland. Our industry is a meritocracy which relies on the hiring, nurturing and retention of the best world-class engineers available in electronics and associated fields. This presentation will outline why we invest in Europe, why France is such a significant part of this and look at the particular place Grenoble has in this story.

Smart Devices of the Future Special Day

5.1 EMBEDDED TUTORIAL – Smart Devices for the Cloud Era

Room – Oisans 0830-1000

Organisers/Moderators:
A Jerraya, CEA-LETI MINATEC, FR
J Goodacre, ARM, UK

Cloud computing will provide unlimited computing power and mobile terminals will take benefit of these new flexible computing platforms. This session presents the context of future mobile terminals, the key evolutions that will enable access to cloud computing and the new functions that will require cloud computing.

6.1.1 HOT TOPIC/EMBEDDED TUTORIAL – Ultra Low Power Smart Devices

Room – Oisans 1100-1230

Organisers/Moderators:
J Goodacre, ARM, UK
A Jerraya, CEA-LETI MINATEC, FR

Low power is considered the key enabling technology for future smart systems. For most applications stringent requirements on power consumption has to be satisfied. This session presents power issues in different application domains and how specific requirements are addressed. This is illustrated with hardware/software design techniques for concrete products.

7.1 HOT TOPIC – Smart Medical Implants

Room – Oisans 1430-1600

Organisers:
A Jerraya, CEA-LETI MINATEC, FR
J Goodacre, ARM, UK

Moderator:
S Yoo, POSTECH, KR

Medical implants integrate a large number of heterogeneous components (computing, sensors, actuators, antenna, RF) to implement sophisticated functions. Unlike classic devices, the design of medical implants includes the building of application specific architecture and specific interfaces and other kinds of packaging required to efficiently interface with human body. This session introduces the key technologies for the design of such complex devices.

8.1 PANEL SESSION – Integrating the Real World Interfaces

Room – Oisans 1700-1830

Organisers/Moderators:
A Jerraya, CEA-LETI MINATEC, FR
J Goodacre, ARM, UK

Panellists:
P Urard, STMicroelectronics, FR
J Rabaey, UC Berkeley, US
R Bramley, STEricsson, FR
A King-Smith, IMGTEC, UK
W Burleson, Massachusetts U, US
F Perruchot, CEA-LETI, FR

Smart systems require interfacing more of the world in an integrated solution (Camera, gyroscope, compass, temp, direction…). This is imposed by social evolution and enabled by new integration technologies. So far, many products featuring a variety of hardware and software have been developed and many more seems to be coming in a fast growing market. The panel will present the most promising products and solutions and discuss the innovations enabling future smart systems.

6.1.2 LUNCH-TIME KEYNOTE AND AWARDS

Room – Oisans - 1340-1400 Awards and 1400-1430 Keynote

1340 Awards Moderator:
Z Peng, Linkoping U, SE

Awards: Presentation of the DATE 10 Best Paper Awards:

TRACK D - PROPERTIES OF AND IMPROVEMENTS TO TIME-DOMAIN DYNAMIC THERMAL ANALYSIS ALGORITHMS
X Chen and R P Dick, U of Michigan, US
L Shang, U of Colorado at Boulder, US

TRACK E - SKEWED PIPELINING FOR PARALLEL SIMULINK SIMULATIONS
A Canedo, T Yoshizawa and H Komatsu, IBM Research, JP

BEST IP - TOWARDS A CHIP LEVEL RELIABILITY SIMULATOR FOR COPPER/LOW-K BACKEND PROCESSES
M Bashir and L Milor, Georgia Institute of Technology, US

Presentation of the EDAA Outstanding Dissertation Awards

1400 Organiser/Moderator:
A Jerraya, CEA-LETI MINATEC, FR

Keynote Speaker:
Hannu Kauppinen, Director, Head of Radio Systems Laboratory, Nokia Research Center, FI

WIRELESS INNOVATIONS FOR SMARTPHONES

Abstract: The ever increasing demand for fast mobile internet connectivity continues to set challenges for research in radio communications. On one hand the capacity demand can be served by offloading data traffic to local networks. On the other hand using more bandwidth, and possibly dynamically allocating spectrum in a flexible way, will improve the usage of the available spectrum. The future of wireless access continues to be defined by the 3GPP and IEEE standards setting bodies. Radios can also provide innovative features that offer new functionalities for consumers, such as ultra fast local connectivity, sensing and positioning.

Intelligent Energy Management - Supply and Utilisation Special Day

9.1 Energy Transfer, Generation and Power Electronics

Room – Oisans 0830-1000

Organisers:
P Mitcheson, Imperial College, UK
P K Wright, UC Berkeley, US

Moderator:
P Mitcheson, Imperial College, UK

Issues relating to energy resources are set to play an increasing role in all of our futures. This special day at DATE is intended to further involve the EDA community in energy related matters at all scales. This session covers setting the scene for the day on energy, covering topics from levels of micro Watts to Giga Watts.

10.1.1 Smart Energy Generation: Design Automation and the Smart-Grid

Room – Oisans 1100-1230

Organisers:
P Mitcheson, Imperial College, UK
P K Wright, UC Berkeley, US

Moderator:
P K Wright, UC Berkeley, US

This session will look at issues relating to the supply side of the electrical grid, including smart grids and the role of electric vehicles in future supply infrastructure and includes talks from both industry and academia.

11.1 Smart Energy Utilisation: From Circuits to Consumer Products

Room – Oisans 1400-1530

Organisers:
P Mitcheson, Imperial College, UK
P K Wright, UC Berkeley, US

Moderator:
P Mitcheson, Imperial College, UK

This session concentrates on smart use of energy at the demand side - from energy issues at the circuit level to larger scale issues with consumer products and use of energy in the home.

12.1 The Role of the EDA Community in the Future of World Energy Supply and Conservation?

Room – Oisans 1600-1730

Organisers/Moderators:
P K Wright, UC Berkeley, US
P Mitcheson, Imperial College, UK

Panellists:
L Bomhold, Synopsys, US
T Green, Imperial College, UK
A Ephrimides, Maryland U, US
C Blumstein, California Institute for Energy and Environment, US
S Henry, RTE, FR

Until recently the electrical power industry has relied solely on traditional technologies - copper and iron as cables, transformers and machines as the mainstream solution for the generation, transmission and distribution of power. Whilst use of these materials and technologies is here to stay, improvements in power semiconductor technology mean that the industry is moving into a position where more and faster control of power systems can be achieved. This high level control requires a sensing and communication infrastructure to be put in place across the network. At the same time, the use of electricity in the home, through the potential of real time consumer pricing requires new technologies.

This panel session aims to pull together heavy current electrical power engineers and light current electronic engineers to form a discussion and debate about the future role of EDA in applications which are being brought about by changes in the functioning of the power industry. Power engineers from both industry and academia will stimulate the discussion with requirements both from a system perspective and consumer perspective. The representatives from the EDA side will respond with what contributions they believe EDA can make, what already exists or is a simple development problem and what research issues remain in achieving these goals. In summary, this panel aims to provide motivation for the EDA industry to work on useful technology that can be applied to heavy power systems with a view to improving global energy efficiency.

10.1.2 SPECIAL DAY KEYNOTE

Room – Oisans 1330-1400

Organiser:
P K Wright, UC Berkeley, US

Keynote Speaker:
Carmelo Papa, Executive VP Industrial and Multisegment, STMicroelectronics, IT

SMART ENERGY AT ST

The exponential increase of world energy demand, with a forecasted raise of 45%[1] between 2010 and 2030, makes energy management one of the most urgent topics of the century and a key driver for semiconductors and electronics products evolution. The main solutions for world energy demand and global warming issues have been individuated in two main streams: an increasing offer from alternative energy sources and their integration into the new Smart Grid and a reduction of the demand through an increase of systems efficiency.

In energy supply and distribution, the Smart Grid is in fact impacting for an estimated 14% of CO2[2] emissions reduction in the global energy system by 2020. In addition it makes it possible to generate high cost savings for industrial and economic system (188 Billion$ per year estimated only for U.S.[2])

New measures for Energy Efficiency will contribute up to 8 Giga-Tons of CO2 reduction (54% of total with the application of policy 450[1]) by 2020, mostly thanks to power electronics applications.

Along these two areas of intervention, ST is investing to provide both effective power semiconductor technologies and ICs for new topologies for power conversion, but not only. New materials (SiC) for power transistors, innovative solutions for power management and digital control, wired and wireless ICs are some examples of ST offer that apply to energy related applications like PV converters, Smart Metering, Connectivity, Building Automation, Electrical Traction and Motor Control.

Along the energy theme, though at different orders of magnitude, innovation for portable systems is tackled at ST R&D: extremely low consuming CMOS technology for digital ICs, low power RF transceivers, milliWatt capable super thin batteries and 3D integration techniques are the base for miniaturised, long lasting battery based systems, that enable new scenarios especially in portable Healthcare and Wireless Autonomous Sensors Networks.

[1] Source: International Energy Agency
[2] Source: The Climate Group
[3] Source: Grid 2030 A National Vision for Electricity s Second 100 Years, United States Department of Energy, Office of Electric Transmission and Distribution

Friday Workshops

0730	WORKSHOP REGISTRATION & WELCOME REFRESHMENTS
BREAKS	Please see individual workshop programmes for lunch and break times

0830 TO 1700	Room – Les Bans	Room – Meije	Room – Bayard	Room – Berlioz
	W1 Workshop on Micro Power Management for Macro Systems on Chip (uPM2SoC)	W2 Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing	W3 Third Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications	W4 Bringing Theory to Practice: Predictability and Performance in Embedded Systems

0830 TO 1700	Room – Stendhal	Room – 7 Laux 4	Room – Belle-Etoile	Room – Chartreuse
	W5 3D Integration – Applications, Technology, Architecture, Design, Automation, and Test	W6 M-BED'2011, the 2nd Workshop on Model Based Engineering for Embedded Systems Design	W7 Hardware Dependent Software Solutions for SoC Design	W8 1st International QEMU Users Forum (QUF)

DATE 11
OPENING PLENARY

Auditorium Dauphine

Biologically-inspired massively-parallel architectures – computing beyond a million processors

S Furber, ICL Professor of Computer Engineering,
School of Computer Science, Manchester U, UK

How technology R&D leadership brings a competitive advantage in the fields of multimedia convergence and power applications

P Magarshack, Group Vice-President, Technology R&D - General Manager, Central CAD and Design Solutions, STMicroelectronics, FR

tuesday 15 march

ET01 Highlights of DATE11 Exhibition /Clustering – an Enabler for Micro and Nanoelectronics

1045 - 1115

Organiser/Moderator:
Juergen Haase, edacentrum, Germany
Speaker:
Andreas Bruening, Silicon Saxony, Germany

Abstract: Each morning Juergen Haase (edacentrum, Germany) will open DATE11 Exhibition with an overview about the highlights of the Exhibition program and provide brand-new information on "What's hot today" to all attendees .

Andreas Brüning, in the Silicon Saxony Cluster (Germany) responsible for the work of the micro/nanoelectronic devision, will invite all attendees to establish close collaboration between clusters like Grenoble and Dresden in his talk:

Clustering: an Enabler for Micro and Nanoelectronics

A short overview about Silicon Saxony will be followed by describing micro and nanoelectronics as an opportunity for Europe as well as clustering as an enabler for micro and nanoelectronics based on the example Grenoble and Dresden. Presentation of Dresden & Genoble cluster as a cooperation for Europe and the expectation to strengthen exchange in Design Automation experience.

2.8 EMBEDDED TUTORIAL – Addressing Critical Power Management Verification Issues in Low Power Designs

1130 - 1300

Organiser:
B Kapoor, Mimasic, US
Moderator:
K Just, Infineon, DE

Abstract: Power management techniques that leverage voltage as a handle are being extensively used in power sensitive designs. These techniques include power gating, power gating with retention, multiple supply voltages, dynamic voltage scaling, adaptive voltage scaling, multi-threshold CMOS, and active body bias. The use of the power management techniques also imply new challenges in validation and testing of designs as new power states are created. We look into verification issues along with the solutions to these issues using a verification strategy that involves power-aware simulation, rule-based structural checking, formal tools, and methodology recommendations. We detail our varied experiences with various design teams in addressing these low power verification issues for applications such as the wireless handset, low power microprocessors, and GPS.

3.8 PANEL SESSION – Power Formats: Beyond UPF and CPF

1430 - 1600

Organiser/ Moderator:
B Pangrle, Mentor Graphics, US
Panellists:
J Biggs, ARM, UK
C Clavel, ST-Ericsson, FR
O Domerego, Texas Instruments, FR
K Just, Infineon/Intel, DE
B Moison, STMicroelectronics, FR

Abstract: Two formats for specifying power intent are currently in wide use in industry today and as designers continue to strive for more power efficient designs new issues arise that certainly need new solutions to improve on today's standards. This panel will discuss areas for improving today's power formats and the direction that these formats need to move in order to provide the most efficient flows for design and verification and especially with regards to low-power. The scope of the formats and their suitability from early ESL design exploration to back-end sign-off checking will also be discussed along with any issues that need to be addressed in order to make design and verification engineers more productive.

ET02 What is missing to enable global IP collection, assembly, and virtual platform distribution?

1615 - 1715

Organiser:
Magillem
Moderator:
Mladen Berekovic, University of Jena, Germany
Speakers/Panellists:
Cyril Spasevski, Magillem, CTO, France
Michael McNamara, Cadence, VP and GM and System Software Group, USA
John Goodenough,
ARM, VP Design Technology and Automation, UK
Antoine Perrin, ST, CAD Manager, France

Abstract: The domains of RTL design, virtual platforms, high level synthesis, and IP assembly automation are converging to enhance the productivity and reliability of system level design methodology. A significant number of companies are creating RTL IP catalogs and leveraging assembly automation to rapidly produce incrementally innovative SoCs. Virtual platforms are enabling a growing practice pre-RTL software development. High level synthesis is increasing the productivity to create new RTL IP. The confluence of these forces is creating a plethora of opportunities, and presenting several challenges. This panel will explore and debate the priorities and benefits of these emerging trends and discuss the following questions:

* How far along are customers in creating internal virtual platform IP catalogs?
* What are the challenges of organizing virtual platform and RTL IP catalogs?
* How do IP-XACT and assembly tools help with this internal management problem
* Are companies starting to organize 3rd party IP suppliers to provide virtual platform and RTL IP, as well as IP-XACT
* What are the challenges in defining IP catalog requirements to 3rd parties?
* Are standards needed in addition to IP-XACT to enable freer IP creation and exchange?

ET03 STMicroelectronics automates quality monitoring for improved design productivity

1730 - 1750

Organiser:
Satin Technologies, STMicroelectronics
Speaker:
Indavong Vongsavady, ST CCDS

Abstract: The Central CAD and Design Solutions (CCDS) group at STMicroelectronics is in charge of developing and deploying design libraries, kits, flows and methodologies throughout the different groups at ST and ST-Ericsson. They also offer internal design services for very complex chips.

In order to make design quality monitoring more timely and accurate, ST CCDS has adopted VIP Lane to help turning their design checklists into fully automated dashboards. These dashboards are becoming the foundation for on-the-fly, fact-based communication between all stakeholders of the same design project.

This presentation will show the benefits of this approach (sharing of more formal design practices, accurate communication between design teams, shorter design cycle) and illustrate these benefits with real life examples.

ET04 Optimization of Power-MOS Structures dedicated to Energy Management ICs

1750 - 1810

Organiser:
Edxact, ST-Ericsson
Speaker:
Jérôme Lescot, ST-Ericsson, France

Abstract: Impact of metal routing on 'rdson' parameter of power-MOS devices is increasing with more advanced process nodes (65n, 40n). Capacity of comanche tool to quickly extract thousands of pin to pin resistances enables us to achieve layout optimization by analysing resistances distribution from pads to any individual transistor. In addition, jivaro reduction makes possible the spice simulation of the structure including both parasitic resistors and functional devices to extract rdson parameter.

Exhibition Theatre Overview

Tuesday 15th March

1045 - 1115	**ET01 Day 1 Opening Session:** Highlights of Date11 Exhibition / Clustering – An Enabler for Micro and Nanoelectronics
1130 - 1300	**2.8 Embedded Tutorial:** Addressing Critical Power Management Verification Issues in Low Power Designs
1430 - 1600	**3.8 Panel:** Power Formats: Beyond UPF and CPF
1615 - 1715	**ET02 Panel:** What is Missing to Enable Global IP Collection, Assembly, and Virtual Platform Distribution?
1730 - 1830	**ET03 Testimonial:** STMicroelectronics Automates Quality Monitoring for Improved Design Productivity
	ET04 Testimonial: Optimization of Power-Mos Structures Dedicated to Energy Management ICS
	ET05 Testimonial: How Software Development Can Take Benefit of a Platform Power Model

Wednesday 16th March

1000 - 1030	**ET06 Day 2 Opening Session:** Highlights of Date11 Exhibition / More Than Moore Solutions for Automotive Products
1030 - 1050	**ET07 Testimonial:** Ball Grid Array Packages Electrical Optimization Using Apache Package Modeling Tools
1100 - 1230	**6.8 Panel:** Embedded Software Debug and Test
1315 - 1415	**ET08 Panel:** Process Variability: Challenges and Solutions
1430 - 1600	**7.8 Embedded Tutorial:** Predictable System Integration
1700 - 1830	**8.8 Embedded Tutorial:** Communication Networks in Next Generation Automobiles

Thursday 17th March

1000 - 1010	**ET09 Day 3 Opening Session:** Highlights of Date11 Exhibition / Testimonials
1010 - 1030	**ET10 Testimonial:** System Level Power Integrity Analysis and Supply Network Optimization of a Dual Core CPU
1030 - 1050	**ET11 Testimonial:** Co-Verification of an Interrupt Driven Firmware Subsystem using Cadence ISX and Coverage Driven Techniques
1100 - 1230	**10.8 Panel:** State of the Art Verification Methodologies in 2015
1245 - 1345	**ET12 Panel:** Early Timing and Power Information of Complex SoC Designs using Augmented Virtual Platforms
1400 - 1530	**11.8 Hot Topic:** Stochastic Circuit Reliability Analysis in Nanometer CMOS
1700 - 1830	**12.8 Hot Topic:** Synthesis Supported Increase of the Analog Design Efficiency

ET05 How Software development can take benefit of a platform power model

1810 - 1830

Organiser:
DOCEA Power, ST-Ericsson

Speaker:
Patrick Arnould, Senior System Architect, ST-Ericsson, France

Abstract: The increasing complexity of applications running on multimedia mobile platforms is becoming more and more critical for battery life, so software optimization to take into account power consumption is crucial but could become very painful without a dedicated environment. A lot of power saving is possible at the software level but the investigations are complex due to the number of parameters involved in this optimization: clock gating, dynamic power switching, dynamic voltage and frequency scaling, traffic, CPU and IP load.

In this testimonial, a validation environment will be used as an example to show the benefit for software developers to have access to a combination of CPU load, traffic and power figures phase per phase and power supply per power supply. It also outlines the challenges for a power modeling methodology to be able to target a wide range of applications, very low power and power hungry systems optimization. Taking the benefit of having a platform power model and before starting any software development, key decisions can be taken to focus very quickly on the best software option to gain power.

The testimonial scope goes from power model construction to fast software optimization on a real application showing the benefit to speed up software development and platform power optimization.

wednesday 16 march

ET06 Highlights of DATE11 Exhibition /More than Moore Solutions for Automotive Products

1000 - 1030

Organiser/Moderator:
Juergen Haase, edacentrum, Germany

Speaker:
Andreas Bruening, ZMD, Germany

Abstract: Each morning Juergen Haase (edacentrum, Germany) will open DATE11 Exhibition with an overview about the highlights of the Exhibition program and provide brand-new information on "What's hot today" to all attendees.

Andreas Brüning, director technology office of ZMD (Germany), will review the productivity in designing More than Moore applications and discuss what is required for analog-mixed signal automotive products in his talk:

Trends, Challenges and Solution Statements for More than Moore concerning Analog-Mixed Signal Automotive Products

Analog Mixed Signal is a very healthy niche regarding micro-/nanoelectronics. Unfortunately the design productivity has not developed much during the last decade and is far behind the More Moore miniaturization. The talk is dealing with the increasing complexity and related productivity based on an analog-/mixed signal benchmark. Demonstrating design challenges, optimization areas and existing solutions. As a result the hot topics for productivity increase are shown.

ET07 Ball Grid Array Packages electrical optimization using Apache package modeling tools

1030 - 1050

Organiser:
Apache / ST

Speakers:
Yvon Imbs, ST Corporate Packaging & Automation, France
Laurent Marechal, ST Corporate Packaging & Automation, France

Abstract: Today's packages are facing many challenges linked to cost pressure, Time to Market improvement, miniaturisation. These evolutions are not, for some of them, moving in the right direction to sustain the performances expected by the end users.

Cost pressure is leading to reduction of area for the Silicon and for the mass production packages will lead to a limitation to off-the-shelf technologies or development of new cost reduction processes and technologies.

Time to market is requesting first design to be the final product. This can only be achieved by an increase effort in term of modelling. Modelling in therefore mandatory in all fields, system level, component level, die level etc… All physical domains are contributing: electrical, thermal, mechanical & thermo-mechanical.

Miniaturisation will request smaller package, thinner traces, thinner substrate. All these aspects have consequences on the electrical behaviour of the package. From a "electrical transparent" media in the end of 1999, there are now becoming the bottlenecks in many applications.

In this talk we will first demonstrate the effects of these constraints on real package designs, in term of application speed, bandwidth of signals, and impact on the margins. We will also explain why the counterpart of this increasing complexity in the package is requesting the help of new tools that can bridge the several part of the system to ensure a full system optimisation.

Preliminary package studies are necessary to define the packaging technology that needs to be optimized versus the die and the board. It consists in impedance computation, interfaces layout strategy and power delivery strategy. The used tools and the results expected from these preliminary studies may differ depending the application and/or the interfaces.

Digital consumer projects (TV, Computer, etc…) are usually using quite big packages as they are not constrained by a form factor. This enables the use of power & ground planes on dedicated layers of the package. The package size and the interface speed are thus requesting a control of the impedance for both single and differential signals.

We will show simulation results based mainly on digital projects (TV applications, Computer & Broad band signals).

Several modelling tools have been used:

* 2D tools (Ansoft) are used to define the impedance guideline derived from the selected technology

* Fast quasi-static modelling tools enables the extraction of the preliminary design databases models for both signal nets and power delivery network

First order results will then permit to validate some early choices in term of technology and routing strategy. They are also used to start some preliminary simulation at system level to ensure time to market objectives.

More accurate models will generated later on during the design phase to refine the simulations and get more quantitative results (Apache Sentinel PSI, Ansoft HFSS)

Package and board resonances can also be studied once the design database are close to completion. Linking the package and board database leads to resonance frequencies that need to be considered versus the application frequencies.

Mobile platform system using multi-GHz CPU cores are needing a proper methodology to handle the power integrity analysis and supply network.The optimization of the power delivery network (PDN) of a System on Chip (SoC) is becoming more and more complex with the increasing operating frequency of its CPU cores.

The defined methodology is mainly using Apache tool features to generate the needed models and run the required analysis. The capabilities of Apache RedHawk are to extract a power model from a SOC, that can be reused in package centric tools to optimise further the power delivery network at package (and board) level. On the other side the package modelling tool (Apache Sentinel NPE) is able to extracted a model that can be imported in the die voltage drop analysis tool (Apache RedHawk) to evaluate the impact of the package routing.

SPEAKERS' BIOGRAPHIES

Yvon Imbs joined STMicroelectronics in 2000 after being graduated as a Ph.D from University of Limoges. He worked for 4 years as responsible of electrical package modeling. He started some activities on IC package co-design inside the Telecom, Peripheral & Automotive Division of ST. Then he joined the Corporate Packaging & Automation team. In addition to the electrical package modeling, he started a Package Design Kit activity linked to the ramp-up of the IC-Package co-design activity. Now he's is charge of the electrical driven co-design aimed to ensure the best trade-off between cost & performances for the BGA packages.

Laurent Marechal joined STMicroelectronics in 2006 after being graduated as M.S. degree in electrical engineering from Polytech'Lille. He joined the Corporate Packaging & Automation team to develop embedded passive devices. In addition he is now in charge of accurate package modeling using 3D Electromagnetical tools and of the support of the electrical driven co-design activity aimed to ensure the best trade-off during BGA package design in close relation with the product Divisions.

6.8 PANEL SESSION – Embedded Software Debug and Test

1100 - 1230

Organiser/Moderator:
M Winterholer, Cadence, DE

Panellists:
F Cerisier, EASii-IC, FR
S Davidmann, Imperas, UK
L Ducuosso, STMicroelectronics, FR
J Engblom, Simics Wind River, SE
A Mayer, Infineon, DE

Abstract: Today's complexity of embedded software is steadily increasing. The growing number of processors in a system and the increased communication and synchronisation of all components requires scalable debug and test methods for each component as well as the system as a whole. Considering today's cost and time to market sensitivity it is important to find and debug errors as early as possible and to increase the degree of test and debug automation to avoid quality losses. These challenges are not only requiring new tools and methodologies but also organisational changes since hardware and software developer have to work closer together to achieve the necessary productivity and quality gain. The panel will discuss new strategies in hardware and software development to make embedded software more reliable and easy to debug.

ET08 Process Variability: Challenges and Solutions

1315 - 1415

Organiser/Moderator:
Stephane Fiorillo, Infiniscale, France

Speakers/Panelists:
Trent McConaghy, Solido Design Automation, USA
Jean-Paul Morin, STMicroelectronics, France
Philippe Raynaud, Mentor Graphics, France
Vincent Fischer, Infiniscale, France

Abstract: This panel will focus on the process variability affecting analog, mixed-signal, and custom digital designs, the various challenges it raises and the solutions that can be applied to handle those issues. A presentation of the various types of process variability (lot to lot or global variations, local variations such as mismatch, layout effects…) will be done. The stakes of this variability will be highlighted, in particular the effects on the yield. The various approaches to handle this variability will be presented. At simulation level, from PVT corner simulations to statistical analysis (Monte Carlo and enhanced Monte Carlo), various approaches can help the designer to analyze the effects of the process variability, and to determine the yield. The model-based approach, which uses simulation results to build a behavioural model, allows the designer to optimize the device sizes taking into account the process variability in order to minimize its effects and maximize the yield. Some concrete examples will be presented, with the presentation of the design, the effects of process variability, the solutions that were implemented and the final results. Finally, the panel will be concluded by on open discussion and questions from the audience.

7.8 EMBEDDED TUTORIAL – Predictable System Integration

1430 - 1600

Organiser/Moderator:
W Kruijtzer, Synopsys, NL

Abstract: Starting from the application side, we present system functions and their implementations on CPUs and function-specific hardware using concrete examples from the video processing domain. This includes quantitative data on bandwidth and latency requirements and an overview of challenges developers face if the SoC infrastructure lacks basic provisions for Quality-of-Service. We then present how these challenges can be addressed by a combination of architectural principles and associated

analysis techniques, based on network calculus. Finally we show how these techniques can be applied in building real-life SoCs. Key benefits of the presented techniques are predictable performance and improved time-to-market, while avoiding costly over-dimensioning to guarantee real-time behaviour.

8.8 EMBEDDED TUTORIAL – Communication Networks in Next Generation Automobiles

1700 - 1830

Organisers:
T Kazmierski, Southampton U, UK
C Grimm, TU Vienna, AT
Moderator:
C Grimm, TU Vienna, AT

Abstract: The tutorial addresses upcoming technologies aimed at communication networks for automotive applications. The first presentation will discuss applications of networked or even autonomous sensors in a car. The second presentation will emphasize novel, cross-industry communication technologies that enhance the standard IEEE 802.3 switched Ethernet. The third and fourth presentations will introduce applications and methods for the design of wireless communication in a car, including methods for wireless energy supply of sensor nodes in cars as well as design tools and methods for design of wireless sensor nodes.

thursday 17 march

ET09 Highlights of DATE11 Exhibition /Testimonials

1000 - 1010

Organiser/Moderator:
Juergen Haase, edacentrum, Germany

Abstract: Each morning Juergen Haase (edacentrum, Germany) will open DATE11 Exhibition with an overview about the highlights of the Exhibition program and provide brand-new information on "What's hot today" to all attendees .

This will be followed by testimonials providing attendees with experience gained in real-life projects: designers present how they were able to solve major design challenges with state-of-the-art methodologies and tools.

ET10 System level power integrity analysis and supply network optimization of a dual core CPU

1010 - 1030

Organiser:
Apache / ST-Ericsson
Speakers/Panelists:
Olivier Bayet, System in Package (SiP) design, ST-Ericsson, France

Abstract: The optimization of the power delivery network (PDN) of a System on Chip (SoC) is becoming more and more complex with the increasing operating frequency of its CPU cores. Having a proper methodology to handle the power integrity analysis and supply network optimization is required to secure the integration of multi-GHz CPU cores in a mobile platform system.

The approach used for ST-Ericsson U8500, the industry's first dual core SMP platform integrating a HSPA+ modem, is based on a system level context available in the simulation environments of each PDN contributor. For this project, the analysis goal was to reach an operating frequency of 1GHz by optimizing the power integrity of the ARM Dual Cortex A9 embedded in the U8500 platform.

In this paper, the first part is describing the methodology and flow used to perform a CPU core power integrity check in a core block level environment using a system level context. The second part is explaining how to extend it to an analysis in package or platform environment still using a system level context. For this methodology, Apache Design Solutions tools provide useful features and extracted models to enable power supply analysis at system level.

Taking into account the capabilities of Apache RedHawk to load a top level and package context even for a voltage drop analysis at block level, a SoC partition is created and plugged into the tool with models of a package and a board with its decoupling capacitors and a voltage regulator. From this analysis, a Chip Power Model (CPM) is generated to enable, in Apache Sentinel-PI and other tools, both package and board level analyses taking into account the complete system.

For the U8500 project, this study resulted in a PDN impedance reduction of about factor 6 in the critical frequency range and enabled an increase from a 600MHz to a 1GHz ARM Dual Cortex A9. This also provided an efficient placement, number and value of decoupling capacitors.

The benefit of this solution is the consistency of models and analysis in the various environments, an access to a simple model (describing a CPU core power/ground grid and its current activity) that could be used with different simulation setups, and an enabler for correlation with measurements. This methodology also provides a first step to solve the foreseen challenges of the next generations of CPU cores.

SPEAKERS' BIOGRAPHY

Olivier Bayet joined STMicroelectronics in 2000 after graduating as a microelectronics engineer from ENSEIRB engineering school. He has worked as a CAD design engineer in the area of IC/Package assembly checks and Voltage Drop analysis, and is currently leading in ST-Ericsson an IC/Package co-design and Signal & Power integrity activity for digital ICs embedded in mobile platforms.

ET11 Co-Verification of an interrupt driven firmware sub-system using Cadence ISX and Coverage Driven techniques

1030 - 1050

Organiser:
EASii-IC, France
Speaker/Panellist:
François Cerisier, Senior Verification Consultant and EDA Activities Manager, EASii-IC, France

Abstract: As System-On-Chip complexity continues to increase, complex state machines are being replaced by processor based sub-systems. The functionalities of such sub-systems are partitioned between hardware blocks and dedicated interrupt based firmware.

Verifying such sub-systems faces the challenge of identifying bugs not only in both the hardware and the software parts, but also at the boundary of the two disciplines.

Co-Verification methodologies have proved to be interesting approaches for critical software verification. Existing methodologies are however based on the assumption that the software provides APIs or software interfaces. They therefore do not directly apply to interrupt driven firmware of these sub-systems.

We present here an approach which enables interrupt based firmware verification for such partitioned hardware/firmware sub-systems at the early stages of the project and before the silicon is available. This methodology has been applied on an industrial complex control sub-system. Hardware event controllability and observability is reached using extended hardware coverage driven verification techniques and the required software observability is achieved using the monitoring facilities of Cadence ISX tool (Incisiv Software Extension).

10.8 PANEL SESSION –State of the Art Verification Methodologies in 2015

1100 - 1230

Organiser:
T Fitzpatrick, Mentor Graphics, US
Moderator:
A Crone, Mentor Graphics, SE
Panellists:
C Chevallaz, STMicroelectronics, FR
B Dickman, ARM, UK
V Esen, Infineon Technologies, DE
O Bringmann, FZI, DE
M Rohleder, Freescale, DE

Abstract: In the last few years, the industry has seen acceleration in the evolution of verification methodologies. While the industry focus has been on enabling a standard based approach to help today's challenges, one can wonder what is needed to prepare us self for the further verification challenges. The expert panellists will discuss the many aspects of verification methodologies, the requirements and predictions for verification methodologies needed 4-5 years from now on.

ET12 Early Timing and Power Information of Complex SoC Designs using Augmented Virtual Platforms

1245 - 1345

Organiser:
COMPLEX FP7 European integrated project
Moderator:
Kim Grüttner, OFFIS, Germany
Speakers/Panellists:
Kim Grüttner (OFFIS)
Bart Vanthournout (Synopsys)
Franco Fummi (EDALab)
Emmanuel Vaumorin (Magillem Design Services)

Abstract: Consideration of an embedded system's timing behavior and power consumption at system-level is an ambitious task. Sophisticated tools and techniques exist for power and timing estimations of individual components such as custom hard and software as well as IP components. But prediction of the composed system behavior can hardly be made.

In this session we present the concept of an ESL framework for timing and power aware rapid virtual system prototyping of embedded HW/SW systems. Our proposed flow combines system-level timing and power estimation techniques available in commercial tools with platform-based rapid prototyping. Our proposal aims at the generation of executable virtual prototypes from a functional C/C++ specification. These prototypes are enriched by static and dynamic power values as well as execution times. They allow a trade-off between different platforms, mapping alternatives, and optimization techniques, based on domain-specific workload scenarios. The proposed flow will be implemented in the COMPLEX FP7 European integrated project (http://complex.offis.de).

11.8 HOT TOPIC – Stochastic Circuit Reliability Analysis in Nanometer CMOS

1400 - 1530

Organiser/Moderator:
G Gielen, KU Leuven, BE

Abstract: Process variability causes statistical spread on the performance of ICs, eventually limiting circuit yield. In addition, aging effects in nanometer CMOS technologies cause a shift in transistor parameters over time, possibly causing circuit malfunction within the lifetime of the circuit. Some of these wear-out phenomena are stochastic in nature, introducing asymmetry in circuits. To guarantee a reliable product over the entire lifetime, fast and efficient design tools can help a designer to estimate the impact of various reliability threats on his/her circuit, at design time. The stochastic nature of the phenomena requires techniques well beyond current commercial tools. This hot topic session addresses both accurate stochastic transistor compact models that include reliability effects, as well as efficient stochastic CAD solutions to evaluate the reliability of an IC at circuit level and at system level. In addition, alternative novel system approaches are presented that exploit the stochasticity.

12.8 HOT TOPIC – Synthesis Supported Increase of Efficiency in Analogue Design

1600 - 1730

Organiser:
J Nowak, IMMS GmbH, DE
Moderator:
R Sommer, TU Ilmenau, DE

Abstract: Analogue design still is the bottleneck in the development of mixed-signal ICs. This is due to the fact that the three steps in analogue circuit design – topology generation or modification, sizing and layout generation – are mainly carried out by hand. In this special session four methods will be presented which allow a semi-automated design process. These approaches include a fully automated hierarchical topology generation for analogue circuits, a generation of a compensation network by automated topology modification, a methodology for sizing based on a combination of analytic and numerical techniques and a method for modular layout generation. The methods and the resulting tools relieve the designer from routine tasks, allow more space for creativity and enable re-use.

48 DESIGN AUTOMATION CONFERENCE

The **Design Automation Conference (DAC)** is the world's leading technical conference and tradeshow on electronic design and design automation.

It is where IC Design and EDA ecosystem learns, networks, and conducts business.

DAC features 175+ exhibitors, over 300 presentations consisting of technical sessions, panels, exciting keynotes, tutorials, co-located workshops and events covering the latest in design methodologies, embedded software and systems and EDA tool developments.

LEARN SHARE & NETWORK

DON'T MISS THE 48th DAC

EXCITING SESSIONS

48th Design Automation Conference
June 5-10, 2011
www.dac.com

The DATE 11 conference programme allows generous opportunities for delegates to visit the exhibition and attend the presentations in the exhibition theatre.

COFFEE & LUNCH BREAKS

Delegates coffee will be served in the main exhibition hall and the additional exhibition area. Lunch is available in Room Ecrins on the lower ground floor and in the exhibition hall there is a cash bar for visitors and exhibitors.

Tuesday 15 March

Morning Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Afternoon	1600 – 1700

Wednesday 16 March

Morning Coffee Break	1000 – 1100
Lunch Break	1230 – 1340
Afternoon	1600 – 1700

Thursday 17 March

Morning Coffee Break	1000 – 1100
Lunch Break	1230 – 1330
Afternoon	1530 – 1600

Evening Reception offered by the City of Grenoble

1830-1930 - Tuesday 15 March

DATE PARTY

1930 - Wednesday 16 March

This year the DATE party will take place in the World Trade Center on Wednesday 16 March. The evening will feature a buffet style dinner with plenty of buffet points and drinks to accompany dinner. Musical entertainment with the opportunity to dance will be provided by the popular neo-folk band DJAL. In an enjoyable atmosphere participants will have the opportunity to meet and mingle with their friends and colleagues. All conference attendees, users, vendors and their guests are encouraged to come to the party. Additional tickets for the full Evening Social Programme may be obtained for 70 Euros each (please ask at the registration desk). Entrance will be by ticket only, so please check that you receive the party ticket when you register.

A number of specialist interest groups will be holding their meetings at DATE. Currently, the following meetings are scheduled but a full list of fringe meetings with description of content will be found on the DATE web portal – www.date-conference.com

Day	Time	Meeting & Contact	Room	Type
Mon	1900-2100	EDAA/ACM PhD Forum Peter Marwedel <peter.marwedel@tu-dortmund.de>	Salle de Reception	Open
Tues	1830-1930	EDAA General Assembly Norbert Wehn <wehn@eit.uni-kl.de>	7 Laux 4	Open
Tues	1830-2030	ETTTC Meeting Matteo Sonza Reorda <matteo.sonzareorda@polito.it>	Bayard	Open
Tues	1830-2130	European SystemC Users Group Meeting Axel Braun <abraun@informatik.uni-tuebingen.de>	Meije	Open
Thu	1730-2030	DIAMOND Tutorial: Handling the Challenges of Debug and Reliability Maksim Jenihhin <maksim@pld.ttu.ee>	Les Bans	Open

Event sponsors

Commercial sponsor

The event is sponsored by:

the European Design and Automation Association

the EDA Consortium

IEEE Council on EDA

ECSI

ACM - SIGDA

RAS

and is organised in cooperation with:

ACM - SIGBED

IEEE Computer Society

IEEE Solid-State Circuits Society (SSCS)

IFIP

IET

SAME

The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in their editorial pages. Listed below are the media houses and publications who generously agree to media partnership with DATE, and whose publications can be found at distribution points around the exhibition.

CHIP DESIGN MAGAZINE

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won't want to miss. And, be sure to visit www.http://eecatalog.com/ for valuable information about all of Extension Media's outstanding technology resources.

EDA CONFIDENTIAL

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes "Recipes", Freddy Santamaria's "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

ELECTRONIQUES

ElectroniqueS the reference monthly for decision makers and engineers in the electronics sector

Circulation of 10,000 copies

www.electroniques.biz, the electronic professional's web site

Daily Newsletter, the day's essential news about our industry's major sectors

Sent to more than 26,000 free subscribers

Weekly newsletter, the newsletter that summarizes the previous 5 daily newsletters main topic

Sent to more than 23,000 free subscribers

Vertical newsletter, 3 subjects: Automotive / Mil-Aero / Medical

5 mailings a year (each 2 in 3 months)

ELEKTRONIK I NORDEN

Elektronik i Norden, an important tool for the Nordic electronic industry. We want Elektronik i Norden to be the most important source of information for the Nordic electronic industry (Sweden, Finland, Norway and Denmark). A circulation of 25 800 personally addressed copies proves we are the major electronics paper in this area. We publish news, comments and in-depth technical articles.

MICRONEWS

Beginning in 1998 with Yole Développement, we have grown to become a group of companies providing market research, technology analysis, strategy consulting, media in addition to finance services. With a solid focus on emerging applications using silicon and/or micro manufacturing Yole Développement group has expanded to include more than 40 associates worldwide covering MEMS and microfluidics, Advanced Packaging, Compound Semiconductors, Power Electronics, LED, and Photovoltaic. The group supports companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to develop their business.

Micronews Media includes our website, www.i-micronews.com, our bi-weekly magazine Micronews, and the four Technology Magazines: MEMS Trends, 3D Packaging, PV Manufacturing and Efficen'Si.

TECH DESIGN FORUM

Today's electronic design engineers face broader challenges than ever before. Software is becoming as important as hardware. And in the IC supply chain, former competitors are now collaborating to achieve success.

Tech Design Forum publication (formerly called the EDA Tech Forum) is the premier guide for success in this complex environment. Focused on the design automation market, this publication and its rich website offer a wealth of practical advice on how to successfully negotiate the day-to-day problems designers face.

The IET

The IET is europe's largest professional body for engineers and technologists, we offer a wide range of products, services and professional qualifications to keep you ahead of the game. With 150,000 members based in 127 countries networking is key to their and your success - find out how to join and be part of the Knowledge Network by visiting us www.theiet.org

THE NEXT SILICON VALLEY

The Next Silicon Valley is an independent media website that publishes global news and information about the world of innovation, entrepreneurship, technology development, regional economic development, venture capital, and investment promotion across global markets. The Next Silicon Valley reaches readers in more than 90 countries and 400 cities worldwide.

If you would like to arrange a Media Partnership with DATE for future events, please contact: Claire Cartwright, Event Manager, European Conferences, tel: +44 (0) 203 052 8065 email: claire.cartwright@ec.u-net.com

DATE 2011 presents the Tool Seminar Track.

The seminars listed below are FREE & OPEN TO ALL, however places are restricted.
All seminars are held in Salle Berlioz on the Ground Floor, adjacent to the registration desk.
Please collect a voucher from the registration desk.

cadence

EUROPRACTICE

What's new in the Europractice Cadence portfolio for 2011 – Technical Update

Tuesday 15 March, 1330-1730

Today 386 institutes across Europe are using Cadence tools via Europractice in their education and research. The portfolio is continuously evolving as new tools become available from Cadence. This seminar gives an update on the latest functionality from a technical viewpoint with special emphasis on digital, mixed signal and low power design including chip planning. The seminar also gives an opportunity for academic institutions to ask Cadence technical and R&D staff questions.

cadence

Unifying IP-XACT platform assembly with virtual platform modeling

Wednesday 16 March, 1330-1630

The goals for IP-XACT have expanded from RTL IP warehousing and easier SoC assembly. As virtual platform adoption has grown, the natural need arises to assemble TLM IP into a virtual platform, and refine it into the resulting RTL SoC. This tutorial will highlight the creation and assembly of SoCs starting from virtual platforms, key decisions to be taken, and potential issues to avoid.

Presenter:
Jean-Michel Fernandez (jmf@cadence.com), Cadence; Cyril Spasevski, Magillem

ADVANCES AT CMP

Thursday 17 March, 0900-1230

CMP is a broker in ICs and MEMS for prototyping and low volume production. Advanced industrial processes are available in CMOS, BiCMOS, SiGe BiCMOS, SOI, GaAs, MEMS and 3DIC. CMP distributes and supports Design Kits and several CAD tools.

The Seminar will review available processes as well as recently introduced processes like 3DIC from Tezzaron, 20nm FDSOI from LETI, pHEMT GaAs from TRIQUINT.

New processes will also be introduced like a magnetic-CMOS process.

Presenter:

Bernard Courtois, Kholdoun Torki

european EDA village

A significant number of European EDA vendors will join forces and provide the semiconductor industry with dedicated innovation for chip and system development. In addition to their booths in the European EDA village, presentations providing overviews and testimonials shall be taking place in the Exhibition Theatre, along with workshops in conjunction with client companies.

Please see the current list of EDA Village participants below:

COMPANY NAME	STAND NUMBER
CISC Semiconductor Design + Consulting GmbH	43
Concept Engineering GmbH	42
Docea	39
INFINISCALE	40
MunEDA	31
Nano-Tera.ch	45
Satin Technologies	41
XYALIS	34

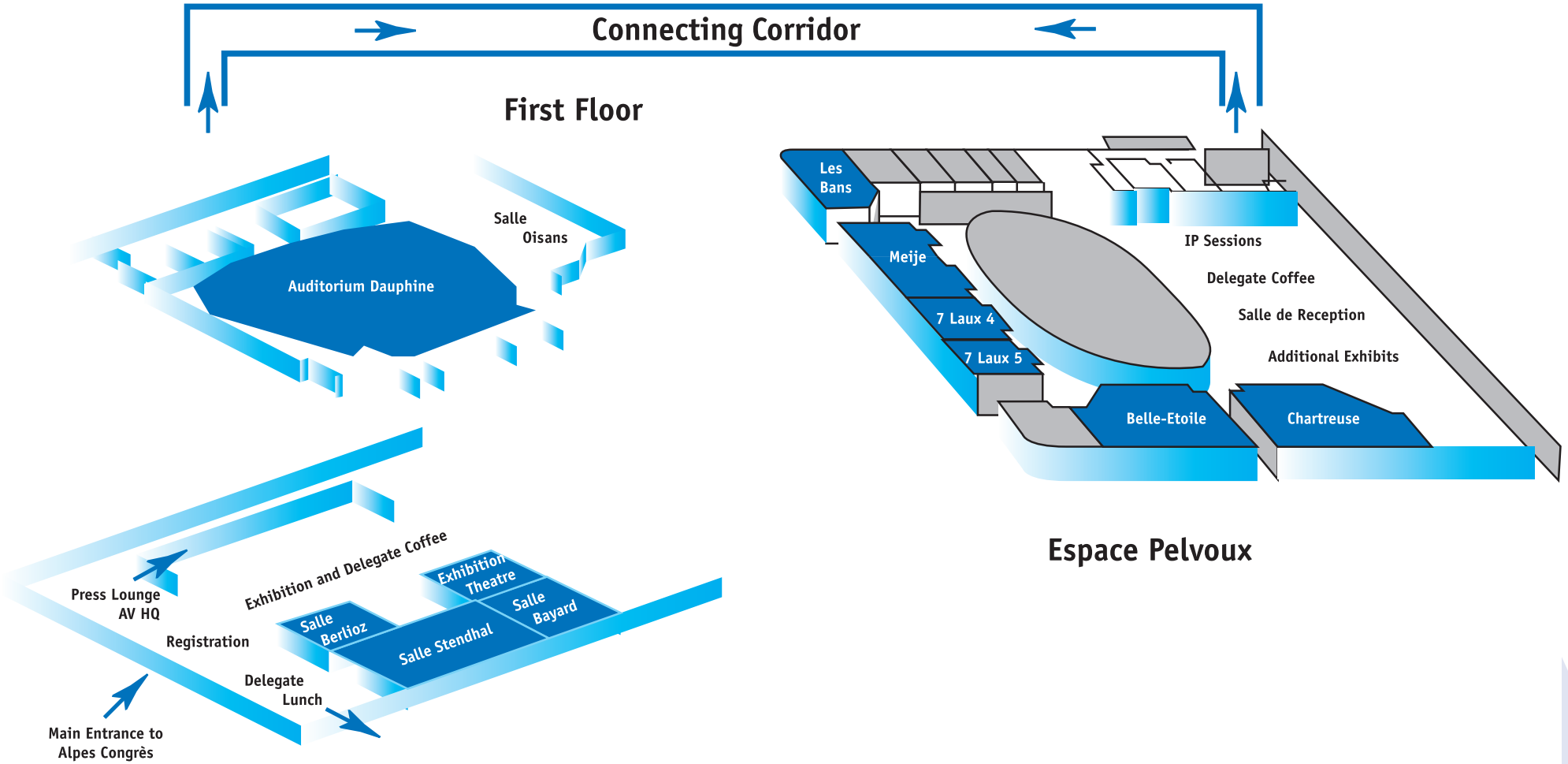
INTERACTIVE PRESENTATIONS

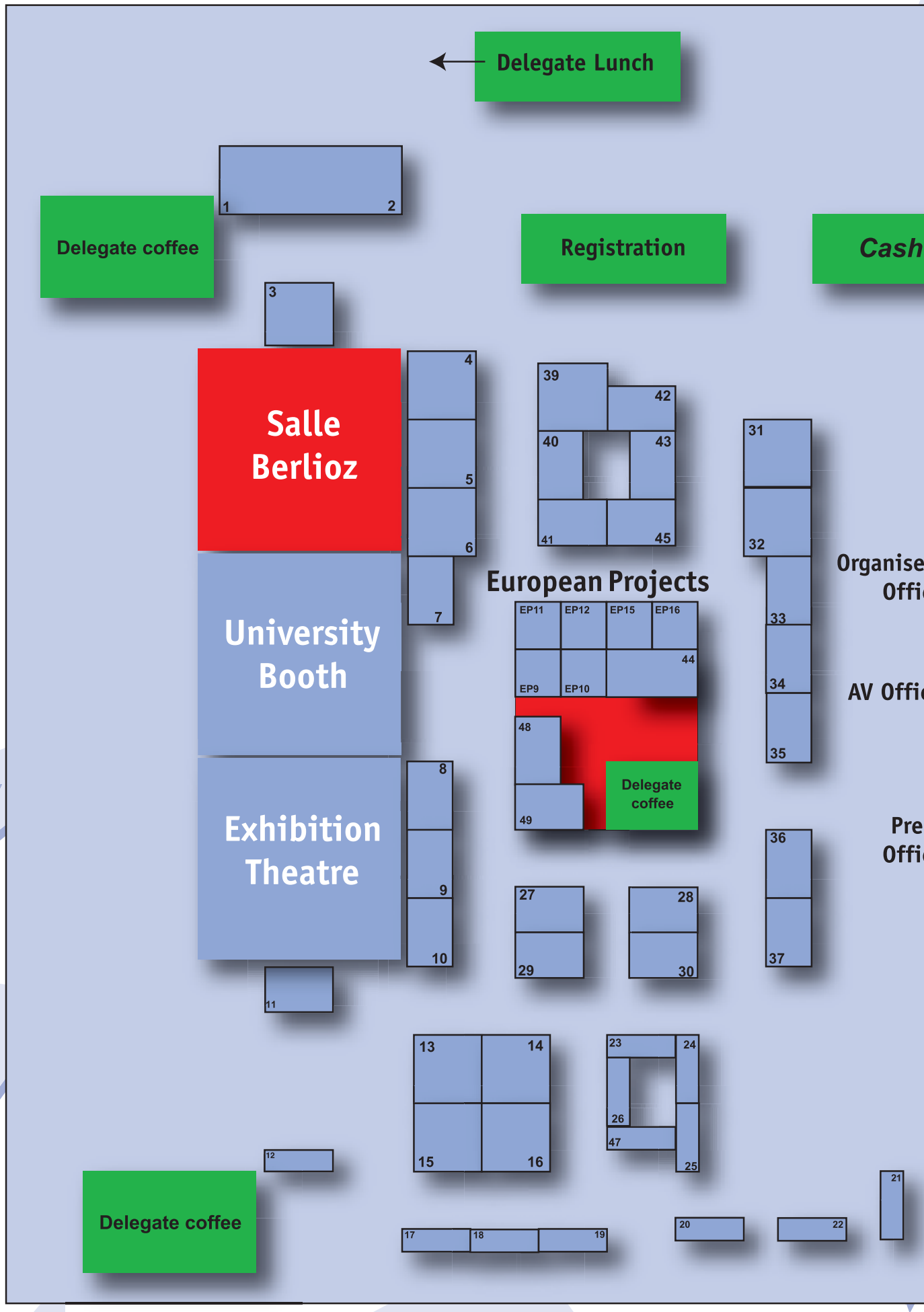
Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can wal karound freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute, one-slide presentation.
To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Sessions will be held in the Salle de Reception area in 30-minute time slots during coffee and exhibition

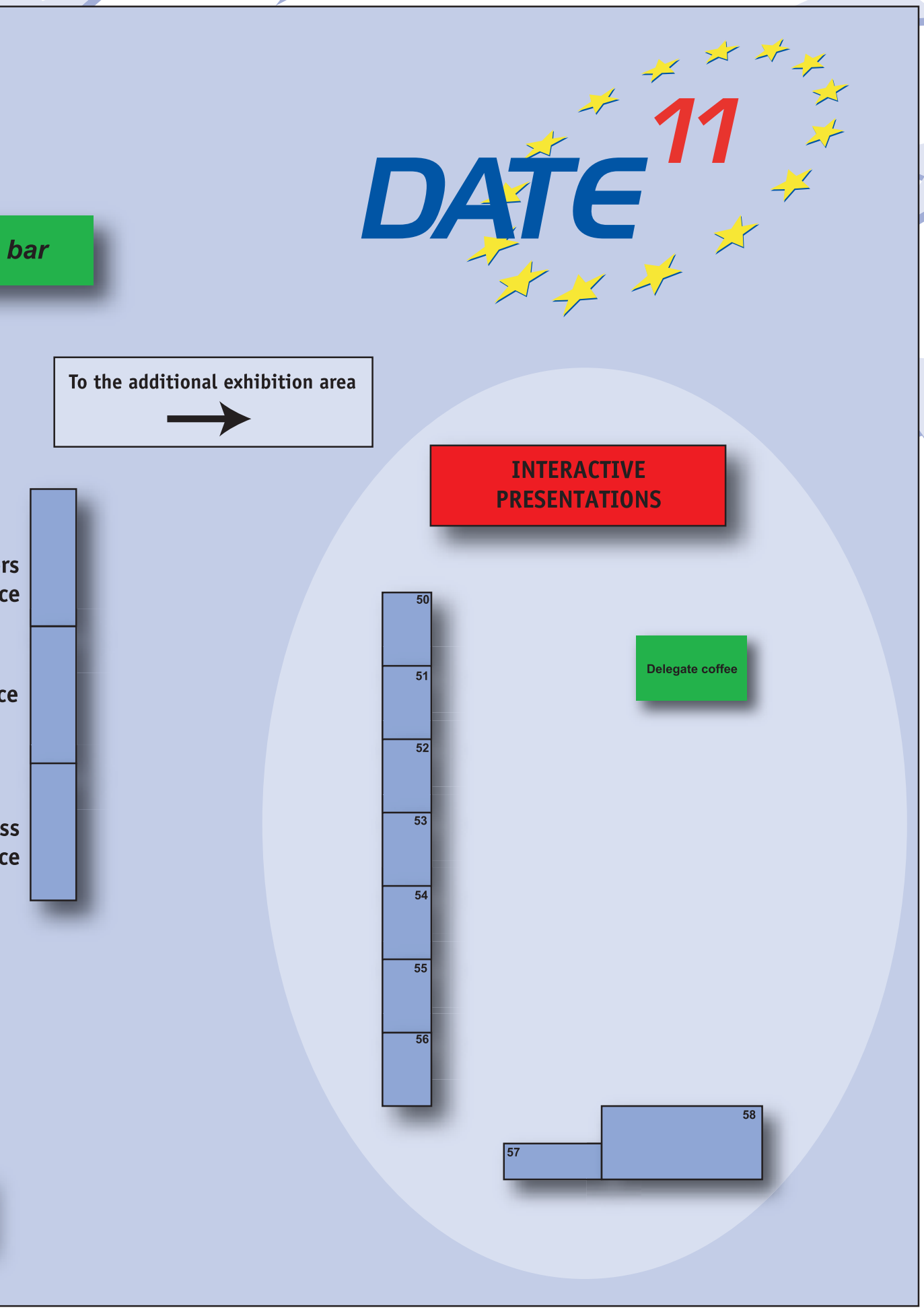
DATE 11

UNIVERSITY BOOTH

DATE 11 will feature the University Booth where system and VLSI CADtools developed in Universities and Research Institutes are demonstrated as well as circuits in their working environment. This provides an alternative and more direct way of communicating CAD research results and displaying working silicon to the interested specialists.The University Booth will be located in the Exhibition Hall and will be furnished with popular workstations. A rotating schedule will operate throughout the three days.


Connecting Corridor
First Floor
Auditorium Dauphine
Salle
Oisans
Press Lounge
AV HQ
Exhibition and Delegate Coffee
Exhibition
Theatre
Salle
Bayard
Salle
Berlioz
Salle Stendhal
Registration
Delegate
Lunch
Main Entrance to
Alpes Congrès
Les
Bans
Meije
7 Laux 4
7 Laux 5
IP Sessions
Delegate Coffee
Salle de Reception
Additional Exhibits
Belle-Etoile
Chartreuse
Espace Pelvoux


Delegate Lunch
Delegate coffee
Registration
Cash
Salle Berlioz
University Booth
Exhibition Theatre
European Projects
EP11
EP12
EP15
EP16
EP9
EP10
Delegate coffee
Delegate coffee
Organise
Offi
AV Offi
Pre
Offi
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
39
40
41
42
43
44
45
47
48
49


DATE 11
bar
To the additional exhibition area
INTERACTIVE PRESENTATIONS
50
51
52
53
54
55
56
Delegate coffee
57
58

Company	Stand
2PARMA (PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures) FP7-ICT-248716	EP15
ACCELONIX	12
ADACSYS	8
ADICSYS	7
AgO Inc	10
ANSYS / Ansoft	6
ApS Brno Ltd., Codasip Division	37
Arteris, Inc.	54
Asygn	53
Atrenta Inc.	27
BLUE PEARL SOFTWARE	28
Chipright	15
CISC Semiconductor Design + Consulting GmbH	43
CMP	32
COCONUT EU project	EP10
Compaan Design BV	44
COMPLEX - COdesing and power Management in PLatform-based design space EXploration	EP16
Concept Engineering GmbH	42
Cortus S.A.	10
CréVinn	15
CST - Computer Simulation Technology AG	56
DEFACTO TECHNOLOGIES	25
DELTA	47
Design Automation Conference (DAC)	16
DOCEA Power	39
Duolog Technologies Ltd	15
EASii-IC	29
EDA Confidential	20
EDALab	48
edXact	23
ElectroniqueS	26
Enterprise Ireland	15
EUROPRACTICE	14
Fractal Technologies	11
GLOBALFOUNDRIES	1 & 2
Gold Standard Simulations Ltd.	30
HiPEAC NoE	EP11
INFINISCALE	40
Infotech	57
IP SOC 11	21
MADNESS - Methods for predictAble Design of heterogeneous Embedded Systems with adaptivity and reliability Support	EP12
Magillem Design Services	33
MICROLOGIC Design Automation	51
Midas	15
MINALOGIC GRENOBLE ISERE	9
MOSIS	35
MunEDA	31
Nano-Tera.ch	45
nSilition	36
N. S. Mangat & Co.	55
Presto Engineering, Inc.	5
ProximusDA	49
R3LOGIC	52
SAME	18
Satin Technologies	41
SELEX Galileo	58
Silansys Semi	15
SPRINGER	3
Tanner EDA	35
Target Compiler Technologies	4
Tech Design Forum	19
The Next Silicon Valley	17
TinnoTek Inc.	50
TowerJazz	13
TRAMS (Terascale Reliable Adaptive Memory Systems) EC FET-IST 248789	EP9
Tyndall's Design Technology Evaluation Group	15
University Booth	46
University of Southampton	22
Veriest Venture	24
XYALIS	34

stand EP15

2PARMA

Contact: Prof. Cristina Silvano
Politecnico di Milano
Dipartimento di Elettronica e Informazione
via Ponzio 34/5, I-20133
Milano Italy
Tel: +39 02 2399 3692
Fax: +39 02 2399 3411
E-Mail: silvano@elet.polimi.it
Website: www.2parma.eu

The 2PARMA project focuses on the definition of a parallel programming model combining component-based and single-instruction multiple-thread approaches, instruction set virtualisation based on portable bytecode, run-time resource management policies and mechanisms as well as design space exploration methodologies for Many-core Computing Fabrics.

The 2PARMA project will demonstrate methodologies, techniques and tools by using innovative hardware platforms provided and developed by the partners, including the "Platform 2012", an early implementation of Many-core Computing Fabric provided by STMicroelectronics.

To ensure a wide range of application scenarios comprising the typical computation-intensive workload of a general-purpose computing system, a set of industrial high performance demanding applications will be used and customized by using the techniques and methodologies developed in 2PARMA project. Applications' architecture, development and integration will leverage in particular from the acknowledged experience of three partners from the Consortium: HHI for Scalable Video Coding application, RWTH for Cognitive Radio, and IMEC for Multi View.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Power & Optimisation
System-Level Design:
Behavioural Modelling & Analysis
Hardware/Software Co-Design
Services:
Design Consultancy
Prototyping
Training
Embedded Software Development:
Compilers
Software/Modelling
Semiconductor IP:
Processor Platforms
Application-Specific IP:
Multimedia Graphics
Wireless Communication

stand 12

ACCELONIX

Contact: Patrick Legenre
PA du Long Buisson, 260 rue Clément Ader
27000 Evreux
FRANCE
Tel: +33 2 32 35 64 80
Fax: +33 2 32 35 00 66
E-Mail: sales@accelonix.com
Website: www.accelonix.fr

ACCELONIX, société indépendante et fournisseur de solutions équipements et logiciels pour l'assemblage et le test des cartes électroniques et microélectronique est reconnue par ses CLIENTS pour son savoir-faire, son expérience et son sens du service. Dans ce cadre, ACCELONIX travaille avec des fournisseurs offrant des solutions originales dans le domaine du test et de la validation de composants.

PRODUCT FINDER

Test:
Design for Test
Design for Manufacture and Yield
Test Automation (ATPG, BIST)
Boundary Scan
Mixed-Signal Test
System Test
Hardware:
FPGA & Reconfigurable Platforms
Development Boards

stand 8

ADACSYS

Contact: Erik Hochapfel
7 rue de la Croix Martre
91120 PALAISEAU
FRANCE
Tel: +33 0 1 69 19 72 72
Fax: +33 0 1 69 19 72 72
E-Mail: erik.hochapfel@adacsys.com
Website: www.adacsys.com

Start verifying your FPGA IP blocs and designs from the very begining of your project... and on your final hardware target. ADACSYS provides innovative hardware accelerated functional verification solutions enabling designers and developers to easily and seamlessly shift from RTL software simulation verification test benches to any FPGA board. Our patented software compilation and runtime flow automatically maps your designs and test benches on any FPGA board. It enables you to quickly verify and certify your FPGA IP blocs and designs on your selected FPGA target.
Our solutions are easy to use and thus have fast learning curves. They reduce your products time to market as well as the risks associated with functional errors and enables you to deliver more robust products.
Today our offer consists of:
A-Soft: the software only solution
For customers who already have their own FPGA board.
A-Full: the complete integrated solution
This turn-key hardware and software product includes A-Soft and an FPGA board, both preconfigured.
A-OD: the platform as a service version of A-Full
This dematerialized and secure product is for customers who want the immediate flexibility of on-demand access in terms of capacity and added performance.

PRODUCT FINDER

ASIC and SOC Design:
Verification
System-Level Design:
Acceleration & Emulation
Test:
Design for Test
System Test
Services:
Prototyping
Training

stand 7

ADICSYS

Contact: Philippe DIEHL
44 rue Cauchy
94110 ARCUEIL
FRANCE
Tel: +33 1 55 01 04 35
E-Mail: contact@adicsys.com
Website: www.adicsys.com

ADICSYS introduces a tool-set enabling an easy and transparent insertion of programmable logic for ASICs, SOCs and silicon IPs in general. The great incentive to implement this flexibility lies in the reduction of risks associated with errors, specification changes and early adopters' challenges. The development and verification time for critical blocks can be minimized while bring-up and debugging capabilities are enhanced.
In today's complex systems, customizable logic can reveal itself as a key element for end user applications.
ADICSYS solutions seamlessly integrate into existing design flows, making them simple and highly cost effective for customers

PRODUCT FINDER

Test:
ASIC and SOC Design:
Synthesis
Services:
Design Consultancy
Semiconductor IP:
Configurable Logic IP

stand 10

AgO Inc

Contact: Dr Roddy Urquhart
Alpha Star Ltd
10 Pitts Lane
Andover
SP10 2HY
UK
Tel: +44 1264 369483
Fax: +44 1264 369483
E-Mail: roddy@alpha-star.eu
Website: www.ago-inc.com

AgO is an EDA company, specialising in analog, RF and mixed-signal design tools. The AnXplorer tool provides feasibility analysis, global optimisation and centering. It is applicable to the design of circuits for wireless communications, automotive, industrial and medical applications.
The feasibility analysis – using DC operating point simulations – identifies the part of the design space where the circuit is stable. Then AnXplorer's multi-algorithm strategy rigorously searches this space, and can find a global optimum in the presence of local optima. Circuit designers can use AnXplorer to rapidly explore the design space to evaluate different circuit topologies. It can also be used to find a robust design solution over a range process, temperature and supply voltage corners. This helps improve yield and enhances the probability of first time silicon success.
When using simulation-based optimisation AnXplorer can work with Eldo, HSpice, MSim and Spectre simulators. It also offers equation-based optimisation.

PRODUCT FINDER

ASIC and SOC Design:
Analogue and Mixed-Signal Design
RF Design

stand 6

ANSYS / Ansoft

Contact: Xavier Le Goaer
Immeuble Central Gare
1 Place Charles de Gaulle
78180 Montigny-le-Bretonneux
Tel: +33 1 30 64 89 90
Fax: +33 1 30 64 89 91
E-Mail: xavier.legoaer@ansys.com
Website: www.ansys.com

ANSYS is a leading developer of high-performance electronic design automation software. The products are designed to simulate high performance electronics designs found in mobile communication and internet devices, broadband networking components and systems, integrated circuits, printed circuit boards, and electromechanical systems.
Siwave™ analyzes entire printed circuit boards and IC packages including packages merged onto boards for complete channel analysis. SIwave extracts frequency dependent circuit models of signal nets and power distribution networks directly from layout databases.
HFSS™ is the industry-standard software for S-parameter extraction and 3-D electromagnetic field simulation of high-frequency and high-speed components. Signal integrity engineers use HFSS software to evaluate signal quality, including transmission path losses, reflection loss due to impedance mismatches, parasitic coupling and radiation.
DesignerSI™
This easy to use design platform integrates rigorous EM analysis with circuit and system simulation in a highly accurate design flow. Engineers using DesignerSI can leverage multiple signal integrity simulation methods such as traditional transient, fast convolution, statistical, and IBIS-AMI analyses in a single user interface.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Package Design
PCB & MCM Design
Services:
Training

stand 37

ApS Brno Ltd., Codasip Division

Contact: Karel Masarik
Bozetechova 2
612 66 Brno
Czech Republic
Tel: +42 0608132875
Fax: +42 0541 211 479
E-Mail: info@codasip.com
Website: www.codasip.com/

The Codasip® team is dedicated helping the customers to develop SoC's using ASIP cores more efficiently while reducing time-to-market significantly. Codasip® was founded in 2005. Codasip® is venture funded by Ministry of Industry of the Czech Republic.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
System-Level Design:
Acceleration & Emulation
Hardware/Software Co-Design
Services:
Design Consultancy
Training
Embedded Software Development:
Compilers
Debuggers
Software/Modelling

stand 54

Arteris, Inc.

Contact: Kurt Shuler
111 W. Evelyn Avenue, Suite 101,
Sunnyvale, CA 94086, USA
Tel: +1 408 470-7300
Fax: +1 408 470-7301
E-Mail: kurt.shuler@arteris.com
Website: www.arteris.com

Arteris provides Network-on-Chip interconnect IP to SoC makers so they can reduce cycle time, increase margins, and easily add functionality. Unlike traditional solutions, Arteris plug-and-play technology is flexible and efficient, allowing designers to optimize for throughput, power, latency and floorplan. Arteris products reduce wire routing congestion and ease timing closure.

PRODUCT FINDER

Semiconductor IP:
Encryption IP
On-Chip Bus Interconnect
On-Chip Debug

stand 53

Asygn

Contact: Andrew Betts
445 rue Lavoisier - F38330 Montbonnot,
France
Tel: +33 4 76 89 80 27
E-Mail: contact@asygn.com
Website: www.asygn.com

Asygn specialises in difficult analog/mixed-signal and RF designs, providing specification and verification solutions in the form of tools and consulting.
If you have issues simulating very large A/MS or RF systems or in dealing with high-Q circuits, then come and see us. If you are fed up with huge simulation runtimes, caused by signals with extremely different time constants, then we may have a solution for you. If you are tackling systems with repeated analog content (such as imagers),

then you should look at our latest software. Asygn software products have been proven to dramatically accelerate simulations on complex analog systems such as mobile phone radios, advanced MEMs sensors and complex imaging arrays. The products integrate seamlessly into standard IC design flows, ensuring design database consistency from system-level down to circuit implementation.
Asygn also offers design services in the above areas. Its extensive track record of successful consulting projects includes custom tool development – a very interesting solution for companies with special challenges.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design
System-Level Design:
Behavioural Modelling & Analysis
Services:
Design Consultancy
Prototyping
Training
Hardware:
FPGA & Reconfigurable Platforms
Development Boards

stand 27

Atrenta Inc.

Contact: Charu Puri
2077 Gateway Place, Suite 300
San Jose
CA 95110
USA
Tel: +1 408 453 3333
Fax: +1 408 453 3322
E-Mail: cpuri@atrenta.com
Website: www.atrenta.com

Atrenta is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools and methodologies to capture design intent, explore implementation alternatives, validate RTL and optimize designs early, before expensive and time-consuming detailed implementation. With over 150 customers, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. Atrenta, Right from the Start!

PRODUCT FINDER

ASIC and SOC Design:
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
System-Level Design:
Physical Analysis
Test:
Design for Test
Services:
Prototyping

stand 28

BLUE PEARL SOFTWARE

Contact: Nichole Fox
4677 Old Ironsides Drive
Suite 430
Santa Clara, CA 95054 USA
Tel: +1 408 9610121
Fax: +1 408 9610125
E-Mail: nichole@bluepearlsoftware.com
Website: www.bluepearlsoftware.com

Blue Pearl Software provides tools which lower design risk, improve the quality of results, save time and reduce the cost of their chip design process.
Blue Pearl Software's RTL Analysis technology automatically checks HDL for compliance with user-selected and user-defined properties, including netlist checks and advanced property checks for CDC.
Blue Pearl's Timing Constraint Generation and Management reads RTL and statically identifies complex false and multicycle paths that occur due to complex control logic. Blue Pearl writes SDC, and writes assertions for testing paths with formal analysis tools. Blue Pearl also merges and compares SDC and migrates constraints up and down the design hierarchy.
Blue Pearl's Timing Constraint Validation reads SDC files and validates them using Blue Pearl's powerful state space search technology. If paths are found invalid Blue Pearl outputs a testbench and patterns that show how invalid paths can be sensitized.
These three technologies have been integrated into a single executable program (The Blue Pearl Software Suite) for fast design analysis, CDC checking, and timing constraint generation, management, and validation.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry

stand 15

Chipright

Contact: James O'Reilly
IIBC
GMIT
Dublin Road
Galway
Ireland
Tel: +353 91 444168
Fax: +353 91 444210
E-Mail: info@chipright.com
Website: www.chipright.com

Accelerate your SystemVerilog migration by 50% with Chipright. Chipright provides products and services for migration from legacy verification languages and environments to the more widely supported IEEE SystemVerilog language. Our products and services can be utilised to speed up the transition timeframe's associated with migration services. • Automation to jumpstart the creation of SystemVerilog test benches and transactors. • Training platform to educate engineers on SystemVerilog verification methods. • Targeted mechanism for migrating legacy verification technology into an advanced SystemVerilog solution. Chipright can convert legacy test benches and BFM's to SystemVerilog test environments and transactors by utilising our extensive verification know-how. Visit our stand today to find out how we can migrate your existing test case libraries and infrastructure to maximise the benefits on offer through using SystemVerilog. We support VMM, OVM and UVM. Visit www.chipright.com or email info@chipright.com

PRODUCT FINDER

ASIC and SOC Design:
Verification
Services:
Design Consultancy
Training

stand 43

CISC Semiconductor Design + Consulting GmbH

Contact: Dr. Markus Pistauer
Lakeside B07
9020 Klagenfurt
AUSTRIA
Tel: +43 463 508 808
Fax: +43 463 508 808-18
E-Mail: backoffice@cisc.at
Website: www.cisc.at

CISC Semiconductor Design+Consulting GmbH is a design and consulting service company for industries developing embedded microelectronic systems with extremely short

SPECIAL FOCUS DAY

Wireless Innovations for Smartphones

WEDNESDAY 16 MARCH

1400 KEYNOTE

Hannu Kauppinen, Director,
Head of Radio Systems Laboratory,
Nokia Research Center, Finland

Time-To-Market cycles. Our core competences are: System design, modeling, simulation, verification and optimization of heterogeneous embedded microelectronic systems with a particular focus on Automotive and RFID systems.
Our customers are represented in the Semiconductor, Automotive and RFID industry. CISC Semiconductor was founded in 1999 and is 100% privately owned. The company is managed by an international team of highest skilled experts. Our main office is situated in Klagenfurt, Austria (close to well known Wörthersee) right in the heart of the Alpen-Adria-Region. We are proud to be able to conduct our international business from this part of the world and also enjoy our life with our families and friends within this beautiful nature. Being an independent company, CISC furthermore is able to provide non CAD/CAE market driven technology for individual customer solutions. CISC offers commercial tools and techniques for simulation based system development of embedded microelectronic systems including RFID systems.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
System-Level Design:
Behavioural Modelling & Analysis
Hardware/Software Co-Design
Test:
System Test
Services:
Design Consultancy
Prototyping
Embedded Software Development:
Software/Modelling
Hardware:
Development Boards

stand 32

CMP

Contact: Bernard Courtois
46 avenue Felix Viallet
38031 Grenoble
France
Tel: +33 476574617
Fax: +33 476473814
E-Mail: cmp@imag.fr
Website: http://cmp.imag.fr

CMP is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 1000 Institutions from 60 countries have been served, more than 5300 projects have been prototyped through 600 manufacturing runs, and more than 55 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, CMOS-Opto from STMicroelectronics and Austriamicrosystems, 20 nm FDSOI from CEA-LETI, 3D-IC from TEZZARON/GLOBALFOUNDRIES, and 150nm pHEMT GaAs from TRIQUINT. ARM IP cores are available on 130nm µ and 65 nm CMOS. MEMS are available on various processes: specific MEMS technologies (PolyMUMPS, SOIMUMPS, MetalMUMPS from MEMSCAP, SUMMIT from SANDIA).
Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ceramic packages.
CAD software (tools for PCs, ARM suite of tools, ...) are also proposed.

PRODUCT FINDER

Services:
Prototyping
Foundry & Manufacturing

stand EP10

COCONUT EU project

Contact: Graziano Pravadelli
Dipartimento di Informatica -
Università di Verona
Strada le Grazie 15, 37134 Verona, Italy
Tel: +39 045 8027081
Fax: +39 045 8027068
E-Mail: graziano.pravadelli@univr.it
Website: www.coconut-project.eu

The COCONUT project is intended to propose a modelling and verification flow to enhance and speed-up embedded platform's design and configuration of mixed continuous/discrete models. In this context, the scientific and technological objective of the COCONUT project consists of developing a systematic methodology and a set of tools to integrate correct-by-construction refinement/abstraction and post-refinement verification methods into a platform-based design flow.
At the booth, COCONUT partners present the project main flow, demo of tools, and relevant results.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Verification
System-Level Design:
Behavioural Modelling & Analysis
Hardware/Software Co-Design

stand 44

Compaan Design BV

Contact: John van Brummen
De Ruyterkade 113
1011 AB Amsterdam
The Netherlands
Tel: +31 20 5216686
Fax: +31 20 6750389
E-Mail: j.van.brummen@compaandesign.com
Website: www.compaandesign.com

Compaan Design develops technology for hotspot parallelization of legacy/certified ISO C applications. It offers innovative products that reliably compile and scale to state-of-the-art silicon with billions of transistors such as x86 multicore, MPSoC and FPGA.
The Compaan Design workflow guides step-by-step parallelization towards improved energy efficiency and computational throughput. Parallelism is exploited for streaming data and increased architecture utilization. Exact dataflow analysis guarantees correctness and robustness of application execution. Code generation is heterogeneous and supports flexible HW/SW codesign.
It is a perfect solution for today's MPSoCs composed of DSPs, FPGAs and microprocessors. It easily retargets to customized processors and IP blocks.

PRODUCT FINDER

System-Level Design:
Acceleration & Emulation
Hardware/Software Co-Design
Embedded Software Development:
Compilers
Software/Modelling
Hardware:
FPGA & Reconfigurable Platforms
Semiconductor IP:
Embedded FPGA
Application-Specific IP:
Data Communication
Digital Signal Processing
Telecommunication

OPENING PLENARY

Biologically-inspired massively-parallel architectures – computing beyond a million processors

S Furber,
ICL Professor of Computer Engineering,
School of Computer Science, Manchester U, UK

How technology R&D leadership brings a competitive advantage in the fields of multimedia convergence and power applications

Philippe Magarshack,
Group Vice-President, Technology R&D -
General Manager, Central CAD and Design
Solutions, STMicroelectronics, France

stand EP16

COMPLEX - COdesing and power Management in PLatform-based design space EXploration

Contact: Adam Morawiec
ECSI, Electronic Chips & Systems design Initiative
Parc Equation
2 avenue de Vignate
38610 Gières
France
OFFIS e.V.
Escherweg 2
Oldenburg
26131
Germany
Telephone:+49 441 97 22 0
Tel: ECSI +33 476 63 4934
Fax: ECSI +33 958 08 2413
E-Mail: adam.morawiec@ecsi.org
Website: http://complex.offis.de/

The primary objective of the COMPLEX (COdesing and power Management in PLatform-based design space EXploration) European Integrated Project is to develop an innovative, highly efficient and productive design methodology and a holistic framework for iteratively exploring the design space of embedded HW/SW systems. COMPLEX will focus on early, fast yet accurate platform-based design space exploration at the system level.
The COMPLEX consortium develops a new design environment for platform-based design-space exploration offering developers of next-generation mobile embedded systems a highly efficient design methodology and tool chain. The integrated environment allows iterative exploration and refinement of advanced applications to meet market requirements. The design technology in particular enables fast simulation and assessment of the platform at Electronic System Level (ESL) with up to bus-cycle accuracy at the earliest instant in the design cycle.
Partners: OFFIS (DE), STMicroelectronics (IT), STMicroelectronics (CN), Thales Communications (FR), GMV (ES), Synopsys (BE), ChipVision (DE), EDALab (IT), Magillem Design Services (FR), Politecnico di Milano (IT), Universidad de Cantabria (ES), Politecnico di Torino (IT), IMEC (BE), ECSI (FR)

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Power & Optimisation
System-Level Design:
Behavioural Modelling & Analysis
Hardware/Software Co-Design
Embedded Software Development:
Compilers
Real Time Operating Systems
Software/Modelling

stand 42

Concept Engineering GmbH

Contact: Gerhard Angst
Boetzinger Str. 29
79111 Freiburg
Germany
Tel: +49 761 470940
Fax: +49 761 4709429
E-Mail: info@concept.de
Website: www.concept.de

Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers, FPGA and IC designers.
Nlview WidgetsTM – a family of schematic generation and visualization engines (Tcl/TK, MFC, Qt, Java, Perl/Tk, wxWidgets) that can be easily integrated into EDA tools.
RTLVisionTM PRO – a graphical debugger for SystemsVerilog, Verilog and VHDL based designs.
GateVision® PRO – a customizable debugger for Verilog, LEF/DEF and EDIF based designs.
SpiceVision® PRO – a customizable debugger for SPICE based designs.
SGvisionTM PRO – a customizable mixed-mode debugger (SPICE and Verilog).

PRODUCT FINDER

ASIC and SOC Design:
Verification
Analogue and Mixed-Signal Design
Test:
Mixed-Signal Test

stand 10

Cortus S.A

Contact: roddy.urquhart@cortus.com
Cortus S.A.
Le Génésis
97 rue de Freyr
34000 Montpellier
France
Tel: +44 1264 369483
Fax: +44 1264 369483
E-Mail: roddy.urquhart@cortus.com
Website: www.cortus.com

Cortus is the technology leader in ultra low power, compact 32-bit microcontroller IP cores. The APS3 combines a power consumption of 22 µW/DMIPS (TSMC 130 nm) with processing power similar to an ARM9. Yet the core itself is no larger than the 8051 – making it a natural upgrade choice for 8-bit/16-bit core users – and is the smallest available core capable of running µCLinux. Microprocessor Report crowned the APS3 the "King of Lilliput".
Software development with C/C++ is supported by a complete toolchain and Eclipse-based IDE. A rich ecosystem of development tools and RTOS is available.
A building block approach ensures that the APS3 is an ideal processor for a very wide range of requirements spanning low end, ultra low cost applications to high end, multi-core systems with multiple coherent caches.
The core is well proven in many high volume applications in technologies ranging from 32nm to 180nm.

PRODUCT FINDER

Services:
Prototyping
Training
Embedded Software Development:
Compilers
Debuggers
Software/Modelling
Semiconductor IP:
Analogue & Mixed Signal IP
CPUs & Controllers
Encryption IP
Physical Libraries
Processor Platforms
Application-Specific IP:
Analogue & Mixed Signal IP
Digital Signal Processing
Security
Wireless Communication

stand 15

CréVinn

Contact: Tadhg Creedon
CréVinn Teoranta
Manor House
Baile an tSagairt
An Spideal
Ireland
Tel: +353 91-558090
Fax: +353-91-558060
E-Mail: Tadhg_creedon@crevinn.com
Website: www.crevinn.com

CréVinn is a leading Silicon System Design Consultancy company, with Design Centres in Galway and Dublin, Ireland. We work with key partners to develop innovative technology in the networking, computing, automotive and industrial markets. In addition, we are engaged in Silicon IP Core and Product Development in the networking and storage fields.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Verification
System-Level Design:
Behavioural Modelling & Analysis
Services:
Design Consultancy
Prototyping
Application-Specific IP:
Data Communication
Digital Signal Processing
Networking
Security
Telecommunication
Wireless Communication

stand 56

CST Computer Simulation Technology AG

Contact: Jerome Mollet
Bad Nauheimer Str. 19
64289 Darmstadt
Germany
Tel: +49 6151 7303 0
Fax: +49 6151 7303 100
E-Mail: info@cst.com
Website: www.cst.com

CST develops and markets high performance software for the simulation of electromagnetic fields in all frequency bands. Its products allow you to characterize, design and optimize electromagnetic devices all before going into the lab or measurement chamber. This can help save substantial costs especially for new or cutting edge products, and also reduces design risk and improves overall performance and profitability.
Its success is based on the implementation of leading edge technology in a user-friendly interface. Furthermore, CST's "complete technology" complements its market and technology leading time domain solver (CST MICROWAVE STUDIO®), thus offering unparalleled speed, accuracy and versatility for all applications.
CST's customers operate in industries as diverse as Telecommunications, Defense, Automotive, Electronics, and Medical Equipment, and include market leaders such as IBM, Intel, Mitsubishi, Samsung, and Siemens. CST markets its products worldwide through a network of distribution and support centers which also provide comprehensive customer support and training.
More information at http://www.cst.com.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Package Design
PCB & MCM Design
Test:
Design for Test
Embedded Software Development:
Software/Modelling

stand 25

DEFACTO TECHNOLOGIES

Contact: Chouki Aktouf
167 Rue De Mayoussard
38430 Moirans
France
Tel: +33 476 668330
Fax: +33 476 910067
E-Mail: chouki.aktouf@defactotech.com
Website: www.defactotech.com

DeFacTo enables designers to complete planning, analysis and implementation of integrated circuit test logic before synthesis by delivering a high quality suite of DFT tools working at the register transfer level (RTL).

PRODUCT FINDER

Test:
Design for Test
Test Automation (ATPG, BIST)
Services:
IP e-commerce & Exchange
Semiconductor IP:
Test IP

stand 47

DELTA

Contact: Mette Brunbjerg Olesen
Venlighedsvej 4
2970 Hoersholm
Denmark
Tel: +45 721 94000
Fax: +45 721 94001
E-Mail: asic@delta.dk
Website: www.asic.madebydelta.com

Are you looking for a complete ASIC supply chain solution?
DELTA Microelectronics is the European leader in providing the semiconductor industry. We give our customers a competitive edge in bringing products to market quickly and enabling a predictable path from IC development via testing and mass production. We offer supply chain management consisting of ASIC development, fabrication, packaging, testing, storage and shipping of ICs - to help address the key challenges fabless IC vendors' face today, from prototypes to mass production. Semiconductor vendors achieve faster time-to-market of smaller, more robust, more profitable semiconductor products by utilising DELTA's turn-key solutions and professional services. DELTA's experienced ASIC design team is specialised in payment systems, RFID, sensor interfaces and opto chips.
Flexibility, quality and competitiveness – DELTA offers solutions at any part of the ASIC development and production process to allow the customer to get the most cost effective combination of services.
Get access to European and Far Eastern wafer and packaging facilities via DELTA's volume purchasing power to obtain the best possible prices.
DELTA is established 70 years ago and is headquartered in Copenhagen, Denmark.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
System-Level Design:
Behavioural Modelling & Analysis
Package Design
Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Services:
Design Consultancy
Prototyping
Foundry & Manufacturing
Hardware:
FPGA & Reconfigurable Platforms
Application-Specific IP:
Analogue & Mixed Signal IP
Data Communication
Digital Signal Processing
Security
Telecommunication
Wireless Communication

stand 16

Design Automation Conference (DAC)

Contact: Susie Horn
MP Associates
1721 Boxelder Street, #107
Louisville, CO 80027
Tel: +1 303 530-4333
Fax: +1 303 530-4334
E-Mail: Susie@dac.com
Website: www.dac.com

The Design Automation Conference (DAC) is the world's leading technical conference and tradeshow on electronic design and design automation. DAC is where the IC Design and EDA ecosystem learns, networks, and conducts business. DAC features hundreds technical sessions, panels, keynotes, tutorials, workshops and events covering the latest in design methodologies, embedded software and systems and EDA tool developments. The exhibition offers booths and suites from over 200 of the leading EDA, silicon, IP, embedded and design services providers. 48th Design Automation Conference, June 5-10, 2011 in San Diego, CA

stand 39

DOCEA Power

Contact: Ridha HAMZA,
Marketing and Sales Director
166 B Rue du Rocher de Lorzier
38430 Moirans
FRANCE
Tel: +33 0 427 85 82 62
Fax: +33 0 488 68 11 22
E-Mail: ridha.hamza@doceapower.com
Website: www.doceapower.com

DOCEA Power develops and markets system-level tools for modeling and optimizing power/thermal behavior of whole electronics systems. DOCEA's Aceplorer software integrates a consistent power data management methodology for capturing and simulating power behavior. The "separation of concerns" approach makes power models usable across the teams and the design flow from system level to silicon measurements. The Aceplorer innovative platform is the solution for early power estimation, architecture exploration, use case profiling, package selection and other technology choices that impact specification. Dealing with power and/or thermal issues with Aceplorer at system level is fast, secure and efficient.
As a service, DOCEA Power generates SPICE-compliant compact thermal models of ICs, SoCs, SiPs or on-board systems. Dynamic thermal simulations get ultra-fast, while accuracy is kept under control.
DOCEA technology has been adopted by world's largest semiconductor companies.

PRODUCT FINDER

ASIC and SOC Design:
Power & Optimisation
System-Level Design:
Behavioural Modelling & Analysis
Test:
System Test
Services:
Training
Embedded Software Development:
Software/Modelling

stand 15

Duolog Technologies Ltd

Contact: Fearghal Hannaway
Concourse Building (5th Floor)
Beacon Court
Sandyford
Dublin 18
Ireland
Tel: +353 1 2178425
E-Mail: Fearghal.hannaway@duolog.com
Website: www.duolog.com

Duolog Technologies is a pioneering developer of EDA tools that enable the rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates platform is a hub for chip integration from IP register to Chip pin. It allows the capture of standardized views of IP-level and chip-level designs, validates the data to ensure correctness and generates source views for different teams, including hardware and software views, design and verification views, ESL and implementation views. Socrates supports current and emerging standards such as IP-XACT, RAL, OVM and UVM. Socrates is delivering significant productivity improvements to Duolog's customers including enhanced inter-team communication, extensive bug elimination and major design cycle reductions. Founded in 1999, Duolog Technologies is headquartered in Dublin, Ireland with development centres in Galway, Ireland and Budapest, Hungary. Duolog also has sales and support offices across Europe, US and Asia.

SPECIAL FOCUS DAY

SMART ENERGY AT ST

KEYNOTE – Thursday, March 17th, 13.30

Carmelo Papa, Executive VP Industrial and Multisegment, STMicroelectronics, IT

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Synthesis
Verification
System-Level Design:
Hardware/Software Co-Design
Test:
Design for Test
Boundary Scan
Services:
Design Consultancy
Data Management and Collaboration
Semiconductor IP:
Test IP
Verification IO

stand 29

EASii-IC

Contact: Francois CERISIER
90, avenue Léon Blum
BP 2612
38036 Grenoble Cedex 2
FRANCE
Tel: +33 4 56 580 580
Fax: +33 4 56 580 599
E-Mail: grenoble@easii-ic.com
Website: www.easii-ic.com

Strong of our experience in IC, electronics and software services, we develop solutions for radiation tests (ASER) and validation (EASii-Board).
We also deliver EDA expert services and EDA solutions.
ASER:
Soft Error Test service is a complete solution to radiation effects characterization of space, automotive or consumer products around the world.
EASii-Board:
A low cost logical pattern generator and analyzer bridging the gap between design and validation, allowing you to build easy and efficient validation platforms.
EDA Solutions:
- Be-Spice: Your browser and visualizer for spice netlists and backannotated simulation results.
- IDesignSpec (Agnisys): Register Automation and Management allowing easy design and verification automation of register features.
- IVerifySpec (Agnisys): Presents a complete status of the verification project. It also provides a collaborative tool for distributed verification teams that improves productivity and quality.
EDA Services:
State of the art methodology consulting, IP and VIP development on partner tools: Agnisys, Breker, Jasper, Mentor.
On-Demand EDA support.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Verification
Analogue and Mixed-Signal Design
System-Level Design:
Physical Analysis
Test:
Silicon Validation
System Test
Services:
Design Consultancy
Prototyping
Data Management and Collaboration
Training
Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Semiconductor IP:
Analogue & Mixed Signal IP
Application-Specific IP:
Analogue & Mixed Signal IP

stand 20

EDA Confidential

Contact: Peggy Aycinena
San Mateo, CA
94402-2241
U.S.A.
Tel: +1 650 579 7952
Fax: +1 650 579 7952
E-Mail: peggy@aycinena.com
Website: www.aycinena.com

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes "Recipes", Freddy Santamaria's "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

stand 48

EDALab

Contact: Walter Vendraminetto
Strada Le Grazie, 15
37134 - Verona (VR)
ITALY
Tel: +39 045 8027062
Fax: +39 045 8027062
E-Mail: info@edalab.it
Website: www.edalab.it

EDALab is a business reality located in Verona, in the north of Italy, which addresses issues of **technological innovation in the field of networked embedded systems.** It has a workforce of about 15 people including partners, employees and external collaborators, united by a common passion for IT and emerging technologies.
The young age and the personal motivation are at the base of the company's success in being proactive and flexible.
Our activity is focused on **embedded system design both from the research point of view and from a production standpoint.** The coexistence of these two souls is part of the EDALab mission, which serves as innovation driver for its customers.
Related links: HIFSuite Tools -> http://hifsuite.edalab.it

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Verification
System-Level Design:
Behavioural Modelling & Analysis
Hardware/Software Co-Design
Test:
Logic Analysis
Test Automation (ATPG, BIST)
System Test
Services:
Prototyping
Embedded Software Development:
Compilers
Real Time Operating Systems
Software/Modelling
Application-Specific IP:
Data Communication
Networking
Telecommunication
Wireless Communication

stand 23

edXact

Contact: Delphine Billon
Parc Work Center - Bât A
Route des Bois
38500 Voiron – France
Tel: +33 0 4 76 66 89 80
Fax: +33 0 4 76 67 36 99
E-Mail: billon@edxact.com
Website: www.edxact.com

EDXACT proposes software that helps to substantially raise the efficiency of postlayout simulation and analysis flows.
Current offerings include:
JIVARO - netlist reduction platform, integrated into any design flow, several interfaces, many references.
Used in production for memory, mixed-signal, analog, RF flows. Timing. Speeding up simulation time, increasing accuracy, reducing memory footprint. Industry-leading netlist reduction.
COMANCHE - parasitics analysis platform. Allows to quickly analyze interconnect parasitics in order to pinpoint problems. Allows to estimate timing, accurately compare different extracted netlists. Several interfaces.

PRODUCT FINDER

ASIC and SOC Design:
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
RF Design

stand 26

ElectroniqueS

Contact: Daniel Haussman
Tel: +33 01 71 18 54 40
Fax: +33 01 71 18 53 01
E-Mail: dhaussmann@nextregie.fr
Website: www.electroniques.biz

ElectroniqueS the reference monthly for decision makers and engineers in the electronics sector
Circulation of 10,000 copies
www.electroniques.biz, the electronic professional's web site
Daily Newsletter, the day's essential news about our industry's major sectors
Sent to more than 26,000 free subscribers
Weekly newsletter, the newsletter that summarizes the previous 5 daily newsletters main topic
Sent to more than 23,000 free subscribers
Vertical newsletter, 3 subjects: Automotive / Mil-Aero / Medical
5 mailings a year (each 2 in 3 months)

stand 15

Enterprise Ireland

Contact: Paul McCloskey
Enterprise Ireland, Industry House, Rossa Avenue, Bishopstown, Cork
Tel: +353 21 4800227
Fax: +353 21 4800271
E-Mail: paul.mcloskey@enterprise-ireland.com
Website: www.enterprise-ireland.com

Chipright, Crevinn Teoranta, Duolog , Silansys and Tyndall are all members MIDAS Ireland.
Enterprise Ireland is the government organisation responsible for the development and growth of Irish enterprises in world markets. It works in partnership with Irish enterprises to help them start, grow, innovate and win export sales on global markets.
MIDAS Ireland (Microelectronic Industry Design Association) is a national cluster consisting of microelectronics design companies and third level institutions in Ireland. The membership currently consists of 7 multinational companies, 18 indigenous companies and 17 academic members representing all the courses in Ireland that produce electronic engineering graduates. Its aim is to promote the growth of

microelectronics in Ireland through collaboration in research, training and education. Enterprise Ireland is an associate member of MIDAS.

stand 14

EUROPRACTICE

Contact: Carl Das
Kapeldreef 75
B-3001 Heverlee
Belgium
Tel: +32 16 281 248
Fax: +32 16 281 584
E-Mail: Carl.Das@imec.be
Website: www.europractice-ic.com

The EUROPRACTICE IC service offers low cost and easy access to ASIC prototype and small volume fabrication.
The service is offered by IMEC (B) and FhG/IIS (D).
Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW (Multi Project Wafer) runs whereby many designs from different customers are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemi, austriamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up to more than 5000 wafers per year per ASIC.

PRODUCT FINDER

ASIC and SOC Design:
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Test:
Design for Test
Test Automation (ATPG, BIST)
Boundary Scan
Mixed-Signal Test
System Test
Services:
Prototyping
Foundry & Manufacturing
Semiconductor IP:
Physical Libraries

stand 11

Fractal Technologies

Contact: Rene Donkers
US office, San Carlos, California, USA
Europe Office, Eindhoven, the Netherlands
Tel: +31 641539004
Fax: +31 847503816
E-Mail: info@fract-tech.com
Website: www.fract-tech.com

The scope of Fractal Technologies is to check consistency and validate all different dataformats used in your design and subsequently improve the Quality of your Standard Cell Libraries, IO's and IP's
FRACTAL TECHNOLOGIES
Your partner to: check consistency and validate all different dataformats and subsequently improve the Quality of your Standard Cell Libraries, IO's and IP's

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Verification
Services:
Design Consultancy

stands 1&2

GLOBALFOUNDRIES

Contact: Simone Wurm
Dresden
Germany
Tel: +49 - 351 - 277 1018
Fax: +49 - 351 - 277 91018
E-Mail: simone.wurm@globalfoundries.com
Website: www.globalfoundries.com

GLOBALFOUNDRIES is the world's first full-service semiconductor foundry with a truly global manufacturing and technology footprint. Launched in March 2009 through a partnership between AMD [NYSE: AMD] and the Advanced Technology Investment Company (ATIC), GLOBALFOUNDRIES provides a unique combination of advanced technology, manufacturing excellence and global operations. With the integration of Chartered in January 2010, GLOBALFOUNDRIES significantly expanded its capacity and ability to provide best-in-class foundry services from mainstream to the leading edge.
GLOBALFOUNDRIES is headquartered in Silicon Valley with manufacturing operations in Singapore, Germany, and a new leading-edge fab under construction in Saratoga County, New York. These sites are supported by a global network of R&D, design enablement, and customer support in Singapore, China, Taiwan, Japan, the United States, Germany, and the United Kingdom.
For more information on GLOBALFOUNDRIES, visit http://www.globalfoundries.com.

stand 30

Gold Standard Simulations Ltd

Contact: Campbell Millar
The Rankine Building,
Oakfield Avenue,
Glasgow,
G12 8LT
UK
Tel: +44 141 330 4790
Fax: +44 141 330 4907
E-Mail: info@goldstandardsimulations.com
Website: www.goldstandardsimulations.com

Gold Standard Simulations (GSS) is the world leader in the simulation of statistical variability in nano-CMOS devices. The services we offer include the physical simulation of statistical variability, statistical compact model extraction and statistical circuit simulation using 'push button' cluster-based technology.

PRODUCT FINDER

ASIC and SOC Design:
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Services:
Training
Embedded Software Development:
Software/Modelling

stand EP11

HiPEAC NoE

Contact: Koen De Bosschere
Universiteit GENT - ELIS,
9000 GENT, BELGIUM
Tel: +32 9 264 42 58
Fax: +32 9 264 35 94
E-Mail: Koen.DeBosschere@elis.ugent.be
Website: www.hipeac.net

HiPEAC is a Network of Excellence on High Performance and Embedded Architecture and Compilation. It gathers over 150 leading European academic and industrial computing-system researchers in one virtual center of excellence with the aim of coordinating their research, improving their mobility and collaborations, increasing their visibility. The network consists of nine research clusters that look into on-chip multi-cores technology and customisation, leading to heterogeneous multi-core systems. HiPEAC organizes several large networking events in Europe: the ACACES Summer school, Computing Systems Weeks (those are co-located with industrial workshops), the HiPEAC conference. Additionally HiPEAC journals, newsletters and roadmaps are published on the regular basis.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Acceleration & Emulation
Hardware/Software Co-Design
Test:
Test Automation (ATPG, BIST)
Services:
Data Management and Collaboration
Embedded Software Development:
Compilers
Real Time Operating Systems
Debuggers
Software/Modelling
Hardware:
FPGA & Reconfigurable Platforms
Semiconductor IP:
Embedded FPGA
Embedded Software IP
On-Chip Bus Interconnect
Application-Specific IP:
Digital Signal Processing
Multimedia Graphics
Networking
Telecommunication
Wireless Communication

stand 40

INFINISCALE

Contact: Stephane FIORILLO
186 chemin de l'étoile
38330 Montbonnot
France
Tel: +33 04 76 51 25 27
Fax: +33 04 76 51 20 46
E-Mail: stephane.fiorillo@infiniscale.com
Website: www.infiniscale.com

About Infiniscale
Variation-aware risk management solutions
Infiniscale provides a unique variation-aware custom IC design solutions dedicated to analysis and optimization of performances and parametric yield for analog and mixed-signal designs. Infiniscale Lysis flow enables variation-aware design methods that can accurately and promptly estimate the risks into variation sensitive devices. Then Lysis can help the designer reducing or possibly removing these risks.
With Lysis, the designer is able to run a million MC in seconds, to visualize PVT influence on performances in real-time, and to optimize parametric yield in an hour.
Lysis innovative approach to variation-aware design is compatible with all the existing design flows, and fully integrated with the industry-leading EDA tools. Infiniscale works with several major semiconductor companies in the area of power management, memories and mixed-signal designs.
Infiniscale's solutions enable designers delivering products on time, while maximizing robustness and yield.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation

stand 57

Infotech

Contact: Abilash Reddy Gaddam
Infotech Enterprises GmbH
Mollenbachstraße 37
71229 Leonberg
Germany
Tel: +49 (0) 7152 9452-0
Fax: +49 (0) 7152 9452-90
E-Mail: info@infotechsw.de
Website: www.infotech-enterprises.com

Infotech Enterprises provides leading-edge engineering solutions to major organizations worldwide. With Global Headquarters in Hyderabad, India, Infotech has 8,000+ engineers across 30 global locations and has generated consolidated revenues of US $201 Million for the fiscal year ending March 2010. Infotech provides concept to silicon and system prototype solutions for ASIC/FPGA Engineering and Embedded Software Development. With over 12 years impeccable track record of "first-pass silicon success" and "on-time delivery" across 200+ ASIC tapeouts, we not only help our customers meet their current design requirements, but also provide technology road maps and innovative solutions for future design trends.
Primary Service Offerings:
•ASIC and SOC Design
•Embedded Software Design
•FPGA & Board Design
Key Highlights:
•12 years track record of "first pass silicon success" across 200+ ASIC tapeouts
•Delivery center based out of San Jose, U.S. : Access to high-end electronics talent from the Silicon Valley
•Expertise in technology nodes down to 28nm and as many as 100 million gates
•Deep understanding of ARM/MIPS/PowerPC-based SOCs with a strong grasp of memory and connectivity technologies
•Extensive background in multimedia (audio, video, speech and image) codecs standards and frameworks

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
Services:
Design Consultancy
Embedded Software Development:
Real Time Operating Systems
Hardware:
FPGA & Reconfigurable Platforms
Development Boards

stand 21

IP SOC 11

Contact: Gabriele Saucier
IP SOC 11
Design And Reuse SA
12 rue Ampere
38016 Grenoble
FRANCE
Tel: +33 476 21 31 02
Fax: +33 476 49 00 52
E-Mail: info@design-reuse.com
Website: www.design-reuse.com

IP - SoC 2011 will be the 20th edition of the working conference on hot topics in the design world, focusing for the past 9 years on IP-based SoC design and held in Grenoble,organized by Design And Reuse . Over the years, IPs have become Subsystems or Platforms and thus as a natural applicative extension.IP-SoC will definitively include a strong Embedded Systems track addressing a continuous technical spectrum from IP to SoC to Embedded System.

stand EP12

MADNESS

Contact: Prof. Luigi Raffo
DIEE - Department of Electric and Electronic Engineering
University of Cagliari
Piazza d'Armi - 09123 CAGLIARI (Italy)
Tel: +390706755765
Fax: +390706755782
E-Mail: request@madnessproject.org
Website: www.madnessproject.org

The main goal of the project is to define innovative methodologies for system-level design, able to guide designers and researchers to the optimal composition of embedded MPSoC architecture, according to the requirements and the features of a given target application field. The proposed approach will tackle the new challenges,

related to both architecture and design methodologies, arising with the technology scaling, the system reliability and the ever-growing computational needs of modern applications.
The proposed methodologies will extend the classic concept of design space exploration to:
* Improve design predictability, bridging the so called "implementation gap", i.e. the gap between the results that can be predicted during the system-level design phase and those eventually obtained after the on-silicon implementation.
* Consider, in addition to traditional metrics (such as cost, performance and power consumption), continued availability of service, taking into account fault resilience as one of the optimization factors to be satisfied.
* Support adaptive runtime management of the architecture, considering, while tailoring the architecture, new metrics posed by novel dynamic strategies and advanced support for communication issues that will be defined.

stand 33

Magillem Design Services

Contact: Lamia Lakehal
4, rue de la Pierre Levée
75011
Paris France
Tel: +33 0 1 40 21 35 50
Fax: +33 0 1 53 36 75 08
E-Mail: lakehal@magillem.com
Website: www.magillem.com

Magillem provides to customers in the electronic industry tools and services that drastically reduce the global cost of complex design.
Magillem has developed an easy to use, state of the art platform solution to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SOC. Main benefits include:
* Maximizing Design and IP Re-use
* Using a virtual platform to configure their system and IPs
* Controlling the Design Flow
* Exploring their Design Flow architecture and optimizing it
* Improving their independence from CAD tools vendors
* Improving interoperability, communication
* Benefiting from better user interfaces to raise productivity
* Relying on worldwide adopted standards
Our Motto:
Methodology tools should adapt to the trends in SoC design and help streamline the design flows without disrupting existing processes

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
System-Level Design:
Hardware/Software Co-Design
Package Design
Services:
Design Consultancy
Data Management and Collaboration
Training
Semiconductor IP:
Memory IP

stand 51

MICROLOGIC Design Automation

Contact: Christophe Bianchi
157 Yaffo Street
AMOT Building
Haifa 35251
Israel
Tel: +972-4-8538835
Fax: +972-4-8527785
E-Mail: info@micrologic-da.com
Website: www.micrologic-da.com

Micrologic interactive nanoToolBox solutions accelerate the signoff of complex deep nanometer designs with:
· Faster time to market
· Improved performance
· Enhanced reliability
· Lower costs
Micrologic's nanoToolBox is a plugin suite of tools for Virtuoso™, consisting of complementary Design Rule Verification (DRC), Reliability Verification (RV) and Layout Versus Schematic (LVS) checkers. Permanently on watch, these programs check, inform and guide the layout process, allowing you to converge to a signoff-ready layout in the minimum possible time.

PRODUCT FINDER

ASIC and SOC Design:
Physical Analysis (Timing, Themal, Signal)
Verification

stand 15

MIDAS

Contact: Paul McCloskey
Enterprise Ireland, Industry House, Rossa Avenue, Bishopstown, Cork
Tel: +353 21 4800227
Fax: +353 21 4800271
E-Mail: paul.mcloskey@enterprise-ireland.com
Website: www.enterprise-ireland.com

MIDAS Ireland (Microelectronic Industry Design Association) is a national cluster consisting of microelectronics design companies and third level institutions in Ireland. The membership currently consists of 7 multinational companies, 18 indigenous companies and 17 academic members representing all the courses in Ireland that produce electronic engineering graduates. Its aim is to promote the growth of microelectronics in Ireland through collaboration in research, training and education. Enterprise Ireland is an associate member of MIDAS.

stand 9

MINALOGIC GRENOBLE ISERE

Contact: Véronique Pequignat
Grenoble Isere - AEPI, 1 Place Firmin Gautier 38027 Grenoble
Minalogic: Maison des Micro et Nanotechnologies,3 Parvis Louis Néel 38054 Grenoble
France
Tel: +33 04 76 70 97 04
Fax: +33 04 76 70 97 19
E-Mail: j.michel@grenoble-isere.com
Website: www.grenoble-isere.com/ www.minalogic.com

AEPI is the economic development agency for Grenoble-Isere/France, and provides complimentary information and services to companies exploring business opportunities. The Grenoble area, smart valley in southeastern France, is Europe's top center in micro-nanotechnologies and derived applications, with the whole food chain of the Industry being represented in the area, from EDA to design, component makers, equipment suppliers and end users. AEPI is also a member of the local board of the new Semi Europe Grenoble office, located on the Minatec Campus.
Global competitive cluster Minalogic fosters research-led innovation in intelligent miniaturized products and solutions for industry. Located in Grenoble, France, the cluster channels in a single physical location a range of highly-specialized skills and resources from knowledge creation to the development and production of intelligent

miniaturized services for industry. The technologies developed at the cluster are applicable to all business sectors : healthcare, energy efficiency, mobility, imagery, including more traditional industries. Minalogic brings together major corporations, small and mid-sized businesses, government agencies, and organizations from the public and private sectors.

stand 35

MOSIS

Contact: Lynne Wright
EDA Solutions Limited
Unit A5, Segengworth Business Centre
Segensworth Road
Fareham
Hants PO15 5RQ
United Kingdom
Tel: +44 1489 564 253
Fax: +44 01489 557 367
E-Mail: lynnewright@eda-solutions.com
Website: www.eda-solutions.com

MOSIS offer low cost and low volume access to a wide range of IC technologies from 1.5um down to the latest 65nm processes. Our services include wafer fabrication and plastic assembly services, via the foundires AMIS, austriamicrosystems, IBM and TSMC, and assembly house I2A.
You can chose between low cost shared access multi project wafer (MPW) runs, yielding up to hundreds of samples, or dedicated mask and wafer runs where higher volumes are required.
With MOSIS there are no die size constraints, so you receive exactly what you need.
MOSIS are represented in Europe by EDA Solutions, who will be happy to explain more to you about our services, and answer any questions you may have. Why not come to Stand 35 or visit the EDA Solutions website www.eda-solutions.com for more details.

PRODUCT FINDER

Services:
Prototyping
Foundry & Manufacturing
Semiconductor IP:
Physical Libraries

stand 31

MunEDA

Contact: Jin Qiu
Stefan-George-Ring 29
81929 Munich
Tel: +49 89 930 86 330
Fax: +49 89 930 86 407
E-Mail: jin.qiu@muneda.com
Website: www.muneda.com

MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA´s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA´s solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

stand 45

Nano-Tera.ch

Contact: Patrick Mayor
Nano-Tera.ch
EPFL / AA
INF 332 Station 14
CH-1015 Lausanne
Tel: +41 21 693 81 66
Fax: +41 21 693 81 60
E-Mail: patrick.mayor@nano-tera.ch
Website: www.nano-tera.ch

The Nano-Tera.ch program is a broad engineering program in Switzerland for health and security of humans and the environment, currently funded by the Swiss government. The program rationale is rooted in advances in engineering nano-scale materials and their exploitation in a variety of systems, requiring extreme integration and coordinated control of diverse micro/nano-scale components. Embodiments of such systems can be found in lightweight, mobile and personalized products embedded in the environment and on/in the body. These products will enable us, for example, to detect in real time different health risks and conditions through integrated bio probing, to reveal security risks through smart buildings and environments, to save energy through ambient sensing, and to detect and monitor environmental hazards such as floods and avalanches from space and/or inaccessible positions on earth. The outstanding novelty and power of these systems stem from their connectedness and the integration of heterogeneous components.

stand 36

nSilition

Contact: Thierry Delmot
Boulevard Dolez, 31
7000 Mons
Belgium
Tel: +32-65-37.42.40
Fax: +32-65-37.42.41
E-Mail: sales@nsilition.com
Website: www.nsilition.com

nSilition is a leader in the development and the qualification of industrial quality, very high performance, low power A/D and D/A converter IP cores with resolutions of up to 16 bits. These converters are available as ready-to-use semiconductor hard macros for most popular silicon processes.
Our design team has many years of hands-on industrial Analog and Mixed-Signal IC design experience. We will support you through the whole integration and product validation phase.
nSilition also provides all other required Analog and Mixed-Signal IP and IC design services: from financial and technical feasibility studies up to characterization tests, production validation and yield improvement.
nSilition services several main customers active in applications area like wireline communication, industrial, medical and aerospace.
We invite you to visit our booth for more details.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
System-Level Design:
Behavioural Modelling & Analysis
PCB & MCM Design
Test:
Design for Test
Design for Manufacture and Yield
Silicon Validation
Mixed-Signal Test
Services:
Design Consultancy
Prototyping
Hardware:
Development Boards
Semiconductor IP:
Analogue & Mixed Signal IP
Application-Specific IP:
Analogue & Mixed Signal IP
Telecommunication

stand 55

N S Mangat & Co

Contact: Mr. Ajit Singh
N.S. Mangat & Company
C 86 Hari Nagar
Clock Tower
New Delhi 110064
India
Tel: +91 11 65175357
Fax: +91 11 41694370
E-Mail: ns.mangat@mail.com
Website: www.nsmangat.com

N.S. Mangat & Company, is the leading technical conference and Exhibition of System design, modeling and design automation in worldwide. And N.S.M is institute of Tasting Quality & Maintenanace was founded in 1993 and is 100% privately owned. The company is managed by an

international team of highest skilled experts and is promoted by a group of qualified and experienced professional that has wide exposure to various traits.

The NSM company has built up a reputation providing prompt services and quality assurance and in the same connection the company is always on a look out for innovations in the domestic as well as international market.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
System-Level Design:
Package Design
Test:
Design for Manufacture and Yield

stand 5

Presto Engineering, Inc.

Contact: Richard Curtin
3907 North First Street
San Jose, CA 95134
Tel: - +1 408 434 1808
Fax: - +1 408 434 6842
E-Mail: richard.curtin@presto-eng.com
Website: www.presto-eng.com

Presto Engineering, an ISO 9001 company, delivers Design Success Analysis, integrated test and product engineering solutions to IDM and fabless companies, helping to improve the speed and predictability of new product releases. Presto combines unique technical expertise, extensive industry experience and state-of-the-art ATE for SoC and RF, reliability, failure analysis and fault isolation capabilities to offer a complete product engineering solution designed to complement the internal resources of its customers.
Presto now offers it's product engineering services from two sites -- the Silicon Valley hub in San Jose and the newly established lab in Normandy, France, after transfer from NXP to Presto in 2010.
Presto's product-engineering services from first silicon characterization to production release include:
- New product debug and failure analysis
- ATE for digital and RF designs
- e-Testing and characterization
- Sample preparation
- Reliability testing

Engineering staff at Presto have extensive industry experience with:
- In-silicon analysis docked with ATE
- Backside silicon FIB and electrical failure analysis for CSP and flip-chip packages
- Dynamic analysis of leakage. interconnect, and timing
- Scan-chain analysis and debug

PRODUCT FINDER

ASIC and SOC Design:
RF Design
System-Level Design:
Package Design
PCB & MCM Design
Test:
Design for Test
Design for Manufacture and Yield
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Services:
Design Consultancy
Prototyping
Foundry & Manufacturing

stand 49

ProximusDA

Contact: Philippe Metsu
ProximusDA GmbH Tuerkenstr. 71, Munich, 80799, Germany
Tel: +49 89 38157177-0
Fax: +49 89 38157177-3
E-Mail: philippe@proximusda.com
Website: www.proximusda.com

ProximusDA provides solutions for System Level Design using a new computing paradigm to enable efficient development and use of today's multi-processing compute capabilities. The company's "Proximus" development framework implements transaction level based methodology to specify, design, simulate and execute targeted parallel systems consisting of hardware and software. ProximusDA delivers products for system architects, system validation engineers and embedded software developers. By providing an alternative to traditional serial hardware and software design flows, Proximus shortens the embedded system development cycle and enables true system level optimization.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
System-Level Design:
Behavioural Modelling & Analysis
Acceleration & Emulation
Hardware/Software Co-Design
Test:
System Test
Services:
Design Consultancy
Embedded Software Development:
Real Time Operating Systems
Debuggers
Software/Modelling
Semiconductor IP:
Embedded Software IP

stand 52

R3LOGIC

Contact: Patrick BOTTI
R3Logic France
BHT-Minatec
7 Parvis Louis Néel
38000 Grenoble
France
R3Logic, Inc.
19A Crosby Drive
Suite 150
Bedford, MA 01730
USA
Tel: +33 (0)9 77 72 10 22
Fax: +1 781 276 7818
E-Mail: info@r3logic.com
Website: www.r3logic.com

R3Logic, Inc. is a privately-held company, founded in 2000, specializing in the design of 3D integrated circuits. Since 2001, working with DARPA-sponsored research programs, we have developed a unique set of EDA tools for 3D integrated circuit design and analysis, especially tools for true 3D integration and custom design.
R3Logic-France, sister-company to R3Logic Inc. and located in Grenoble, France, was established in 2008 following an invitation to join a European Consortium with STM and CEA-LETI. In the following year, R3Logic France created a common lab with CEA-LETI to research and develop new solutions for 3D Integration and participate as one of the main players in the Grenoble 3D EDA ecosystem.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
MEMS Design
RF Design

stand 18

SAME

Contact: Anne Claire DESNEULIN
C/o SKEMA
60 Rue Dostoïevski -BP 085
06902 Sophia Antipolis - France
Tel: +33 492 294 825
Fax: +33 492 294 321
E-Mail: anne-claire.desneulin @same-association.org
Website: www.same-conference.org

- SAME's Mission:

Valorize, promote and develop excellence in the microelectronics sector covering the design technology for advanced electronic circuits in the South of France.
- SAME Objective:

- To organize the SAME Forum to promote the microelectronic industry within the region.

• SAME in Action:
- SAME 2011 Forum: October 12 & 13, 2011 and SAFA Workshops - Sophia Antipolis, France.
Main Topic: Digital Mobility
More information on
www.same-conference.org
- "SAME goes back to School": Presents information on careers in microelectronics engineering to regional high school students with the aim of encouraging them to take engineering degrees.
- Promoting microelectronic start-ups: individualised analysis and assistance on everything from defining market strategy to client/partner prospecting.
- CIM PACA provides academic and industrial entities with leading-edge tools to design ICs for the next generation of secure mobile communication devices.
- Sophia Academy: is an initiative of leaders' company. They want to propose to their employees a local access to high level trainings. They want to share their experiences and mutualize their needs.

stand 41

Satin Technologies

Contact: Michel Tabusse
Cap Omega, Rond-Point Benjamin Franklin
CS 39521
34960 Montpellier Cedex 2, France
Tel: +33 467 13 00 86
Fax: +33 467 13 00 10
E-Mail: date2011@satin-tech.com
Website: www.satin-tech.com

Satin Technologies delivers software solutions for fact-based design quality monitoring and closure.
Working within customers' design flows, the company's VIP Lane® turns customers' design practices (for IP blocks, SoCs, embedded systems) into a robust and reliable set of quality criteria and metrics. These customer-based parameters are used to create automated, sharable dashboards and quality compliance reports.
By providing an alternative to manually filled, time-consuming checklists and documents, VIP Lane® delivers effective flow integration and on-the-fly quality monitoring at zero overhead to design teams.

PRODUCT FINDER

Services:
Data Management and Collaboration

stand 58

SELEX Galileo

Contact: Sergio Pellegrini
Via A. Einstein 35,
50013 Campi Bisenzio (FI)
ITALY
Tel: +39 055 89501
Fax: +39 055 8950600
E-Mail: sales.marketing@selexgalileo.com
Website: www.selexgalileo.com

SELEX Galileo, a Finmeccanica Company, develops integrated capability solutions which deliver enhanced situation awareness, security, and safety across land, sea and air. Solutions from surveillance, imaging, tracking, targeting to protection and navigation control systems for military and government missions. Customers across 5 continents have already selected SELEX Galileo as their partner of choice to provide total awareness, total protection solutions for their present and future needs.

stand 15

Silansys Semi

Contact: Niall O'Hearcain
Adelaide Chambers
Peter Street
Dublin 8
Ireland
Tel: +353 1 4830840
E-Mail: niall@silansys.com
Website: www.silansys.com

Silansys develops and supplies innovative turnkey ASIC products and provides a full range of Design Services to industry-leading companies worldwide. Silansys is a qualified product and services supplier to a wide range of blue-chip OEM and top-5 semiconductor companies worldwide in markets ranging from consumer communications to hi-rel industrial sensors. Silansys has a world-class track-record in architecting and delivering successful commercial products that integrate innovative RF, Mixed-Signal and Digital technology into single-chip SoC products.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
RF Design
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Hardware/Software Co-Design
Package Design
PCB & MCM Design
Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Services:
Design Consultancy
Prototyping
Data Management and Collaboration
IP e-commerce & Exchange
Foundry & Manufacturing
Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Workstations & IT Infrastructure
Semiconductor IP:
Analogue & Mixed Signal IP
Application-Specific IP:
Analogue & Mixed Signal IP
Data Communication
Digital Signal Processing
Networking
Wireless Communication

stand 3

SPRINGER

Contact: Lothar Minicka
Tiergartenstr. 17
69121 Heidelberg
Germany
Tel: +49 6221 4870
Fax: +49 6221 4878366
E-Mail: lothar.minicka@springer.com
Website: www.springer.com

Springer is one of the world-leaders in book publishing, boasting a broad range of subject matter, and a history of working with the most prestigious scholars in the field. Additionally, Springer publishes an astute collection of Journals, with a track record of generating the latest sought after content. For additional information about all our engineering publications, please stop by our booth, or visit us at springer.com

SPECIAL FOCUS DAY

WIRELESS INNOVATIONS FOR SMARTPHONES

KEYNOTE –
Wednesday, March 16th, 1400
Hannu Kauppinen,
Director, Head of Radio Systems Laboratory,
Nokia Research Center, Finland

stand 35

Tanner EDA

Contact: Lynne Wright
EDA Solutions Liimited
Unit A5, Segensworth Business Centre,
Segenswoth Road,
Fareham
Hants PO15 5RQ
United Kingdom
Tel: +44 1489 564 253
Fax: +44 1489 557 367
E-Mail: lynnewright@eda-solutions.com
Website: www.eda-solutions.com

Tanner EDA develops and markets electronic design automation software for designers of mixed-signal and analog ICs, and MEMS circuits. Our L-Edit Pro layout and verification software and T-Spice Pro design entry and simulation software provide a complete, productive and cost-effective design solution. Tanner Tools are easy-to-use and truly affordable, with a powerful range of features and industry-standard file formats. With over 25,000 licenses sold worldwide these are the best and most reliable products for IC Design for Windows PC.
We are represented in Europe by EDA Solutions (www.eda-solutions.com). Come and meet us and see for yourself the Power Behind the Tool!

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design
Services:
Design Consultancy
Semiconductor IP:
Analogue & Mixed Signal IP
Physical Libraries
Application-Specific IP:
Analogue & Mixed Signal IP

stand 4

Target Compiler Technologies

Contact: Jeroen De Lille
Technologielaan 11-0002,
3001 Leuven,
Belgium
Tel: +32 16 38 1030
Fax: +32 16 38 1049
E-Mail: info@retarget.com
Website: www.retarget.com

Target Compiler Technologies is the leading provider of software tools to automate and optimize the design and programming of application-specific processor cores (ASIPs).

The "IP Designer" tool suite has been applied by customers worldwide for diverse application domains, including GSM/WCDMA/HSDPA handsets, VoIP, audio/video/image codec/processing, automotive, ADSL/VDSL modems, wireless LAN, hearing instruments, and mobile/low-power applications.
URL: www.retarget.com

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
System-Level Design:
Acceleration & Emulation
Hardware/Software Co-Design
Services:
Design Consultancy
Embedded Software Development:
Compilers
Debuggers
Software/Modelling

stand 19

Tech Design Forum

Contact: Sandra Sillion
Tel: +1 949 226 2011
E-Mail: Sandras@rtcgroup.com
Website: www.edatechforum.com

Today's electronic design engineers face broader challenges than ever before. Software is becoming as important as hardware. And in the IC supply chain, former competitors are now collaborating to achieve success.
Tech Design Forum publication (formerly called the EDA Tech Forum) is the premier guide for success in this complex environment. Focused on the design automation market, this publication and its rich website offer a wealth of practical advice on how to successfully negotiate the day-to-day problems designers face.

stand 17

The Next Silicon Valley

Contact: Richard Wallace
Tel: +1 631 907-2559
E-Mail: rwallace@thenextsiliconvalley.com
Website: www.thenextsiliconvalley.com

The Next Silicon Valley is an independent media website that publishes global news and information about the world of innovation, entrepreneurship, technology development, regional economic development, venture capital, and investment promotion across global markets. The Next Silicon Valley reaches readers in more than 90 countries and 400 cities worldwide.

stand 50

TinnoTek Inc.

Contact: Shan-Chien Fang
121R, Innovation Incubator, National Tsing Hua University, 101, Sec. 2, Kuang-Fu Rd.,Hsinchu 300, Taiwan, R.O.C.
Tel: +886 3 5741082
Fax: +886 3 5741084
E-Mail: service@tinnotek.com.tw
Website: www.tinnotek.com.tw

PRODUCT FINDER

ASIC and SOC Design:
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Services:
IP e-commerce & Exchange
Semiconductor IP:
Configurable Logic IP

stand 13

TowerJazz

Contact: Melinda Jarrell
4321 Jamboree Road
Newport Beach, CA 92660
USA
Tel: 001 9494358181
Fax: 001 949-435-8757
E-Mail: melinda.jarrell@towerjazz.com
Website: www.towerjazz.com

TowerJazz is recognized for our industry leading models and tools which give our customers a significant competitive market advantage with first time design success, optimal performance, and the shortest time-to-market at reduced cost. Our extensive design enablement infrastructure provides an environment optimized for analog and RF designs. This includes silicon verified and highly scalable device models and robust physical design tools for up front design optimization. Unique tools such as Monte Carlo statistical and PCM based models allow the user to maximize the performance-yield tradeoff. In addition, MOSVAR model libraries improve simulation accuracy reducing product development time. The Jazz Inductor Toolbox (JIT) provides advanced modeling capability for octagonal and square inductors to provide designers flexibility in choosing the right inductors when designing their products. Our powerful and efficient tools enable unprecedented accuracy in device models and our unparalleled customer support at every stage of the design flow ensures confidence in designs at near zero risk.

PRODUCT FINDER

ASIC and SOC Design:
Verification
MEMS Design
RF Design
Services:
Foundry & Manufacturing
Semiconductor IP:
Analogue & Mixed Signal IP
Application-Specific IP:
Analogue & Mixed Signal IP
Wireless Communication

stand EP9

TRAMS

Contact: Antonio Rubio
c/ Jordi Girona 31, 08034 Barcelona, Spain
Tel: +34934017485
Fax: +34934016756
E-Mail: antonio.rubio@upc.edu
Website: www.trams-project.eu

Technology projections indicate that future electronic devices will keep shrinking, being faster and consuming less energy per operation. In the next decade, a single chip will be able to perform trillions of operations per second and provide trillions of bytes per second in off-chip bandwidth. This is the so called Terascale Computing era, where terascale performance will be mainstream, available in personal computer, and being the building block of large data centers with petascale computing capabilities. However, these smaller devices will be much more susceptible to faults and its performance will exhibit a significant degree of variability. As a consequence, to unleash these impressive computing capabilities, a major hurdle in terms of reliability has to be overcome. The TRAMS project is the bridge for reliable, energy efficient and cost effective computing in the era of nanoscale challenges and teraflop opportunities.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Physical Analysis (Timing, Themal, Signal)
Verification
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Semiconductor IP:
CPUs & Controllers
Memory IP
On-Chip Bus Interconnect
Physical Libraries

stand 15

Tyndall's Design Technology Evaluation Group

Contact: Ted O'Shea
University College Cork
Dyke Parade
Cork
Ireland
Tel: +353 21 4904159
E-Mail: ted.OShea@Tyndall.ie
Website: www.tyndall.ie/DTE

Tyndall's Design Technology Evaluation (DTE) group performs Intellectual Property patent infringement investigation for key European and US companies. This group implements a complete 'tear down' of an IC's design, its technology, its assembly and system; then compare with a portfolio of patents in order to ascertain if infringement has occurred. A report is then generated providing clear evidence in relation to specific patents. Where necessary, staff will also support its findings as a 'facts expert witness' in a court of law. In support of our IP investigation work is an extensive infrastructure of analysis equipment in excess of €35 Million. This group also performs extensive electrical characterisation of 'mixed signal' designs.

PRODUCT FINDER

ASIC and SOC Design:
Physical Analysis (Timing, Themal, Signal)
System-Level Design:
Acceleration & Emulation
Hardware/Software Co-Design
Test:
Design for Test
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
System Test
Services:
Design Consultancy
IP e-commerce & Exchange
Foundry & Manufacturing
Training
Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Semiconductor IP:
Analogue & Mixed Signal IP
Memory IP
On-Chip Debug
Test IP
Verification IO
Application-Specific IP:
Analogue & Mixed Signal IP
Security

stand 46

University Booth

Contacts: Volker Schöber (Germany), Lorena Anghel (France)
edacentrum GmbH, Schneiderberg 32, 30167 Hannover, Germany
TIMA Laboratory, 46 avenue Felix Viallet, 38031 Grenoble, France
Tel: +49 (511) 762 19688 (Germany), +33 (4) 7657 4696 (France)
Fax: +49 (511) 762 19695 (Germany), +33 (4) 7657 4981 (France)
E-Mail: university-booth@date-conference.com
Website: date-conference.com/group/exhibition/u-booth

The University Booth is part of the DATE program and is sponsored by the DATE Sponsor Society. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are presenting innovative hardware and software demonstrations. All demonstrations will take place during the exhibition within a dedicated time slot. The University Booth is organized by Lorena Anghel (TIMA Laboratory) and Volker Schöber (edacentrum).

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Physical Analysis (Timing, Themal, Signal)
Verification
Analogue and Mixed-Signal Design
MEMS Design
RF Design
System-Level Design:
Behavioural Modelling & Analysis
Physical Analysis
Acceleration & Emulation
Hardware/Software Co-Design
Package Design
Test:
Design for Manufacture and Yield
Logic Analysis
Test Automation (ATPG, BIST)
Boundary Scan
Silicon Validation
Mixed-Signal Test
System Test
Services:
Design Consultancy
Prototyping
Data Management and Collaboration
IP e-commerce & Exchange
Training
Embedded Software Development:
Compilers
Software/Modelling
Hardware:
FPGA & Reconfigurable Platforms
Development Boards

stand 22

University of Southampton

Contact: Dr Steve Beey
University of Southampton
School of Electronics and Computer Science
Highfield, Southampton, SO17 1BJ
UK
Tel: +44 2380 596663
Fax: +44 2380 592901
E-Mail: spb@ecs.soton.ac.uk
Website: www.ecs.soton.ac.uk

The School of Electronics and Computer Science (ECS) is at the forefront of electronics systems design for energy harvesting applications. ECS has a strong international reputation in the field of energy harvesting and is at the forefront of research activities in this area. ECS is leading the EPSRC funded project 'Next Generation Energy Harvesting Electronics: Holistic Approach' and is also managing on behalf of the community the EPSRC funded Network on Energy Harvesting. ECS also a partner on two ongoing EU Framework 7 projects on energy harvesting, TRIADE and TIBUCON, and togther these research activities combine state of the art development of flexible energy harvesting systems with practical applications in aeronautics and building management. The energy harvesting network provides an important focus for the community with the objective of raising the profile of research in this area and identifying future opportunities. In 2004, ECS formed Perpetuum Ltd, a University spin-out based upon vibration energy harvesting research.

PRODUCT FINDER

ASIC and SOC Design:
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Analogue and Mixed-Signal Design
MEMS Design
System-Level Design:
Behavioural Modelling & Analysis
Acceleration & Emulation
Hardware/Software Co-Design
PCB & MCM Design
Test:
Design for Test
Design for Manufacture and Yield
Mixed-Signal Test
System Test
Services:
Design Consultancy
Prototyping
Data Management and Collaboration
IP e-commerce & Exchange
Embedded Software Development:
Software/Modelling
Semiconductor IP:
Analogue & Mixed Signal IP
Embedded FPGA
Embedded Software IP
Application-Specific IP:
Analogue & Mixed Signal IP
Digital Signal Processing

stand 24

Veriest Venture

Contact: Berg Tara
22A Raul Walenberg St. Beit Zamir, Ramat Hachayal, Tel Aviv, Israel
Tel: +972.73.705.2530
Fax: +972.3.644.0737
E-Mail: info@veriest-v.com
Website: www.veriest-v.com

Veriest Venture is a novel IC and EDS design house providing forefront ASIC and FPGA design services and Electronic Design complex System engineering services. Our family of customers includes leading companies across the networking, data, communication, consumer electronics and wireless industries. Our skilled and creative team can effectively promote architecture design, implementation, system integration and advanced verification. Veriest's scope of expertise extends form silicon to system specification, and is a design leader in system and micro architecture, frontend VSLI, functional and formal verification and FPGA emulation. Owing to our productive partnerships with major EDA companies, such as Cadence, Synopsys and Mentor Graphics, Veriest has become one of the early adopters of the latest in chip design and EDA technologies. Our highly trained design quality engineers and process analysts ensure we continue to provide leading applications and ASIC, SoC, FPGA design and verification services. From specification to first-time-right silicon, our expertise in architecture, high speed and low power design and methodology enables our customers to achieve enhanced performance and faster time-to-market.

PRODUCT FINDER

ASIC and SOC Design:
Design Entry
Behavioural Modelling & Simulation
Synthesis
Power & Optimisation
Verification
System-Level Design:
Behavioural Modelling & Analysis
Acceleration & Emulation
Hardware/Software Co-Design
PCB & MCM Design
Services:
Design Consultancy
Prototyping
Data Management and Collaboration
IP e-commerce & Exchange
Training
Embedded Software Development:
Software/Modelling
Hardware:
FPGA & Reconfigurable Platforms
Development Boards
Semiconductor IP:
Configurable Logic IP
CPUs & Controllers
Embedded FPGA
Memory IP
On-Chip Bus Interconnect
Processor Platforms
Verification IO
Application-Specific IP:
Data Communication
Digital Signal Processing
Multimedia Graphics
Networking
Telecommunication
Wireless Communication

stand 34

XYALIS

Contact: Rene Donkers
US office, San Carlos, California, USA
Europe Office, Eindhoven, the Netherlands
Tel: +31 641539004
Fax: +31 847503816
E-Mail: info@fract-tech.com
Website: www.fract-tech.com

XYALIS is an EDA company offering a fully integrated Mask Data Preparation solution to eliminate the risk of error, reduce time to manufacturing, and increase manufacturing yield by automating frame generation, Multi-Project Wafers assembly, intuitive mask set creation, and wafer map optimization, and by streamlining the mask order process. XYALIS' solutions have been developed in cooperation with major semiconductor industry leaders and have been used in production for years.

PRODUCT FINDER

Test:
Design for Manufacture and Yield
Services:
Data Management and Collaboration
Embedded Software Development:
Software/Modelling

DATE 12

Conference and Exhibition
March 12-16, 2012, ICC, Dresden, Germany

Preliminary Call for Participation

Scope of the Event

The 15th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organisation of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. **More details are given on the DATE website (www.date-conference.com).**

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Power Estimation and Optimization
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical and Healthcare Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles; Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by **September 11th, 2011** via: http://www.date-conference.com/submit.html
Papers can be submitted either for standard oral presentation or for interactive presentation

DATE Secretariat

European Conferences
3 Coates Place,
Edinburgh, EH3 7AA, UK

Tel: +44-131-225-2892
Fax: +44-131-225-2925
Email: sue.menzies@ec.u-net.com

Chairs

General Chair: Wolfgang Rosenstiel, University of Tuebingen, Germany, rosenstiel@informatik.uni-tuebingen.de

Program Chair: Lothar Thiele, ETH Zurich, Switzerland, thiele@tik.ee.ethz.ch