advance programme

DATE 11

Design, Automation & Test in Europe

Grenoble, France
March 14 - 18, 2011

www.date-conference.com

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welcome to DATE 11

Dear Colleague,

We proudly present to you the Advance Programme of **DATE 11.** DATE combines the world's favourite electronic systems design conference with an international exhibition for electronic design, automation and test, from system level hardware and software implementation right down to integrated circuit design. While many conferences currently suffer from travel restrictions in many companies and face severe problems in attracting attendees, DATE 2011 received some 950 submissions. The importance of DATE as a worldwide indispensable meeting point is demonstrated by the fact that more than 50% of the submissions came from outside Europe. The most popular topics this year were Simulation/Emulation and Low Power Systems Design, Estimation and Optimisation.

For the 14th successive year DATE has prepared an exciting technical programme, with the help of more than 300 members of the Technical Programme Committee, who dedicated their time to thoroughly review the submissions, ranging from system level down to circuit design and covering all the most relevant application domains.

This year the conference will be held in France, at Alpexpo in Grenoble and will span an entire working week starting on Monday March 14 with tutorials, and ending on Friday March 18 with workshops.

The **plenary keynote speakers** on Tuesday are Steve Furber of Manchester University, UK, to talk about 'Biologically-inspired massively-parallel architectures – computing beyond a million processors', and Philippe Magarshack, STMicroelectronics, France to talk about 'How Technology R&D Leadership brings a competitive advantage in the fields of multimedia convergence and power applications'. On the same day, the **Executive Track** offers a series of business panels discussing hot topics in design: 'Ideas on Future of EDA and IP Industry', '22nm Challenges and Wealth/Knowledge Creation Opportunities' and 'System Level Complexity and Innovation'. To emphasise that DATE is the major event for the designers, DATE 11 features invited sessions where **Europe's famous consumer industry presents its best designs and design practices.**

The main conference programme from Tuesday to Thursday includes 77 technical sessions organised in parallel tracks from four areas:

D – Design Methods, Tools, Algorithms and Languages
A – Application Design
T – Test Methods, Tools and Innovative Experiences
E – Embedded Software

Extra tracks are dedicated to the Executive Day on Tuesday and the two special days: **Smart Devices of the Future Day** on Wednesday and **Intelligent Energy Management – Supply and Utilisation Day** on Thursday with Hannu Kauppinen, Nokia Research Center, FI and Carmelo Papa, STMicroelectronics, IT as keynote speakers. Additionally, there are 62 Interactive Presentations which are organised into five IP sessions.

Finally, DATE offers a comprehensive overview of commercial design and verification tools in its exhibition including vendor seminars and abundant networking possibilities with fringe meetings.

We wish you a productive and exciting DATE 11 and a memorable social party on Wednesday evening.

DATE 11 General Chair
Bashir Al-Hashimi
University of Southampton, UK
bmah@ecs.soton.ac.uk

DATE 11 Programme Chair
Enrico Macii
Politecnico di Torino
enrico.macii@polito.it

plenary session

Tuesday, March 15, 2011, 0830 – 1030

Opening Address – Awards – Keynote Speakers

first keynote address

Biologically-inspired massively-parallel architectures – computing beyond a million processors

S Furber, ICL Professor of Computer Engineering, School of Computer Science, Manchester U, UK

Moore's Law continues to deliver ever-more transistors on an integrated circuit, but discontinuities in the progress of technology mean that the future isn't simply an extrapolation of the past. For example, design cost and complexity constraints have recently caused the microprocessor industry to switch to multi-core architectures, even though these parallel machines present programming challenges that are far from solved. Moore's Law now translates into ever-more processors on a multi-, and soon many-core chip. The software challenge is compounded by the need for increasing fault-tolerance as near-atomic-scale variability and robustness problems bite harder.

We look beyond this transitional phase to a future where the availability of processor resource is effectively unlimited and computations must be optimised for energy usage rather than load balancing, and we look to biology for examples of how such systems might work. Conventional concerns such as synchronisation and determinism are abandoned in favour of real-time operation and adapting around component failure with minimal loss of system efficacy.

plenary session

Tuesday, March 15, 2011, 0830 – 1030

Opening Address – Awards – Keynote Speakers

second keynote address

How technology R&D leadership brings a competitive advantage in the fields of multimedia convergence and power applications

Philippe Magarshack, Group Vice-President, Technology R&D - General Manager, Central CAD and Design Solutions, STMicroelectronics, France

From 1985 to 1989, Magarshack designed microprocessors arithmetic blocks at AT&T Bell Labs in New Jersey, Pennsylvania and California. In 1989, he joined Thomson-CSF in Grenoble, France, as libraries and ASIC Manager. In 1994, Magarshack joined the Central R&D of SGS-THOMSON Microelectronics (now STMicroelectronics), where he held several Program Management roles in advanced CMOS Design Platforms. Since 2005, Magarshack heads ST's Central Library, IP and CAD organisation, which defines and provides design solutions to all ST Product Groups in CMOS, embedded NVM and BCD processes, ranging from 0.35um to 20nm technologies.

In his current role, Magarshack oversees ST's EDA vendor strategy, setting up and managing joint R&D programs to address ST's future design needs. Magarshack is ST's Enablement Executive at the IBM ISDA CMOS Bulk Alliance in 32/28nm and 22/20nm.

Philippe Magarshack was born in London, UK, and graduated with an engineering degree in Physics from Ecole Polytechnique in Palaiseau, France in 1983 and with an Electronics Engineering degree from Ecole Nationale Supérieure des Télécommunications in Paris, France in 1985.

general information

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 11. Full General Information covering full technical programme details, conference registration costs and booking forms, hotel reservations and booking forms, travel to and in Grenoble, and social event details is available on the conference website - **www.date-conference.com**

interactive programme on web

A fully interactive DATE 11 programme is available on the web – **www.date-conference.com** - where you will be able to view the entire detail of the programme and plan your attendance in advance.

venue

The Conference will take place from 14-18 March 2011 and the Exhibition from 15-17 March 2011 in Alpexpo, Avenue d'Innsbruck, Grenoble, France - **www.alpexpo.com**

date party – wednesday

This year the DATE party will take place in the World Trade Center, Grenoble. The evening will feature a buffet style dinner with plenty of buffet points and drinks to accompany dinner. Musical entertainment with the opportunity to dance will be provided by the popular neo-folk band DJAL. In an enjoyable atmosphere participants will have the opportunity to meet and mingle with their friends and colleagues. All conference attendees, users, vendors and their guests are encouraged to come to the party. Additional tickets for the full Evening Social Programme may be obtained for 70 Euros each (see website for booking forms). Entrance will be by ticket only, so please check that you receive the party ticket when you register.

cancellation policy

Registered delegates should note that no refunds will be made unless a written request for cancellation is received prior to **18 February 2011.** All refunds are subject to a 10% processing fee. Substitutions will be accepted at any stage.

interactive presentations

Chair: Andrea Acquaviva, Politecnico di Torino, IT

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute, one-slide presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area.

Interactive Sessions will be held in the Salle de Reception area in 30-minute time slots during coffee and exhibition breaks. Coffee and water will be available during the session.

executive sessions – tuesday

Organiser:
Yervant Zorian, Synopsys, US

DATE 11 will again feature an Executive Track of presentations by leading company executives (CEOs, Presidents and VPs) representing a range of semiconductor manufacturers, EDA vendors, fabless houses, IP providers and equipments suppliers. This one-day program will be held on Tuesday 15 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 5-6 executives and run in parallel to the technical conference tracks. All three executive sessions will first provide each executive with a time-slot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view.

2.1 EXECUTIVE SESSION - Ideas on Future of EDA and IP Industry

– see page 27

3.1 EXECUTIVE SESSION – 22nm Challenges and Wealth/Knowledge Creation Opportunities

– see page 34

4.1 EXECUTIVE SESSION - System Level Complexity and Innovation

– see page 39

Organisers:
Ahmed Jerraya, CEA LETI, FR
John Goodacre, ARM, US

Smart Devices of the Future Special Day

Future electronic systems will be dominated by the convergence between design (hardware and software) and fabrication to master next generation smart devices. The design of highly integrated and autonomous intelligent devices for healthcare, mobile and consumer applications require deep knowledge of technology characteristics to reach the required performance. Furthermore, hardware and software are being employed increasingly to overcome fabrication imperfection and to improve yield. This special day will focus on applications, key enabling technologies and future trends driving smart devices of the future.

The **Keynote Presentation** entitled 'Wireless Innovations for Smartphones' will be given by Hannu Kauppinen, Director, Head of Radio Systems Laboratory, Nokia Research Center, Finland.

5.1 **EMBEDDED TUTORIAL –Smart Devices for the Cloud Era**
– see page 44

6.1.1 **HOT TOPIC/EMBEDDED TUTORIAL – Ultra Low Power Smart Devices**
– see page 50

6.1.2 **SPECIAL DAY KEYNOTE AND AWARDS**
– see page 55

7.1 **HOT TOPIC – Smart Medical Implants**
– see page 56

8.1 **PANEL SESSION – Integrating the Real World Interfaces**
– see page 62

Organisers:
Paul Mitcheson, Imperial College, UK
Paul K Wright, UC Berkeley, US

Intelligent Energy Management – Supply and Utilisation Special Day

The links between the disciplines of computation, power electronics, and power systems must become stronger as we move into a world of increasing energy utilisation and efficiency. This special day will foster the necessary links between these separate disciplines through invited presentations from experts in the areas of energy generation, storage and utilisation. The day will also cover recent innovations in enabling technologies for portable devices (energy-harvesting and wireless powering) and applications of intelligent systems to improve the utilisation of electricity supply through smart metering and infrastructure.

The **Keynote Presentation** entitled 'Smart Energy at ST' will be given by Carmelo Papa, Executive VP Industrial and Multisegment, STMicroelectronics, Italy.

9.1 **TUTORIAL – Energy Transfer, Generation and Power Electronics** – see page 68

10.1.1 **Smart Energy Generation: Design Automation and the Smart-Grid** – see page 75

10.1.2 **SPECIAL DAY KEYNOTE** – see page 80

11.1 **Smart Energy Utilisation: From Circuits to Consumer Products** – see page 81

12.1 **PANEL SESSION – What does the power industry need from the EDA industry and what is the EDA industry doing about it?** – see page 88

special sessions

Special Sessions Chairs:
Wolfgang Mueller, University of Paderborn, DE
Tom Fitzpatrick, Mentor Graphics, US

The following 17 Special Sessions have been organised, which should prove to be of great general interest.

Panel Sessions provide a forum in which motivated opinions on a controversial issue are discussed. The 'trend setters' are given a time-slot to present their views, which are then subjected to critical appraisal from the audience. **Hot Topic** sessions give technical information about emerging new topics and provide a good overview and technical insight. Presenters are leading experts in the field. They present their view on the relevant issues and their importance for research and development. **Embedded Tutorials** give an insight of relevant topics usually starting from an introductory base.

2.4 **Panel and Embedded Tutorial – Logic Synthesis and Place and Route: After 20 Years of Engagement, Wedding in View?**
Organiser: M Casale-Rossi, Synopsys, US

2.8 **Embedded Tutorial – Addressing Critical Power Management Verification Issues in Low Power Designs**
Organiser: B Kapoor, Mimasic, US

3.8 **Panel Session – Power Formats: Beyond UPF and CPF**
Organiser: B Pangrle, Mentor Graphics, US

5.7 **Embedded Tutorial – Architectures for Online Error Detection and Recovery in Multicore Processors**
Organiser: D Gizopoulos, Piraeus U, GR

6.7 **Hot Topic – Virtual Manycore Platforms: Moving Towards 100+ Processor Cores**
Organisers: R Leupers, RWTH Aachen U, DE and **G Martin,** Tensilica, US

6.8 **Panel Session – Embedded Software Debug and Test**
Organiser: M Winterholer, Cadence, DE

7.7 **Hot Topic – Foundations of Component-Based Design for Embedded Systems**
Organisers: A Sangiovanni-Vincentelli, UC Berkeley, US and Trento U, IT and **J Sifakis,** VERIMAG, FR

7.8 **Embedded Tutorial – Predictable System Integration**
Organiser: W Kruijtzer, Synopsys, NL

8.7 **Hot Topic – Flows, Application and Future of Component-based Design for Embedded Systems**
Organisers: A Sangiovanni-Vincentelli, UC Berkeley, US and Trento U, IT and **J Sifakis,** VERIMAG, FR

8.8 **Embedded Tutorial – Communication Networks in Next Generation Automobiles**
Organisers: T Kazmierski, Southampton U, UK and **C Grimm,** TU Vienna, AT

9.7 **Embedded Tutorial – Sub-Wave Length Lithography and Variability Aware Test and Characterisation Methods**
Organiser: S Kundu, U of Massachusetts Amherst, US

10.7 **Embedded Tutorial – Die Stacking Goes Mobile and Embedded**
Organiser: A Jerraya, CEA-LETI MINATEC, FR

10.8 **Panel Session –State of the Art Verification Methodologies in 2015**
Organiser: T Fitzpatrick, Mentor Graphics, US

11.7 **Hot Topic – New Frontiers in Embedded Systems Design: Technology and Applications**
Organiser: G De Micheli, EPF Lausanne, CH

11.8 **Hot Topic – Stochastic Circuit Reliability Analysis in Nanometer CMOS**
Organiser: G Gielen, KU Leuven, BE

12.7 **Hot Topic – Sustainability through Massively Integrated Computing: Are We Ready to Break the Energy Efficiency Wall for Single-Chip Platforms?**
Organiser: R Marculescu, Carnegie Mellon U, US

12.8 **Hot Topic – Synthesis Supported Increase of Efficiency in Analogue Design**
Organiser: J Nowak, IMMS GmbH, DE

MONDAY

Educational Tutorials
Welcome Reception

TUESDAY

Technical Conference and Exhibition Day 1
Vendor Exhibition
Tool Seminars
Exhibition Theatre (also featuring Track 8 special conference sessions)
Opening Plenary, Keynote Addresses and Distinguished Awards
Executive Sessions
Lunch and Learn Session sponsored by Mentor Graphics
Evening Reception offered by the City of Grenoble

WEDNESDAY

Technical Conference and Exhibition Day 2
Vendor Exhibition
Tool Seminars
Exhibition Theatre (also featuring Track 8 special conference sessions)
Smart Devices of the Future Special Day and Keynote
DATE Awards Ceremony
DATE Party

THURSDAY

Technical Conference and Exhibition Day 3
Vendor Exhibition
Tool Seminars
Exhibition Theatre (also featuring Track 8 special conference sessions)
Intelligent Energy Management –
Supply and Utilisation Special Day and Keynote

FRIDAY

Special Interest Workshops

CONTACTS

DATE Event Secretariat
European Conferences
3 Coates Place
EDINBURGH EH3 7AA
United Kingdom
Tel: +44 131 225 2892
Fax: +44 131 225 2925

Conference and Speaker Enquiries
Email: sue.menzies@ec.u-net.com

Exhibitor and Exhibition Enquiries
Email: claire.cartwright@ec.u-net.com

0730	TUTORIAL REGISTRATION AND WELCOME REFRESHMENTS			
BREAKS	1100-1130 Morning, 1300-1430 Lunch, 1600-1630 Afternoon.			
0930 to 1800	A (Room - Belle-Etoile)	B (Room – Chartreuse)	C (Room – Les Bans)	
	Low Power SOC Design: Best Practice – and what's next?	Electronic System Level Design and Verification	Manufacturing, CAD and Thermal-Aware Design for 3D System-on-Chip Design	
0930 to 1300	D1 (Room – Meije 3)	E1 (Room – 7 Laux 4)	F1 (Room – 7 Laux 5)	G1 (Room – Room Meije 2)
	MPSoC Hardware/Software Architectural and Design Challenges/Solutions	On-chip interconnect for new generation of SoC	Renewable energy: solar power generation, conversion and delivery	Power-Aware Testing and Test Strategies for Low Power Devices
1430 to 1800	D2 (Room – Meije 3)	E2 (Room – 7 Laux 4)	F2 (Room – 7 Laux 5)	G2 (Room – Meije 2)
	Model-based MPSoC Architecture Synthesis for Highly-demanding Embedded Applications	Design and Verification Challenges for Automotive Electronics	Overcoming CMOS Reliability Challenges: From Devices to Circuits and Systems	Testing TSV-Based 3D Stacked Ics
1800	Welcome Reception			

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1030-1130 Exhibition Break, 1300-1430 Lunch, 1600-1700 Exhibition Break (1600-1630 IP1)					
0830	1.1 PLENARY: OPENING, KEYNOTE ADDRESSES AND AWARDS PRESENTATION, Auditorium Dauphine							

	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
1130 to 1300	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	2.1 EXECUTIVE SESSION – Ideas on Future of EDA and IP Industry	2.2 System-Level Techniques to Handle Performance, Reliability and Thermal Issues	2.3 Modelling and Simulation of Interconnects	2.4 PANEL AND EMBEDDED TUTORIAL SESSION – Logic Synthesis and Place and Route: After 20 Years of Engagement, Wedding in View	2.5 Transient Faults and Soft Errors	2.6 Networked Embedded Systems	2.7 Design of Energy-Efficient and Automotive Systems	2.8 EMBEDDED TUTORIAL – Addressing Critical Power Management Verification Issues in Low Power Designs
1400	3.0 SPECIAL LUNCH-TIME SESSION 1300-1400 Grenoble EDA Ecosystem Session - From Research to Market sponsored by Mentor Graphics, Auditorium Dauphine							
1430 to 1600	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	3.1 EXECUTIVE SESSION – 22nm Challenges and Wealth/Knowledge Creation Opportunities	3.2 Power Optimisation of Multi-Core Architectures	3.3 Core Algorithms for Formal Verification Engines	3.4 Predicting Bugs and Generating Tests for Validation	3.5 Timing Related Issues in Test	3.6 Performance and Timing Analysis	3.7 Implementations for Digital Baseband Processing	3.8 PANEL SESSION – Power Formats: Beyond UPF and CPF
1700 to 1830	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	4.1 EXECUTIVE SESSION – System Level Complexity and Innovation	4.2 Robust and Low Power Systems	4.3 Formal Verification Techniques and Applications	4.4 System Level Simulation and Validation	4.5 Advances in Analogue, Mixed Signal and RF Testing	4.6 Design Automation Methodologies and Architectures for Three-Dimensional ICs	4.7 Resource Management for QoS Guaranteed NoCs	SEE WEB OR EVENT GUIDE FOR LATEST EXHIBITION PROGRAMME
1830	Evening Reception Offered by the City of Grenoble							

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP2), 1230-1340 Lunch, 1600-1700 Exhibition Break (1600-1630 IP3)					
	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
0830 to 1000	5.1 SMART DEVICES EMBEDDED TUTORIAL – Smart Devices for the Cloud Era	5.2 An Encyclopedia of Routing	5.3 Temperature and Variation Aware Design in Low Power Systems	5.4 Advanced NoC Tooling and Architectures	5.5 INDUSTRIAL 1	5.6 Analysis, Compilation and Runtime Techniques	5.7 EMBEDDED TUTORIAL – Architectures for Online Error Detection and Recovery in Multicore Processors	EXHIBITION OPENS AT 1000
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1100 to 1230	6.1.1 SMART DEVICES HOT TOPIC/EMBEDDED TUTORIAL – Ultra Low Power Smart Devices	6.2 Placement and Floorplanning	6.3 Power Modelling, Analysis and Optimisation	6.4 Design and Test of Fault Resilient NoC Architectures	6.5 New Techniques for Diagnosis and Debug	6.6 Embedded Software for Parallel Architectures	6.7 HOT TOPIC – Virtual Manycore Platforms: Moving Towards 100+ Processor Cores	6.8 PANEL SESSION – Embedded Software Debug and Test
1340	6.1.2 SPECIAL DAY KEYNOTE AND AWARDS 1340-1400 Awards and 1400-1430 Keynote, Room – Oisans							
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1430 to 1600	7.1 SMART DEVICES HOT TOPIC – Smart Medical Implants	7.2 Emerging Memory Technologies	7.3 Architectural Optimisation for Low Power Systems	7.4 Advanced Technologies for NoC Implementation	7.5 Emerging Test Solutions for Advanced Technologies, RF and MEMS Devices	7.6 Innovative Power-Aware Systems for a Green and Healthy Society	7.7 HOT TOPIC – Foundations of Component-Based Design for Embedded Systems	7.8 EMBEDDED TUTORIAL – Predictable System Integration
	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
1700 to 1830	8.1 SMART DEVICES PANEL SESSION – Integrating the Real World Interfaces	8.2 System-Level Design Techniques for Automotive Systems	8.3 Power/Error Tradeoffs	8.4 Memory System Architectures	8.5 Testing and Designing SRAM Memories	8.6 Cryptanalysis, Attacks and Countermeasures	8.7 HOT TOPIC – Flows, Application and Future of Component-based Design for Embedded Systems	8.8 EMBEDDED TUTORIAL – Communication Networks in Next Generation Automobiles

0730	REGISTRATION & SPEAKERS' BREAKFAST	BREAKS	1000-1100 Exhibition Break, (1000-1030 IP4), 1230-1330 Lunch, 1530-1600 Break (1530-1600 IP5)					
	SPECIAL TRACK	EMERGING TECHNOLOGIES	APPLICATIONS	DESIGN TECHNOLOGY	TEST	EMBEDDED SOFTWARE	SYSTEM DESIGN	SPECIAL SESSIONS
0830 to 1000	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	9.1 INTELLIGENT ENERGY MANAGEMENT TUTORIAL – Energy Transfer, Generation and Power Electronics	9.2 Design Automation Methodologies for Emerging Technologies	9.3 System Modelling	9.4 Modelling and Verification of Analogue and RF Circuits	9.5 INDUSTRIAL 2	9.6 Embedded System Resource Allocation and Management	9.7 EMBEDDED TUTORIAL – Sub-Wave Length Lithography and Variability Aware Test and Characterisation Methods	EXHIBITION OPENS AT 1000
1100 to 1230	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	10.1.1 INTELLIGENT ENERGY MANAGEMENT – Smart Energy Generation: Design Automation and the Smart-Grid	10.2 Advanced Algorithms and Applications for Reconfigurable Computing	10.3 System Optimisations and Adaptivity	10.4 Design and Simulation of Mixed-Signal Systems	10.5 Advances in Test Generation and Fault Simulation	10.6 Model Based Verification and Synthesis of Embedded Systems	10.7 EMBEDDED TUTORIAL – Die Stacking Goes Mobile and Embedded	10.8 PANEL SESSION –State of the Art Verification Methodologies in 2015
1330	10.1.2 SPECIAL DAY KEYNOTE, 1330-1400 Keynote, Room – Oisans							
1400 to 1530	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	11.1 INTELLIGENT ENERGY MANAGEMENT – Smart Energy Utilisation: From Circuits to Consumer Products	11.2 Architectural Innovations for Reconfigurable Computing	11.3 Asynchronous Circuits and Advanced Timing Issues in Logic Synthesis	11.4 High Level Synthesis	11.5 New Directions in Testing	11.6 Hardware Design for Multimedia Applications	11.7 HOT TOPIC – New Frontiers in Embedded Systems Design: Technology and Applications	11.8 HOT TOPIC – Stochastic Circuit Reliability Analysis in Nanometer CMOS
1600 to 1730	Room – Oisans	Room – Meije	Room – Belle-Etoile	Room – Stendhal	Room – Chartreuse	Room – Bayard	Room – Les Bans	Exhibition Theatre
	12.1 INTELLIGENT ENERGY MANAGEMENT PANEL SESSION – The Role of the EDA Community	12.2 Design and Run-Time Support for Dynamic Reconfigurability	12.3 Reliability and Error Tolerance in Logic Synthesis	12.4 Reliability and Error Tolerance in Logic Synthesis	12.5 Error Correction and Resilience	12.6 Security Modules from Layout to Network-on-Chip	12.7 HOT TOPIC – Sustainability through Massively Integrated Computing...	12.8 HOT TOPIC – Synthesis Supported Increase of Efficiency in Analogue Design

0730 **WORKSHOP REGISTRATION & WELCOME REFRESHMENTS**

BREAKS **Please see individual workshop programmes for lunch and break times**

	Room – Les Bans	Room – Meije	Room – Bayard	Room – Berlioz	Room – Stendhal	Room – 7 Laux 4	Room – Belle-Etoile	Room – Chartreuse
0830 TO 1700	W1 Workshop on Micro Power Management for Macro Systems on Chip (uPM2SoC)	W2 Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing	W3 Third Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications	W4 Bringing Theory to Practice: Predictability and Performance in Embedded Systems	W5 3D Integration – Applications, Technology, Architecture, Design, Automation, and Test	W6 M-BED'2011, the 2nd Workshop on Model Based Engineering for Embedded Systems Design	W7 Hardware Dependent Software Solutions for SoC Design	W8 1st International QEMU Users Forum (QUF)

Organiser: Luca Fanuci, Pisa U, IT

Eleven pre-conference tutorials will be given on Monday. Three are full-day tutorials (A, B and C). Eight are half-day tutorials, four to be given in the morning (D1, E, F1 and G1) and four in the afternoon (D2, E2, F2 and G2). A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.

The titles, organisers, speakers, and abstracts of the tutorials are given below:

0930 **FULL-DAY TUTORIALS – A, B, C**

A (Room - Belle-Etoile)

Low Power SoC Design: Best Practice – and what's next?

Organiser: David Flynn, ARM, UK

Speakers: David Flynn, ARM, UK
Alan Gibbons, Synopsys, UK
David Jacquet, ST-Ericsson, FR
José Pineda de Gyvez, NXP, NL
Praveen Raghavan, IMEC, BE

Low power design is an ever growing challenge and concern for designers, especially in battery powered consumer devices where both active and standby energy consumption and usable lifetime impact strongly on product success.

Active power management approaches such as Dynamic Voltage and Frequency Scaling, DVFS, are well understood but tough to put into practice industrially. Static power mitigation techniques such as Power Gating are increasingly required on advanced technology nodes with significant sub-threshold and gate leakage currents.

Over the last four or so years Electronic Design Automation tools have standardised on significant support for "multi-voltage" design and implementation and "power-intent" extensions to annotate RTL designs for supply voltage, power switching, isolating or clamping interfaces and inferring state retention.

In order to exploit these low power techniques effectively a system-level or architectural perspective increasingly matters in order to control and optimise the hardware layers of power management.

Understanding basic industrial best practice now, and how more advanced techniques can build on the existing multi-voltage tools support is a goal of this DATE 2011 tutorial that brings together presenters with a wealth of experience and expertise in real-world low power system design.

The invited presentations will cover theory and practice, starting with building blocks and components at the IP level and outlying methodologies for design, implementation and verification with the evolving power intent format standards (CPF and UPF).

Worked examples from multi-media and wireless application space will be addressed with a strong focus on practical design that works in production, and the areas of software and hardware partitioning and optimisation.

The tutorial will round off with a look at what is next on the low power roadmap for energy optimal design and research approaches to technology scaling and resilient and error tolerant design.

B **(Room - Chartreuse)**

Electronic System Level Design and Verification

Organisers: Thomas Bollaert, Mentor Graphics, US
Carole Dunn, Mentor Graphics, US

Speakers: Thomas Bollaert, Mentor Graphics, US
Yvan Desmartin, STMicroelectronics, FR
Michael Fingeroff, Mentor Graphics, US
Bernhard Niemann,
Fraunhofer Institute for Integrated Circuits, DE

Today's advanced designs have grown too massive and complex to cost-effectively design and verify using traditional RTL methods alone. Electronic System Level (ESL) design methods give designers the answers they need to overcome this dilemma. And of all the ESL methodologies flooding the market, the one technology that has gained considerable traction and use is high-level synthesis (HLS).

This tutorial explores the practical application of HLS with presentations from knowledgeable HLS users. In addition, Michael Fingeroff, the author of the High-Level Synthesis Blue Book, shares his guidance for how novices can go to experts by simply following the best practice coding examples shown in the book. Join us for a full-day of exploring how the promise of HLS is becoming a reality.

C **(Room - Les Bans)**

Manufacturing, CAD and Thermal-Aware Design for 3D System-on-Chip Design

Organisers: David Atienza, EPF Lausanne, CH
Yuan Xie, Penn State U, US

Speakers: David Atienza, EPFL, CH
Tanay Karnik, Intel, US
Jeonghee Shin, IBM, US
Sachin S Sapatnekar, U of Minessota, US
P Leduc, CEA-LETI, FR
Yuan Xie, Penn State U, US

Three-dimensional integration (3D) with stacked chips is emerging as an attractive solution for overcoming even further the barriers to interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology, with smaller form factor, higher integration density, and the support for the realisation of mixed-technology chips in multi-processor system-on-chip (MPSoC) designs. Consequently, 3D Integration technologies have become the focus of the recent semiconductor and IC design R&D activities world-wide, and recent advances in process technology have brought 3D technology to the point where it is feasible and practical, and it has raised widespread interest in the semiconductor and fab-less industry. However, adding the third dimension implies the redesign of EDA tools and design/architectural techniques to fully explore new approaches and address the additional challenges of the 3D manufacturing complexity. Moreover, 3D stacking creates even higher power and heat density, leading to degraded performance if thermal management is not handled properly in novel system-level design flows, which can combine mature multi-tier IC stacking manufacturing, appropriate 3D computer-aided design (CAD) tools and sensible hardware/software thermal-aware architectures for 3D MPSoCs.

The goal of this full-day tutorial is to provide a thorough overview of the complete design flow for 3D MPSoCs and mixed-design ICs, namely, starting from the 3D integration process technology up to the application and market drivers for 3D products, while covering the different system-level EDA related challenges in 3D MPSoCs, architectures for 3D MPSoC design and, finally, thermal modeling and management of MPSoC at the system level. Thus, this tutorial brings together leading 3D IC and MPSoC design experts in both industry/research centers (Intel, IBM, CEA-LETI) and academia (PennState, Univ. Minesota and EPFL), from both US and Europe, in order to cover in a comprehensive and structured way the key aspects of 3D technologies, design and products.

0930 **HALF-DAY TUTORIALS – D1, E1, F1, G1**

D1 **(Room - Meije 3)**

MPSoC Hardware/Software Architectural and Design Challenges/Solutions

Organiser: Bernard Candaele, Thales, FR

Speakers: Geert Vanmeerbeeck, IMEC, BE
Kari Tiensyrjä and Jari Kreku, VTT, FI
Axel Jantsch, KTH, SE
Dimitrios Soudris, ICCS, GR
Bernard Candaele and Sylvain Aguirre, Thales, FR

Multi-core SoCs are rapidly becoming main stream but raise numerous architectural hardware and software challenges in designing and programming. The tutorial will review state of the art, research and developments and next challenges for HW/SW architectures and design space exploration to implement multi-cores/many cores SoC or FPGA platforms for wireless and multimedia applications.

Mapping software onto multi-processor platforms requires efficient parallel programming techniques whilst achieving non-functional requirements. The fundamentals, design steps and alternative programming models to implement such embedded applications onto multi-cores are discussed and presented.

The need to accommodate a large number of applications on these massively parallel computing platforms requires the system engineer to quickly evaluate the performances of application mappings. The tutorial will review mainstream evaluation techniques based on simulation, abstract workload and processing capacity models.

On-chip and in-package memory organisation and efficient data management are key to high performance. The tutorial will review various memory architectures and techniques to address space management, cache coherency, memory consistency, and dynamic application specific memory allocation techniques.

The tutorial will conclude with a case study in telecom, reviewing current related studies and next challenges.

In summary, the tutorial will focus on the following topics:

- High level design space exploration of heterogeneous and customisable multi-core architecture based on abstract architecture and workload models representing the applications;
- Options and implications of the on-chip memory architecture covering central, distributed, private, and shared organisations;
- On-chip memory architectures and application specific dynamic memory allocation techniques for the considered multi-core architectures.

E1 **(Room - 7 Laux 4)**

On-chip Interconnect for New Generation of SoC

Organisers: Marcello Coppola, STMicroelectronics, FR
Miltos Grammatikakis, TEI of Crete, GR

Speakers: Reinig Helmut, Infineon, DE
Luca Carloni, Columbia University, US
Raj Yavatkar, Intel, US
Michael Dimelow, ARM, UK
Philippe D'audigier, STMicroelectronics, FR

On-chip interconnect design for embedded systems is moving away from traditional shared buses, such as AMBA AHB, IBM CoreConnect and STMicroelectronics STBus, towards sophisticated point-to-point communication architectures enriched by a set of services. The proliferation of multicore system-on-chip (SoC) and the desire to effectively consolidate applications in standardised platforms are driving forces of on-chip interconnect evolution. On-chip interconnects can benefit from knowledge transfer of PC, communication server and IT industry by embracing several well-known technologies. However, due to critical challenges from complex applications and deep submicron technology, we must completely rethink our use cases and provide further enhancements for on-chip interconnects. New principles, constraints and processes are necessary for optimising system-level reuse, wire density, gate complexity, reliability, performance, scalability, power-efficiency and thermal management within the on-chip domain.

Within this context, this tutorial aims to evaluate the effectiveness of emerging innovative design methodologies, tools and leading-edge industrial practices for the evolution of on-chip interconnects in current state-of-the-art and next generation multicore SoC. Active researchers and well-established design managers firmly rooted in business realities and in tune with future trends will present important aspects and challenges within the vast and ever-changing world of on-chip interconnect technology, providing real life SoC examples.

A balanced, well-organised structure with strongly-connected presentations accompanied by numerous illustrations and easy-to-understand examples will foster well-focused information exchange to the general embedded community, providing ample time for questions. The target audience includes mainly CS/EE professionals (e.g. hardware engineers, SoC architects and managers), as well as semiconductor vendors and investors.

F1 **(Room - 7 Laux 5)**

Renewable Energy: Solar Power Generation, Conversion and Delivery

Organisers: Roberto Zafalon, STMicroelectronics, IT
Francesco G Gennaro, STMicroelectronics, IT

Speakers: Francesco G Gennaro, STMicroelectronics, IT
Gianluca Gigliucci, Enel, IT
Salvatore Lombardo, IMM - CNR, IT
Lars Bomholt, Synopsys, CH

Efficient generation, distribution and management of electric energy can reduce consumption in Europe from 20% to 30% by 2020 and CO2 emission in the same order of magnitude to achieve the Kyoto protocol targets and to limit the energy cost increase.

Solar energy generation proves to be a sustainable and efficient policy for global CO2 reduction. When coupled with the "Smart Energy Grid", it gives a reliable, flexible, accessible and yet cost-effective power source.

The Tutorial focuses on the solar energy supply chain, ranging from solar cells to innovative energy harvesting techniques, high efficiency power conversion and energy delivery through the smart grid.

The state-of-the-art and future trends of solar cells technology will be discussed, from standard Si cells to ultra-thin (20um) Si wafer PV cells, Si heterojunction cells, novel architectures (e.g. back-contact), new materials (for ARC, and passivation dielectrics), screen printing, laser processing and fully printable Dye-Sensitized-Solar Cells (DSSC). Next to the technology overview, the current status and features of system simulation of photovoltaic solutions using Synopsys TCAD Sentaurus for solar cell design and Saber for PV system simulation will be provided, suitable to model the thermally induced variations in performance.

Power conversion and control system design will be then addressed for a variety of cell technologies, with a special focus on Maximum Power Point Tracking operation.

Finally, energy delivery and transport will be the next challenge in the Smart Grid, with regards to management and control of electricity's exchange by means of communication infrastructure, either wired or wireless.

G1 **(Room - Meije 2)**

Power-Aware Testing and Test Strategies for Low Power Devices

Organisers: Yiorgos Makris, Yale U, US
Dimitris Gizopoulos, Piraeus U, GR

Speakers: Patrick Girard, LIRMM/CNRS, FR
Nicola Nicolici, McMaster U, CA
Xiaoqing Wen, Kyushu Institute of Technology, JP

Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organised into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2011

1430 **HALF-DAY TUTORIALS – D2, E2, F2, G2**

D2 (Room - Meije 3)

Model-based MPSoC Architecture Synthesis for Highly-demanding Embedded Applications

Organiser: Lech Jozwiak, TU Eindhoven, NL

Speakers: Lech Jozwiak, TU Eindhoven, NL
Menno Lindwer, SiliconHive, NL
Jan Madsen, TU Denmark, DK

The recent spectacular progress in modern nanoelectronic technology enabled implementation of very complex multiprocessor systems on single chips (MPSoCs) and created a big stimulus towards development of high-performance systems for various highly-demanding embedded applications. In result, the increasingly complex and sophisticated MPSoCs are required to perform real-time computations to extremely tight schedules, with high demands regarding energy, power, area, and cost efficiency. Moreover, they are required to be flexible enough to enable reuse among different product versions, adherence to evolving standards or user requirements, and easy modification during their development or even their field use. This all results in serious design and development challenges, such as: multi-objective MPSoC optimisation, resolution of numerous complex design tradeoffs, reduction of the design productivity gap, time-to market and development costs without compromising quality, etc. The opportunities created can effectively be exploited only through use of more adequate application-specific system architectures and more integrated system IP modules, supported by new system-level design methods and EDA tools. This tutorial focuses on mastering the automatic architecture synthesis and application mapping for heterogeneous customisable multi-processor systems-on-chip (MPSoCs) based on configurable and extensible application-specific instruction-set processors (ASIPs). The MPSoC design technology based on adaptable ASIPs is able to deliver high performance, high flexibility and low energy consumption at the same time. It is relevant for a very broad range of modern applications and applicable to several implementation technologies. The tutorial presents the results of our analysis of the main problems that have to be solved and challenges to be faced in design of such heterogeneous customisable MPSoCs for modern demanding applications. It discusses the problems of architecture synthesis and application mapping involving multi-objective optimisation, adequate exploitation of multiple trade-offs, and coherent development of computing, communication and memory sub-systems for complex hard real-time embedded MPSoCs, as well as, proposes the model-based semi-automatic architecture synthesis methods and EDA-tools that enable effective and efficient solution of these problems.

E2 (Room - 7 Laux 4)

Design and Verification Challenges for Automotive Electronics

Organiser: Riccardo Groppo, Centro Ricerche FIAT, IT

Speakers: Riccardo Groppo, Centro Ricerche FIAT, IT
Patrick Leteinturier, Infineon, DE
Erwan Hemon, Freescale, FR
Pascal Caunegre, Freescale, FR
Manfred Thanner, Freescale, FR
Franco Toto, STMicroelectronics, IT
Davide Appello, STMicroelectronics, IT
Matteo Sonza Reorda, Politecnico di Torino, IT

The increasing complexity of automotive electronics, both in terms of electronic control systems' architecture and the new generation of complex ICs, must meet ever more demanding vehicle's requirements. On one hand the request for higher computational performances is due to more complex real-time mathematical models meant to achieve a better system control (i.e. improved combustion process for CO2 reduction); furthermore these mathematical models can also be designed to serve as "virtual sensors" in order to limit an overall system cost which is increasing day by day due to fuel economy and clean transportation increasing demands: this has been the driving factor of multi-core microcontrollers' architecture. The request for a better system partitioning and computational balance has also lead to the development of a new generation of mixed A/D intelligent ICs. On the other hand the need for improved reliability and, most of all, safety levels together with the stringent target cost, typical of the automotive business, is creating one of the biggest challenges at the silicon makers. In fact, automotive systems must have a high level of functional safety and fault tolerance built-in to ensure dependable and predictable operation over the lifetime of the product, which will be more than 10 years. The automotive-specific ISO 26262 safety standard defines the maximum acceptable failure rates and fault tolerant features that should be considered in the design and implemented in the development process. As a consequence modern design techniques and methodologies must be used in order to achieve those targets and predict system behavior in case of fault. Hence the tutorial will present basic and more advanced topics that cover various aspects of these challenges in a comprehensive fashion. It will start with the OEM view of the challenges, then advanced design methodologies, high level modeling, verification and statistical screening techniques will be described. The approach towards functional safety will require adequate efforts in terms of formal verification. Finally, an exhaustive testing automation and verification phase must be planned.

F2 (Room - 7 Laux 5)

Overcoming CMOS Reliability Challenges: From Devices to Circuits and Systems

Organiser: Yu (Kevin) Cao, Arizona State U, US
Subhasish Mitra, Stanford U, US

Speakers: Yu (Kevin) Cao, Arizona State U, US
Georges Gielen, KU Leuven, BE
Subhasish Mitra, Stanford U, US
Sani Nassif, IBM, US

With extreme miniaturisation of CMOS circuits, factors such as transient errors, device degradation, and variability induced by manufacturing and operating conditions are becoming important. While design margins are being squeezed to achieve high energy efficiency, expanded design margins are required to cope with process variability and device degradation. Even if error rates stay constant on a per-bit basis, total chip-level error rates grow with the scale of integration. Moreover, difficulties with traditional burn-in can leave early-life failures unscreened. This tutorial will present a wide range of topics that cover various aspects of these challenges in a comprehensive fashion: starting from device-level reliability modeling and characterisation, all the way to techniques for designing globally-optimised robust circuits (both digital and analog) and systems. Innovations in EDA tools to overcome reliability challenges will also be discussed. By focusing on resilience techniques across multiple abstraction layers (often referred to as cross-layer resilience techniques), this tutorial will illustrate new opportunities in designing cost-effective robust systems of the future.

G2 (Room - Meije 2)

Testing TSV-Based 3D Stacked Ics

Organisers: Yiorgos Makris, Yale University, US
Dimitris Gizopoulos, Piraeus U, GR

Speakers: Erik Jan Marinissen, IMEC, BE
Yervant Zorian, Synopsys, US

Three-dimensional stacking of multiple integrated circuits has benefits in terms of combining heterogeneous technologies and achieving a small footprint. The semiconductor industry is preparing itself to make a major step forward in three-dimensional stacking, now that the technology of TSVs is becoming available. TSVs are conducting nails which extend out of the back-side of a thinned-down die, enabling the vertical interconnect to another die. TSVs are high-density, low-capacitance interconnects compared to traditional wire-bonds, and hence allow for many more interconnections between stacked dies, while operating at higher speeds and consuming less power. TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities. 3D-SICs combine a smaller form factor and lower overall manufacturing costs with many other compelling benefits, and hence their technology is quickly gaining ground.

Like all micro-electronic products, 3D-SICs need to be tested for manufacturing defects incurred during their many, high-precision, and hence defect-prone manufacturing steps. These tests should be both effective and cost-efficient. Solutions regarding test flow, test contents, and test access need to be developed before 3D-SICs can be brought to the market. Next to all basic and most advanced test technology issues, 3D-SICs have some unique new test challenges of their own. These challenges include (1) development of new fault models and corresponding tests for TSV-based interconnects and new 3D-induced intra-die defects, (2) wafer probing on small and numerous micro-bumps and/or TSV tips and pads under stringent damage requirements, (3) handling of and probing on wafers with thinned-die stacks, (4) the design, partitioning, and optimisation of DfT architectures that span across multiple dies, and (5) optimisation of the test flow for maximum effectiveness and lowest cost.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2011

Tutorials

MONDAY 14 MARCH, 2011

0730 **TUTORIAL REGISTRATION**
0800 **Tutorial Welcome Refreshments**

0930-1800

A (Room – Belle-Etoile)	**Low Power SoC Design: Best Practice – and what's next?**
B (Room – Chartreuse)	**Electronic System Level Design and Verification**
C (Room – Les Bans)	**Manufacturing, CAD and Thermal-Aware Design for 3D System-on-Chip Design**

0930

D1 (Room – Meije 3)	**MPSoC Hardware/Software Architectural and Design Challenges/Solutions**
E1 (Room – 7 Laux 4)	**On-chip Interconnect for New Generation of SoC**
F1 (Room – 7 Laux 5)	**Renewable energy: solar power generation, conversion and delivery**
G1 (Room – Meije 2)	**Power-Aware Testing and Test Strategies for Low Power Devices**

1430

D2 (Room – Meije 3)	**Model-based MPSoC Architecture Synthesis for Highly-demanding Embedded Applications**
E2 (Room – 7 Laux 4)	**Design and Verification Challenges for Automotive Electronics**
F2 (Room – 7 Laux 5)	**Overcoming CMOS Reliability Challenges: From Devices to Circuits and Systems**
G2 (Room – Meije 2)	**Testing TSV-Based 3D Stacked ICs**

Tutorial attendees should choose in advance one tutorial from D1, E1, F1 or G1, which take place in the morning, and/or one tutorial from D2, E2, F2 or G2, which take place in the afternoon. Those wishing to attend one of the full-day tutorials should choose in advance one of A, B or C. A participant should enrol for either one full-day tutorial or one morning and/or one afternoon half-day tutorial (it is possible to attend for a morning or afternoon only in the case of the half-day tutorials). Combination of a full-day tutorial with a half-day tutorial is not allowed. Additional tutorial information can be found on the web – www.date-conference.com.
All tutorials run in parallel in accordance with the timetable below.
Rooms will be signposted.

00730 - 0930	**Registration and Tutorial Welcome Refreshments** (Main Foyer)
0930 – 1100	**Tutorials**
1100 – 1130	**Break**
1130 – 1300	**Tutorials**
1300 – 1430	**Lunch Break**
1330	**CONFERENCE REGISTRATION BEGINS**
1430 – 1600	**Tutorials**
1600 – 1630	**Break**
1630 – 1800	**Tutorials**
1800 – 1930	**WELCOME RECEPTION** (Main Foyer)
1900 – 2100	**FRINGE TECHNICAL MEETINGS**

technical programme

TUESDAY 15 MARCH, 2010

0730 REGISTRATION and SPEAKERS' BREAKFAST

1.1 Plenary: Opening and Keynote

Auditorium Dauphine **0830-1030**

Session Chair: B M Al-Hashimi, Southampton U, UK

0830 **OPENING REMARKS AND AWARDS**

B M Al-Hashimi, General Chair, Southampton U, UK
E Macii, Programme Chair, Politecnico di Torino, IT

Presentation of Distinguished Awards

0910 **BIOLOGICALLY-INSPIRED MASSIVELY-PARALLEL ARCHITECTURES – COMPUTING BEYOND A MILLION PROCESSORS**
S Furber, ICL Professor of Computer Engineering, School of Computer Science, Manchester U, UK

0950 **HOW TECHNOLOGY R&D LEADERSHIP BRINGS A COMPETITIVE ADVANTAGE IN THE FIELDS OF MULTIMEDIA CONVERGENCE AND POWER APPLICATIONS**
P Magarshack, Central R and D Vice-President, STMicroelectronics, FR

1030 **EXHIBITION BREAK**

Types of papers

Tracks 1, 2, 3, 4, 5, 6, 7 and 8 (except the executive sessions 2.1, 3.1 and 4.1) of the conference programme will present scientific papers that have been reviewed based on their contribution in scientific innovation. Long presentation papers are allocated a 30-minute time slot for presentation and questions. Short presentation papers are allocated a 15-minute time slot for presentation and questions. All papers are published in the DATE 11 Proceedings on DVD.

Track IP contains the interactive presentations which are scientific papers that have been reviewed based on the criteria of presenting work in progress. The Interactive Presentation papers will be presented in 5 separate IP Sessions which will be held in the Salle de Reception and will also each be introduced in a brief one-minute presentation during the relevant session prior to the IP Session. These papers are also published in the DATE 11 Proceedings on DVD.

(A) = Best Paper Award Candidate

IP = Interactive presentation

2.1 EXECUTIVE SESSION - Ideas on Future of EDA and IP Industry

Room – Oisans **1130-1300**

Organiser:
Yervant Zorian,
Synopsys, US

Moderator:
Peggy Aycinena,
EDA Confidential, US

Executives:
A Bose, President & CEO, Atrenta, US
J Bruggeman, Chief Marketing Office, Cadence, US
K Flautner, VP R&D, ARM, UK
C Heer, Vice President, Infineon, DE
J Kunkel, Senior VP & GM, Synopsys, US
Naveed Sherwani, President & CEO, Open Silicon, US

Designing today's emerging chips necessitates advanced methods and flows, which include the utilisation of a coherent set of IP blocks and interoperable EDA tools. This impacts today's IP and EDA industries and results in new solutions based on technical and business alliances and convergence. This session will discuss the above topic and address the upcoming challenges.

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.2 System-Level Techniques to Handle Performance, Reliability and Thermal Issues

Room – Meije **1130-1300**

Moderators:
D Goswami, TU Munich, DE
T Stefanov, Leiden U, NL

This session is on novel techniques to optimise system performance and reliability. The first paper is on using emulation to evaluate the impact of PVT-variability on system performance. The second paper describes how to reduce the number of simulations while performing thermal analysis of systems. The third paper proposes techniques for improving the endurance of NAND Flash memory. The fourth paper describes register index remapping techniques to optimise energy and temperature.

1130 **VESPA: VARIABILITY EMULATION FOR SYSTEM-ON-CHIP PERFORMANCE ANALYSIS**
V Kozhikkottu, R Venkatesan and A Raghunathan, Purdue U, US
S Dey, UCSD, US

1200 **THERMAL-AWARENESS ON-LINE TASK ALLOCATION FOR 3D MULTI-CORE PROCESSOR THROUGHPUT OPTIMISATION**
C L Lung, National Tsing-Hua U & ITRI, Taiwan, ROC
Y L Ho and S C Chang, National Tsing-Hua U, ROC
D M Kwai, ITRI, ROC

1230 **ENDURANCE-ENHANCED FLASH TRANSLATION LAYER FOR NAND FLASH MEMORY THROUGH REUSE STRATEGY**
Y Wang, D Liu, Z Qin and Z Shao,
The Hong Kong Polytechnic U, HK

1245 **REGISTER ALLOCATION FOR SIMULTANEOUS REDUCTION OF ENERGY AND PEAK TEMPERATURE ON REGISTERS**
T Liu, M Li and C J Xue, City U of Hong Kong, HK

IPs **IP1-1, IP1-8 AND IP1-9**

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.3 Modelling and Simulation of Interconnects

Room – Belle-Etoile **1130-1300**

Moderators:
W Schilders, TU Eindhoven, NL
S Grivet-Talocia, Politecnico di Torino, IT

In this session, several methods for interconnect analysis are presented. The emphasis is on model extraction via order reduction or identification, and on statistical analysis. The first paper presents a parallel algorithm for fast verification of model passivity. The second paper proposes an efficient methodology for computing statistical properties of interconnects without resorting to sampling based approaches. The two short papers and the interactive presentations address modelling, simulation and architecture of power grid networks.

1130 (A) **A PARALLEL HAMILTONIAN EIGENSOLVER FOR PASSIVITY CHARACTERISATION AND ENFORCEMENT OF LARGE INTERCONNECT MACROMODELS**
L Gobbato, A Chinea and S Grivet-Talocia,
Politecnico di Torino, IT

1200 **FAST STATISTICAL ANALYSIS OF RC NETS SUBJECT TO MANUFACTURING VARIABILITIES**
Y Bi, K-J Van Der Kolk and N Van Der Meijs, TU Delft, NL
J Fernandez Villena and L M Silveira,
INESC ID / IST, TU Lisbon, PT

1230 **A SCALED RANDOM WALK SOLVER FOR FAST POWER GRID ANALYSIS**
B Boghrati and S Sapatnekar,
U of Minnesota, Minneapolis, US

1245 **A BLOCK-DIAGONAL STRUCTURED MODEL REDUCTION SCHEME FOR POWER GRID NETWORKS**
Z Zhang, Massachusetts Institute of Technology, US
X Hu and C-K Cheng, UC San Diego, US
N Wong, The U of Hong Kong, HK

IPs **IP1-2 AND IP1-3**

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.4 PANEL AND EMBEDDED TUTORIAL SESSION – Logic Synthesis and Place and Route: After 20 Years of Engagement, Wedding in View?

Room – Stendhal **1130-1300**

Organiser:
M Casale-Rossi, Synopsys, US

Moderator:
A Domic, Synopsys, US

INTRODUCTION – Evolution and Trends in Design Implementation

G De Micheli, EPF Lausanne, CH

Pannellists:
G De Micheli, EPF Lausanne, CH
P Groeneveld, Magma Design Automation, US
H Hiller, Infineon, DE
E Macii, Politecnico di Torino, IT
P Magarshack, STMicroelectronics, FR

The first half of the 80's marked a fundamental milestone in the history of design implementation: an amazing number of key research papers were published, in a relatively short period of time; suddenly, logic synthesis, placement, and routing algorithms reached a maturity level which enabled the birth of the first wave of modern EDA companies and design implementation tools: Silvar-Lisco, Cadence, Synopsys, Tangent…

Some of them have disappeared, some others have been acquired, some are still standing out there, after 30 years and 15 silicon process' technology nodes – we went from 3 microns and ~1K instances, to 22 nanometers and 100M instances, with timing and power progressively moving away from the gate into the wire. How have EDA companies and their tools adapted themselves to the change? What else can be done, moving forward?

Professor Giovanni De Micheli will give the introduction and describe where do we stand, why, and what are the hottest research topics. Dr Antun Domic, will moderate the panel of university and industry experts who will discuss what new links are needed between logic synthesis and place & route, and whether a closer – exclusive ? – relationship is inevitable, or...

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.5 Transient Faults and Soft Errors

Room – Chartreuse **1130-1300**

Moderators:
D Appello, STMicroelectronics, IT
C Metra, Bologna U, IT

New approaches for transient fault analysis and soft error concurrent detection are presented.

1130 **TIME REDUNDANT PARITY FOR LOW-COST TRANSIENT ERROR DETECTION**
D J Palframan, N S Kim and M H Lipasti, Wisconsin-Madison U, US

1200 **CROSS-LAYER OPTIMISED PLACEMENT AND ROUTING FOR FPGA SOFT ERROR MITIGATION**
K Huang, Y Hu andX Li, Institute of Computing Technology, CAS, PRC

1230 **TRIGONOMETRIC METHOD TO HANDLE REALISTIC ERROR PROBABILITIES IN LOGIC CIRCUITS**
C-C Yu and J P Hayes, U of Michigan, Ann Arbor, US

1245 **SOFT ERROR RATE ESTIMATION OF DIGITAL CIRCUITS IN THE PRESENCE OF MULTIPLE EVENT TRANSIENTS (METS)**
M Fazeli, S N Ahmadian, S G Miremadi and H Asadi, Sharif U of Technology, IR
M B Tahoori, Karlsruhe Institute of Technology, DE

IP **IP1-4**

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.6 Networked Embedded Systems

Room – Bayard **1130-1300**

Moderators:
L Almeida, Porto U, PT
P Puschner, TU Vienna, AT

This session addresses different issues in designing networked embedded systems. The first paper considers FlexRay systems based on a switch and proposes a global traffic scheduling method that allows increasing the total throughput while being scalable by mixing an ILP optimisation technique with an adequate heuristic. The second paper develops in the same scope of FlexRay-based systems and proposes a heuristic that determines possible reconfigurations needed to tolerate node failures and encodes them in the initial system static configuration. Node failures can then be tolerated by using redundant slots and/or combining messages in existing frames and slots. The third paper addresses applications programming in wireless sensor networks and proposes extending the programming language in a way to allow the automatic generation of fault detection and tolerance code based on a transformation of the specification.

1130 **FLEXRAY SWITCH SCHEDULING - A NETWORKING CONCEPT FOR ELECTRIC VEHICLES**
M Lukasiewycz and S Chakraborty, TU Munich, DE
P Milbredt, AUDI AG, DE

1200 **A RECONFIGURATION APPROACH FOR FAULT-TOLERANT FLEXRAY NETWORKS**
K Klobedanz and W Mueller, Paderborn U/C-Lab, DE
A Koenig, Paderborn U, DE

1230 **SIMPLIFIED PROGRAMMING OF FAULTY SENSOR NETWORKS VIA CODE TRANSFORMATION AND RUN-TIME INTERVAL COMPUTATION**
L Bai and R P Dick, U of Michigan,US
P A Dinda, Northwestern U, US
P Chou, UC Irvine, US

IP **IP1-5**

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.7 Design of Energy-Efficient and Automotive Systems

Room – Les Bans **1130-1300**

Moderators:
K Danne, Intel
M Di Natale, Scuola S S Anna, IT

This session addresses designing for energy and power efficient systems on different levels. It covers circuit level aspects, architectural approaches as well as efficient runtime usage of computing devices. Also, methods and issues in the migration of serial-data communication to high-bandwidth Ethernet for the automotive and the use of formal specifications and models as enablers for testing automation.

1130 **PARALLEL ACCELERATORS FOR GLIMMERHMM BIOINFORMATICS ALGORITHM**
N Chrysanthou, G Chrysos, E Sotiriades and I Papaefstathiou, TU Crete, GR

1145 **AN EFFICIENT ON-LINE TASK ALLOCATION ALGORITHM FOR QOS AND ENERGY EFFICIENCY IN MULTICORE MULTIMEDIA PLATFORMS**
F Paterna, A Caprara and L Benini, DEIS - Bologna U, IT
A Acquaviva, DAUIN – Politecnico di Torino, IT
F Papariello and G Desoli, ST Microelectronics, IT

1200 **SUB-CLOCK POWER-GATING TECHNIQUE FOR MINIMISING LEAKAGE POWER DURING ACTIVE MODE**
J N Mistry and B M Al-Hashimi, Southampton U, UK
D Flynn and S Hill, ARM Ltd, UK

1230 **AN AUTOMATED DATA STRUCTURE MIGRATION CONCEPT - FROM CAN TO ETHERNET/IP IN AUTOMOTIVE EMBEDDED SYSTEMS (CANOVERIP)**
A Kern and T Streichert, Daimler AG, DE
J Teich, Erlangen-Nuremberg U, DE

1245 **FORMAL SPECIFICATION AND SYSTEMATIC MODEL-DRIVEN TESTING OF EMBEDDED AUTOMOTIVE SYSTEMS**
S Siegl, INI.FAU, DE
C Berger, Automotive Safety Technologies GmbH, DE
G Kiffe, AUDI AG, DE
K-S Hielscher and R German, Erlangen-Nuremberg U, DE

IP **IP1-6 AND IP1-10**

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

2.8 EMBEDDED TUTORIAL – Addressing Critical Power Management Verification Issues in Low Power Designs

Room – Exhibition Theatre **1130-1300**

Organiser:
B Kapoor, Mimasic, US

Moderators:
K Just, Infineon, DE

Power management techniques that leverage voltage as a handle are being extensively used in power sensitive designs. These techniques include power gating, power gating with retention, multiple supply voltages, dynamic voltage scaling, adaptive voltage scaling, multi-threshold CMOS, and active body bias. The use of the power management techniques also imply new challenges in validation and testing of designs as new power states are created. We look into verification issues along with the solutions to these issues using a verification strategy that involves power-aware simulation, rule-based structural checking, formal tools, and methodology recommendations. We detail our varied experiences with various design teams in addressing these low power verification issues for applications such as the wireless handset, low power microprocessors, and GPS.

1130 **INTRODUCTION TO POWER MANAGEMENT TECHNIQUES AND ASSOCIATED VERIFICATION ISSUES**
B Kapoor, Mimasic, US

1145 **SOC POWER MANAGEMENT CHALLENGES**
J Goodenough, ARM, US

1215 **BEST PRACTICES IN LOW POWER DESIGN VERIFICATION METHODOLOGY**
P Tiwari, Synopsys, US

1245 **FUTURE TRENDS IN POWER MANAGEMENT DESIGN AND VERIFICATION**
S Verma, Conexant, US

1300 **LUNCH BREAK AND SPECIAL SESSION (SPONSORED BY MENTOR GRAPHICS)**

3.0

SPECIAL LUNCH-TIME SESSION – Grenoble EDA Ecosystem Session - From Research to Market

Auditorium Dauphine **1300-1400**

Moderator:
M Croft, Mentor Graphics, UK

Three views of the value of European Research to EDA and Semiconductors: CEA-LETI, ST and Mentor Graphics speak of the value of close cooperation in the EU.

1300 **FROM RESEARCH TO MARKET**
Laurent Malier, CEO, CEA-LETI, FR

With its research centers, university campus, 500 foreign companies and 40,000 scientists, engineers and technicians employed in the area, the Grenoble-Isère region, otherwise known as France's Silicon Valley, mixes world-class intellectual and scientific dynamism with exceptional quality of life. It is the ideal springboard for Academia-Industry collaboration. This presentation details collaboration schemes between Industry and research institutes and industry happening in Grenoble. This often involves long-term projects based on sharing research costs and requires joint technical programs with a predetermined timetable, with specific technology transfer and operating conditions.

1320 **SUCCESSFUL R&D COLLABORATIONS AS A COMPETITIVE ADVANTAGE**
Philippe Magarshack, Group Vice-President, Technology R&D - General Manager, Central CAD and Design Solutions, STMicroelectronics, FR

ST's Grenoble center was born as a spin-off from a Grenoble research lab several decades ago. Since then, we have continued to maintain our innovation leadership with long-term Public-Private Partnerships in Grenoble, France and Europe. Starting in 1992, ST has partnered with its competitors to build its 200mm and 300mm R&D centers and fabs in Crolles, near Grenoble. In 2008, ST joined ISDA alliance in Fishkill NY to collaborate to its 32/28nm and 20nm CMOS processes. More recently, ST has reinforced and enlarged the scope of its local R&D partnership to Design and Design Automation. This complete eco-system is now bringing valuable innovation to our products and our customers.

1340 **INVESTING IN THE TOP TALENT FOR EDA**
Eric Selosse, Vice-President and General Manager, Emulation Division, Mentor Graphics, FR

Mentor Graphics has a long track record of investing in Europe for R&D expertise. Over the last year, despite the economic conditions, we have continued to recruit in France, the UK and Poland. Our industry is a meritocracy which relies on the hiring, nurturing and retention of the best world-class engineers available in electronics and associated fields. This presentation will outline why we invest in Europe, why France is such a significant part of this and look at the particular place Grenoble has in this story.

1400 **CLOSE**

3.1 EXECUTIVE SESSION – 22nm Challenges and Wealth/Knowledge Creation Opportunities

Room – Oisans **1430-1600**

Organiser:
Yervant Zorian,
Synopsys, US

Moderators:
Antun Domic,
Senior Vice President & GM, Synopsys, US

Executives:
Rudy Lauwereins, IMEC, BE
Maria Marced, President, TSMC Europe, NL
Leon Stok, Vice President, IBM, US
Gerd Teepe, Vice President, Global Foundries, DE

The continuously nanometer scaling in semiconductor technology with its 22nm and below can dramatically impact business performance of semiconductor industry. It can also significantly affect age-old IC design and manufacturing flows. The executives in this session will discuss future trends and upcoming changes in the semiconductor industry and their impact on the IC value chain.

1600 **EXHIBITION BREAK/IP1**

3.2 Power Optimisation of Multi-Core Architectures

Room – Meije **1430-1600**

Moderators:
C Piguet, CSEM, CH
M Lopez-Vallejo, UP Madrid, ES

This session contains papers about the power-aware design of multicore architectures regarding voltage-frequency assignments for each core, process variations, thermal management and task management through tiny O.S.

1430 (A) **TOPOLOGICALLY HOMOGENEOUS POWER-PERFORMANCE HETEROGENEOUS MULTICORE SYSTEMS**
K Chakraborty and S Roy, Utah State U, US

1500 **VARIABILITY-AWARE DUTY CYCLE SCHEDULING IN LONG RUNNING EMBEDDED SENSING SYSTEMS**
L Wanner, R Balani, S Zahedi, C Apte, P Gupta and M Srivastava, UCLA, US

1530 **RELIABILITY-AWARE THERMAL MANAGEMENT FOR MANY-CORE PROCESSORS**
V Hanumaiah and S Vrudhula, Arizona State U, US

1600 **EXHIBITION BREAK/IP1**

3.3 Core Algorithms for Formal Verification Engines

Room – Belle-Etoile **1430-1600**

Moderators:
S Quer, Politecnico di Torino, IT
S Seshia, UC Berkeley, US

Today's formal verification environments heavily rely on core algorithms for logical reasoning at the Boolean (SAT and QBF) or higher (SMT) levels. The papers in this session present advances in each of these domains, paving the way towards new applications and verification engines of increased capacity.

1430 **CLAUSE SIMPLIFICATION THROUGH DOMINATOR ANALYSIS**
H Han and F Somenzi, U of Colorado at Boulder, US
H Jin, Cadence Design Systems, US

1500 **INTEGRATION OF ORTHOGONAL QBF SOLVING TECHNIQUES**
S Reimer, F Pigorsch, C Scholl and B Becker, Albert-Ludwigs-U Freiburg, DE

1530 **STABLE A NEW QF-BV SMT SOLVER FOR HARD VERIFICATION PROBLEMS COMBINING BOOLEAN REASONING WITH COMPUTER ALGEBRA**
E Pavlenko, F Seelisch, D Stoffel, M Wedler, G-M Greuel and W Kunz, Kaiserslautern U, DE
A Dreyer, Fraunhofer ITWM, Kaiserslautern, DE

1600 **EXHIBITION BREAK/IP1**

3.4 Predicting Bugs and Generating Tests for Validation

Room – Stendhal **1430-1600**

Moderators:
D Grosse, Bremen U, DE
V Bertacco, U of Michigan, US

The session proposes novel ideas to predict functional bug location and generating tests automatically to support validation efforts. We open the session with a paper that leverages predictive models to locate bugs in a sequence of design versions. The following two papers leverage property decomposition and assertion mining to guide the generation of high quality validation tests. Finally, we will discuss a work on validating embedded software.

1430 **EMPIRICAL DESIGN BUGS PREDICTION FOR VERIFICATION**
Q Guo, T Chen, H Shen, Y Chen, W Hu and Y Wu
Chinese Academy of Sciences (ICT/CAS), PRC

1500 **DECISION ORDERING BASED PROPERTY DECOMPOSITION FOR FUNCTIONAL TEST GENERATION**
M Chen, East China Normal U, PRC
P Mishra, Florida U, US

1530 **TOWARDS COVERAGE CLOSURE: USING GOLDMINE ASSERTIONS FOR GENERATING DESIGN VALIDATION STIMULUS**
L Liu, D Sheridan, W Tuohy and S Vasudevan, U of Illinois, Urbana-Champaign, US

1545 **SCALABLE HYBRID VERIFICATION FOR EMBEDDED SOFTWARE**
J Behrend, D Lettnin, P Heckeler, J Ruf, T Kropf and W Rosenstiel, Tuebingen U, DE

IP **IP1-7**

1600 **EXHIBITION BREAK/IP1**

3.5 Timing Related Issues in Test

Room – Chartreuse **1430-1600**

Moderators:
H-J Wunderlich, Stuttgart U, DE
S K Goel, TSMC, US

The first paper proposes a technique to characterise the impact of timing faults by analysing the phase movement of scan patterns. The second one presents a non-scan DFT approach to enhance the fault coverage by using both outputs of a subset of flipflops. Finally, a low area overhead controller is presented for clock gating to avoid power droop during scan capture.

1430 **DIAGNOSING SCAN CHAIN TIMING FAULTS THROUGH STATISTICAL FEATURE ANALYSIS OF SCAN IMAGES**
M Chen and A Orailoglu, UC San Diego, US

1500 **DESIGN-FOR-TEST METHODOLOGY FOR NON-SCAN AT-SPEED TESTING**
M Banga, N Rahagude and M S Hsiao, Virginia Tech, US

1530 **A CLOCK-GATING BASED CAPTURE POWER DROOP REDUCTION METHODOLOGY FOR AT-SPEED SCAN TESTING**
S Sarangi, C Liu, B Yang and A Sanghani, NVIDIA Corp, US

1600 **EXHIBITION BREAK/IP1**

3.6 Performance and Timing Analysis

Room – Bayard **1430-1600**

Moderators:
H Falk, TU Dortmund, DE
R Wilhelm, Saarland U, DE

In many embedded systems the timing assessment of tasks and entire systems is of utmost importance. The first paper introduces a method for assessing the response-time behaviour of synchronous real-time programs.

By employing model checking and infeasible-path pruning the authors manage to handle the state spaces of concurrent application efficiently. The second and third papers present novel source code instrumentation techniques in order to improve the accuracy when simulating transaction level models (TLM). The major novelty is a mapping between the control flows at source code level and binary level. The fourth paper presents a simulator for embedded real-time systems targeting multi-core platforms. The simulator provides a means for an early exploration of configuration options for both the operating system and application tasks in such a distributed real-time environment.

1430 **PRUNING INFEASIBLE PATHS FOR TIGHTER WCRT ANALYSIS OF SYNCHRONOUS PROGRAMS**
S Andalam and P S Roop, Auckland U, NZ
A Girault, INRIA, FR

1500 **FAST AND ACCURATE RESOURCE CONFLICT SIMULATION FOR PERFORMANCE ANALYSIS OF MULTI-CORE SYSTEMS**
S Stattelmann and O Bringmann, FZI Karlsruhe, DE
W Rosenstiel, Tuebingen, DE

1530 **AN APPROACH TO IMPROVE ACCURACY OF SOURCE-LEVEL TLMS OF EMBEDDED SOFTWARE**
Z Wang, K Lu and A Herkersdorf, TU Munich, DE

1545 **HOST-COMPILED MULTICORE RTOS SIMULATOR FOR EMBEDDED REAL-TIME SOFTWARE DEVELOPMENT**
P Razaghi and A Gerstlauer, U of Texas at Austin, US

1600 **EXHIBITION BREAK/IP1**

3.7 Implementations for Digital Baseband Processing

Room – Les Bans **1430-1600**

Moderators:
F Kienle, TU Kaiserslautern, DE
F Clermidy, CEA-LETI, FR

In this session new techniques for digital communication systems are presented. Three papers deal with multiple-input multiple-output (MIMO) detectors exploiting different implementation approaches. One paper presents a flexible channel decoder based on application specific instruction set multiprocessor design.

1430 **A FLEXIBLE HIGH THROUGHPUT MULTI-ASIP ARCHITECTURE FOR LDPC AND TURBO DECODING**
P Murugappa, R Al-Khayat, A Baghdadi and M Jezequel, TELECOM Bretagne; UMR CNRS, FR

1500 **A LOW-POWER VLIW PROCESSOR FOR 3GPP-LTE COMPLEX NUMBERS PROCESSING**
F Clermidy and C Bernard, CEA-LETI, FR

1530 **ARCHITECTURE AND FPGA-IMPLEMENTATION OF A HIGH THROUGHPUT K+-BEST DETECTOR**
N Heidmann and T Wiegand, Bremen U, DE

1545 **A LOW-AREA LOW-POWER 2X2 64-QAM SPHERE DECODER**
N Moezzi-Madani, T Thorolfsson and W R Davis, North Carolina State U, US
J Crop and P Chiang, Oregon State U, US

1600 **EXHIBITION BREAK/IP1**

3.8 PANEL SESSION – Power Formats: Beyond UPF and CPF

Room – Exhibition Theatre 1430-1600

Organiser/Moderator:
B Pangrle, Mentor Graphics, US

Panellists:
J Biggs, ARM, UK
C Clavel, ST-Ericsson, FR
O Domerego, Texas Instruments, FR
K Just, Infineon/Intel, DE
B Moison, STMicroelectronics, FR

Two formats for specifying power intent are currently in wide use in industry today and as designers continue to strive for more power efficient designs new issues arise that certainly need new solutions to improve on today's standards. This panel will discuss areas for improving today's power formats and the direction that these formats need to move in order to provide the most efficient flows for design and verification and especially with regards to low-power. The scope of the formats and their suitability from early ESL design exploration to back-end sign-off checking will also be discussed along with any issues that need to be addressed in order to make design and verification engineers more productive.

1600 **EXHIBITION BREAK/IP1**

IP1 Interactive Presentations

Room - Salle de Reception 1600-1630

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP1-1 **BUFFERING IMPLICATIONS FOR THE DESIGN SPACE OF STREAMING MEMS STORAGE**
M G Khatib, Twente U, NL

IP1-2 **EFFICIENT RC POWER GRID VERIFICATION USING NODE ELIMINATION**
A Goyal and F N Najm, Toronto U, CA

IP1-3 **A NOVEL TSV TOPOLOGY FOR MANY-TIER 3D POWER-DELIVERY NETWORKS**
M B Healy and S K Lim, Georgia Institute of Technology, US

IP1-4 **COST-EFFICIENT FAULT-TOLERANT DECODER FOR HYBRID NANOELECTRONIC MEMORIES SYSTEM**
N Z Haron and S Hamdioui, TU Delft, NL

IP1-5 **DYNOAA - DYNAMIC OFFSET ADAPTATION ALGORITHM FOR IMPROVING RESPONSE TIMES OF CAN SYSTEMS**
T Ziermann and J Teich, Erlangen-Nuremberg U, DE
Z Salcic, Auckland U, NZ

IP1-6 **A SENSOR FUSION ALGORITHM FOR AN INTEGRATED ANGULAR POSITION ESTIMATION WITH INERTIAL MEASUREMENT UNITS**
S Sabatelli and A Rocchi, SensorDynamics AG, IT
L Fanucci, Pisa U, IT

IP1-7 **DYNAMIC BINARY TRANSLATION OF SIMD INSTRUCTIONS TO SPEED-UP EMBEDDED PROCESSOR SIMULATION**
L Michel,N Fournel and F Petrot,
TIMA Laboratory, CNRS/INP Grenoble/UJF, FR

IP1-8 **SYSTEM-LEVEL ENERGY-EFFICIENT SCHEDULING FOR HARD REAL-TIME EMBEDDED SYSTEMS**
L Niu, Claflin U, US

IP1-9 **TIMING ERROR STATISTICS FOR ENERGY-EFFICIENT ROBUST DSP SYSTEMS**
R Abdallah and N Shanbhag,
U of Illinois at Urbana Champaign, US

IP1-10 **SCTMR: A SCAN CHAIN-BASED ERROR RECOVERY TECHNIQUE FOR TMR SYSTEMS IN SAFETY-CRITICAL APPLICATIONS**
M Ebrahimi, S G Miremadi and H Asadi,
Sharif U of Technology, IR

4.1 EXECUTIVE SESSION - System Level Complexity and Innovation

Room – Oisans **1700-1830**

Organiser:
Yervant Zorian,
Synopsys, US

Moderator:
Garry Smith,
Gary Smith EDA, US

Executives:
Simon Bloch, VP & GM, Mentor Graphics. US
Donald Friedberg, VP, LSI, US
Philippe Magarashack, VP, STMicroelectronics, FR
Amit Majumdar, Fellow, AMD, US
Raj Yavatkar, Fellow, Intel, US

The widening gap between growing system complexity, designer productivity, and embedded software increasingly limits traditional system design methods and flows. This results in several new approaches and innovative methods that work to elevate the limitations of different aspects of system design.

Executives from the IC value chain will present the technical and business challenges and the new opportunities in designing today's complex systems.

1830 **CLOSE**

4.2 Robust and Low Power Systems

Room – Meije **1700-1830**

Moderators:
C Silvano, Politecnico di Milano, IT
M Berekovic, TU Braunschweig, DE

This session features six papers that work to improve system power and robustness. Techniques are presented to optimise the thermal and power characteristics of chip multiprocessors and 3D architectures. In addition, work is presented that allows designs to tolerate voltage emergencies and design errors in SoCs.

1700 **ENABLING IMPROVED POWER MANAGEMENT IN MULTICORE PROCESSORS THROUGH CLUSTERED DVFS**
T Kolpe, A Zhai and S S Sapatnekar, Minnesota U, US

1730 **DYNAMIC THERMAL MANAGEMENT IN 3D MULTI-CORE ARCHITECTURE THROUGH RUN-TIME ADAPTATION**
F Hameed, M A Al Faruque and J Henkel,
Karlsruhe Institute of Technology, DE

1800 **DISTRIBUTED HARDWARE MATCHER FRAMEWORK FOR SOC SURVIVABILITY**
I Wagner and S-L Lu, Intel, US

1815 **A COST-EFFECTIVE SUBSTANTIAL-IMPACT-FILTER BASED METHOD TO TOLERATE VOLTAGE EMERGENCIES**
S Pan, X Hu, Y Hu and X Li,
Chinese Academy of Sciences, PRC

IPs **IP2-1 AND IP2-8**

1830 **CLOSE**

4.3 Formal Verification Techniques and Applications

Room – Belle-Etoile **1700-1830**

Moderators:
M Wedler, Kaiserslautern U, DE
C Scholl, Freiburg U, DE

This session proposes extensions to model checking, its usage and applications. The first paper presents an improvement to SAT-based unbounded model checking. The second paper proposes the use of mutation techniques to facilitate the identification of flaws in design specifications. The third paper tackles the problem of automatically synthesising and verifying buffer sizes for NoCs, with a novel use of SMT-based model checking.

1700 **INTERPOLATION SEQUENCES REVISITED**
G Cabodi, S Nocco and S Quer, Politecnico di Torino, IT

1730 **AUTOMATED DEBUGGING OF SYSTEMVERILOG ASSERTIONS**
B Keng and A Veneris, Toronto U, CA
S Safarpour, Vennsa Technologies Inc, CA

1800 **COUNTEREXAMPLE-GUIDED SMT-DRIVEN OPTIMAL BUFFER SIZING**
B A Brady, D Holcomb and S A Seshia, UC Berkeley, US

IPs **IP2-2 AND IP2-9**

1830 **CLOSE**

4.4 System Level Simulation and Validation

Room – Stendhal **1700-1830**

Moderators:
F Fummi, Verona U, IT
P Sanchez, Cantabria U, ES

The session presents simulation and validation techniques working at system level. In particular, the first paper approaches simulation for OS preemptive scheduling while the second proposes an accurate system level simulation. The last two papers deal with speeding up multi-core architectures simulation.

1700 **DOM: A DATA-DEPENDENCY-ORIENTED MODELING APPROACH FOR EFFICIENT SIMULATION OF OS PREEMPTIVE SCHEDULING**
P-C Wang, M-H Wu and R-S Tsay,
National Tsing-Hua U,Taiwan, ROC

1730 **CYCLE-COUNT-ACCURATE PROCESSOR MODELING FOR FAST AND ACCURATE SYSTEM-LEVEL SIMULATION**
C-K Lo, L-C Chen, M-H Wu and R-S Tsay,
National Tsing-Hua U, Taiwan, ROC

1800 **A SHARED-VARIABLE-BASED SYNCHRONISATION APPROACH TO EFFICIENT CACHE COHERENCE SIMULATION FOR MULTI-CORE SYSTEMS**
C-Y Fu, M-H Wu and R-S Tsay,
National Tsing Hua U, Taiwan, ROC

1815 **SPEEDING UP MPSOC VIRTUAL PLATFORM SIMULATION BY ULTRA SYNCHRONISATION CHECKING METHOD**
Y-F Yeh, C-Y Huang, C-A Wu and H-C Lin,
National Taiwan U, Taiwan, ROC

IPs **IP2-3 AND IP2-10**

1830 **CLOSE**

4.5 Advances in Analogue, Mixed Signal and RF Testing

Room – Chartreuse **1700-1830**

Moderators:
A Richardson, Lancaster U, UK
H Stratigopoulos, IMAG, FR

The first paper deals with PLL BIST, followed by a paper on a power detector for RF circuits. Next advances in defect-oriented testing are discussed, and finally high-speed test generation is addressed. The IPs present high-speed test generation and DfT solutions.

1700 **AN ALL-DIGITAL BUILT-IN SELF-TEST TECHNIQUE FOR TRANSFER FUNCTION CHARACTERISATION OF RF PLLS**
P-Y Wang, National Taiwan U, Taiwan, ROC
H-M Chang and K-T Cheng, UC Santa Barbara, US

1730 **TRUE POWER DETECTOR FOR RF PA BUILT-IN CALIBRATION AND TESTING**
J Machado Da Silva and P Mota, INESC Porto, Porto U, PT

1745 **TEST TIME REDUCTION IN ANALOGUE/MIXED-SIGNAL DEVICES BY DEFECT ORIENTED TESTING: AN INDUSTRIAL EXAMPLE**
H Hashempour, J Dohmen, B Tasic, B Kruseman, C Hora, M Van Beurden and Y Xing,
NXP Semiconductors, NL

1815 **TESTING OF HIGH-SPEED DACS USING PRBS GENERATION WITH "ALTERNATE-BIT-TAPPING"**
M Singh, M Sakare and S Gupta, IIT Bombay, IN

IPs **IP2-4 AND IP2-11**

1830 **CLOSE**

4.6 Design Automation Methodologies and Architectures for Three-Dimensional ICs

Room – Bayard **1700-1830**

Moderators:
Y Xie, Penn State U, US
H Li, New York U, US

This session includes papers covering EDA and architectural techniques for emerging 3D IC technologies. The first paper presents statistical thermal evaluation and mitigation techniques for 3D CMP; the second paper explores design space for 3D staced DRAMs; the third paper presents a heat transfer model for TSVs; and the last paper presents novel power network design for 3D ICs.

1700 **STATISTICAL THERMAL EVALUATION AND MITIGATION TECHNIQUES FOR 3D CHIP-MULTIPROCESSORS IN THE PRESENCE OF PROCESS VARIATIONS**
D-C Juan, S Garg and D Marculescu, Carnegie Mellon U, US

1730 **DESIGN SPACE EXPLORATION FOR 3D-STACKED DRAMS**
C Weis and N Wehn, Kaiserslautern U, DE
I Loi and L Benini, DEIS – Bologna U, IT

1800 **ANALYTICAL HEAT TRANSFER MODEL FOR THERMAL THROUGH SILICON VIAS**
H Xu, V F Pavlidis and G De Micheli, EPF Lausanne, CH

1815 **A NEW ARCHITECTURE FOR POWER NETWORK IN 3D IC**
H-T Chen, H-L Lin, Z-C Wang and TT Hwang,
National Tsing-Hua U, Taiwan, ROC

IPs **IP2-5, IP2-12 AND IP2-13**

1830 **CLOSE**

4.7 Resource Management for QoS Guaranteed NoCs

Room – Les Bans **1700-1830**

Moderators:
A Hansson, Twente U, NL
F Petrot, TIMA Laboratory, FR

QoS and task mapping are key elements in NoC-based resource management, and this session discusses some of the major challenges regarding cost-efficient solutions to these problems. In this session the first paper proposes a software level approach for QoS-aware composability of applications mapping on NoCs. The second paper discusses the benefits of virtual point-to-point NoC links in mesh-based multi-core task mapping. The third paper presents the use of a central hardware unit to enable run-time virtual channel allocation for QoS in NoCs. Finally, the fourth paper in the session proposes an FPGA bridge to preserve QoS in NoC-based multi-FPGA designs.

1700 **ACHIEVING COMPOSABILITY IN NOC-BASED MPSOCS THROUGH QOS MANAGEMENT AT SOFTWARE LEVEL**
E A Carara and F G Moraes,
Pontifical Catholic U of Rio Grande Do Sul (PUCRS), BR
G Sassateli and G M Almeida, LIRMM, FR

1730 **SUPPORTING NON-CONTIGUOUS PROCESSOR ALLOCATION IN MESH-BASED CMPS USING VIRTUAL POINT-TO-POINT LINKS**
M Asadinia, A Tavakkol and H Sarbazi-Azad, TU Sharif, IR
M Modarressi, TU Sharif, IR and EPF Lausanne, CH

1800 **GUARANTEED SERVICE VIRTUAL CHANNEL ALLOCATION IN NOCS FOR RUN-TIME TASK SCHEDULING**
M Winter and G Fettweis, TU Dresden, DE

1815 **AN FPGA BRIDGE PRESERVING TRAFFIC QUALITY OF SERVICE FOR ON-CHIP NETWORK-BASED SYSTEMS**
A Beyranvand Nejad and M Escudero Martinez,
TU Delft, NL
K Goossens, TU Eindhoven, NL

1830 **CLOSE**

Smart Devices of the Future Special Day

WEDNESDAY 16 MARCH, 2011

0730 REGISTRATION and SPEAKERS' BREAKFAST

5.1 SMART DEVICES EMBEDDED TUTORIAL – Smart Devices for the Cloud Era

Room – Oisans **0830-1000**

Organisers/Moderators:
A Jerraya, CEA-LETI MINATEC, FR
J Goodacre, ARM, UK

Cloud computing will provide unlimited computing power and mobile terminals will take benefit of these new flexible computing platforms. This session presents the context of future mobile terminals, the key evolutions that will enable access to cloud computing and the new functions that will require cloud computing.

0830 **ENTERING THE PATH TOWARDS TERABIT/S WIRELESS LINKS**
G P Fettweis, F Guderian and S Krone, TU Dresden, DE

0900 **MOBILE CLOUD COMPUTING**
P Blouet, STEricsson, FR

0930 **IMAGE SENSORS: FROM EARLY VISIONS TO PERCEPTION FOR TOMORROW**
A Dupret, M Tchagaspanian, L Alacoque, A Peizerat and A Verdant, CEA-LETI MINATEC, FR

1000 **EXHIBITION BREAK/IP2**

5.2 An Encyclopedia of Routing

Room – Meije **0830-1000**

Moderators:
D Stroobandt, Ghent U, BE
I Markov, U of Michigan, US

This sessions covers such diverse topics in routing as Steiner-tree optimisation sensitive to electromigration, capacitive balancing of rotary clock networks, power-aware multi-Vdd routing, and PCB routing.

0830 **POWER-DRIVEN GLOBAL ROUTING FOR MULTI-SUPPLY VOLTAGE DOMAINS**
T-H Wu, A Davoodi and J Linderoth, Wisconsin – Madison U, US

0900 **OBSTACLE-AWARE MULTIPLE-SOURCE RECTILINEAR STEINER TREE WITH ELECTROMIGRATION AND IR-DROP AVOIDANCE**
J-T Yan and Z-W Chen,
Chung-Hua U, Hsinchu, Taiwan, ROC

0930 **STEINER TREE BASED ROTARY CLOCK ROUTING WITH BOUNDED SKEW AND CAPACITIVE LOAD BALANCING**
J Lu, V Honkote and B Taskin, Drexel U, US
X Chen, Pennsylvania U, US

0945 **ON ROUTING FIXED ESCAPED BOUNDARY PINS FOR HIGH SPEED BOARDS**
T-Y Tsai, GUC, Taiwan, ROC
R-J Lee, C-Y Chin, C-Y Kuan and H-M Chen,
NCTU, Taiwan, ROC
Y Kajitani, Kitakyushu U, JP

IP **IP2-6**

1000 **EXHIBITION BREAK/IP2**

5.3 Temperature and Variation Aware Design in Low Power Systems

Room – Belle-Etoile **0830-1000**

Moderators:
D Helms, OFFIS, DE
N Chang, Seoul National U, KR

This session introduces dynamic operating voltage for nanoscale SRAMs and temperature-dependent leakage minimisation for real-time systems followed by variability-aware dynamic power management for chip multiprocessors.

0830 **DYNAMIC WRITE LIMITED MINIMUM OPERATING VOLTAGE FOR NANOSCALE SRAMS**
S Nalam and B H Calhoun, Virginia U, US
V Chandra and R C Aitken, ARM, US

0900 **VARIABILITY AWARE DYNAMIC POWER MANAGEMENT FOR CHIP MULTIPROCESSOR ARCHITECTURES**
M Ghasemazar and M Pedram, U of Southern California, US

0930 **LEAKAGE AWARE ENERGY MINIMISATION FOR REAL-TIME SYSTEMS UNDER THE MAXIMUM TEMPERATURE CONSTRAINT**
H Huang and G Quan, Florida International U, US

1000 **EXHIBITION BREAK/IP2**

5.4 Advanced NoC Tooling and Architectures

Room – Stendhal **0830-1000**

Moderators:
A Jantsch, KTH, SE
S Yoo, Pohang U of Science and Technology, KR

In this session, we have three papers that address advanced tooling, architecture and run-time features for NoCs. In the first paper, the authors present a method to design NoCs with multiple design objectives, such as power consumption, latency and dynamic effects. In the second paper, the authors show an efficent implementation of the network, so that L1 accesses can be performed in a single clock cycle. In the last paper, the authors present a method to detect deadlocks in NoCs during the operation of the system. Together, the papers span the spectrum of tooling, implementation and dynamic effects in NoC design and operation.

0830 **MULTI-OBJECTIVE TABU SEARCH BASED TOPOLOGY GENERATION TECHNIQUE FOR APPLICATION-SPECIFIC NETWORK-ON-CHIP ARCHITECTURES**
A Tino and G N Khan, Ryerson U, CA

0900 **A FULLY-SYNTHESISABLE SINGLE-CYCLE INTERCONNECTION NETWORK FOR SHARED-L1 PROCESSOR CLUSTERS**
I Loi, M R Kakoee and L Benini, DEIS – Bologna U, IT
A Rahimi, UC San Diego, US

0930 (A) **RUN-TIME DEADLOCK DETECTION IN NETWORKS-ON-CHIP USING COUPLED TRANSITIVE CLOSURE NETWORKS**
R Al-Dujaily, T Mak, F Xia, A Yakovlev and M Palesi, Newcastle U, UK

IP **IP2-14**

1000 **EXHIBITION BREAK/IP2**

5.5 INDUSTRIAL 1

Room – Chartreuse **0830-1000**

Moderators:
E J Marinissen, IMEC, BE
W Nebel, OFFIS, DE

This session is dedicated to presentations in which industry points out to the community real-life design and technology challenges that should be addressed in the short-to-medium term. Further details about the topics presented in this session can be found in the 2-page industrial papers included in the conference proceedings.

0830 **DEVELOPING AN INTEGRATED VERIFICATION AND DEBUG METHODOLOGY**
A Matsuda and T Ishihara, Kyushu U, JP

0845 **AN ANALYTICAL COMPACT MODEL FOR ESTIMATION OF STRESS IN MULTIPLE THROUGH SILICON VIA CONFIGURATIONS**
G Eneman, D Milojevic, K De Meyer, A Mercha, E Beyne, T Hoffmann and G Van der Plas, IMEC, BE
J Cho, Samsung
V Moroz and M Choi, Synopsys

0900 **POWER MANAGEMENT VERIFICATION EXPERIENCES IN WIRELESS SoCs**
B Kapoor, Mimasic, US
A Hunter, ARM, US
P Tiwari, Synopsys, US

0915 **CHALLENGES IN DESIGNING HIGH SPEED MEMORY SUBSYSTEM FOR MOBILE APPLICATIONS**
T G Yip and P Yeung, Rambus Inc, US

0930 **SOLID STATE PHOTODETECTORS FOR NUCLEAR MEDICAL IMAGING APPLICATIONS**
M Mazzillo, P G Fallica, A Messina, M Romeo and R Zafalo, STMicroelectronics, IT
E Ficarra, DAUN - Politecnico di Torino, IT

0945 **FAULT GRADING OF SOFTWARE-BASED SELF-TEST PROCEDURES FOR DEPENDABLE AUTOMOTIVE APPLICATIONS**
O Ballan and G Fontana, STMicroelectronics, IT
P Bernardi, M Grosso and E Sanchez, Politecnico di Torino, IT

1000 **EXHIBITION BREAK/IP2**

5.6 Analysis, Compilation and Runtime Techniques

Room – Bayard **0830-1000**

Moderators:
H Falk, TU Dortmund, DE
H van Someren, ACE Associated Compiler Experts, NL

This session focuses on techniques to improve runtime behaviour. It comprises contributions on static data flow clustering, demand code paging, adaptive task migration and compilation of SyncCharts.

0830 **CARAT: CONTEXT-AWARE RUNTIME ADAPTIVE TASK MIGRATION FOR MULTI CORE ARCHITECTURES**
J Jahn, M A Al Faruque and J Henkel, Karlsruhe Institute of Technology, DE

0900 **A RULE-BASED STATIC DATAFLOW CLUSTERING ALGORITHM FOR EFFICIENT EMBEDDED SOFTWARE SYNTHESIS**
J Falk, C Zebelein, C Haubelt and J Teich, Erlangen-Nuremberg U, DE

0930 **DEMAND CODE PAGING FOR NAND FLASH IN MMU-LESS EMBEDDED SYSTEMS**
J Baiocchi and B R Childers, Pittsburgh U, US

IP IP2-7

1000 EXHIBITION BREAK/IP2

5.7 EMBEDDED TUTORIAL – Architectures for Online Error Detection and Recovery in Multicore Processors

Room – Les Bans 0830-1000

Organiser:
D Gizopoulos, Piraeus U, GR

Moderator:
X Vera, Intel Corporation, ES

This special session focuses on dependable multicore processor architectures and in particular solutions for online error detection, diagnosis, recovery, and repair during their operation in the field. The huge investment in the design and production of multicore processors may be put in risk due to incorrect system operation that can be caused by hard errors (due to manufacturing defects and aging/wearout), soft errors (due to environmental disturbances), and design bugs (due to pre-silicon verification inefficiencies). The speakers of the special session (from academia and industry) present effective architectural approaches that deal with all these sources of erroneous operation in the processor cores and the memories of a multicore architecture.

0830 **DESIGNING RESILIENT MULTICORE HARDWARE BY TREATING SOFTWARE ANOMALIES**
S Adve, U of Illinois at Urbana-Champaign, US

0900 **DYNAMIC VERIFICATION OF CORES AND MEMORY SYSTEMS**
D J Sorin, Duke U, US

0930 **HOW TO MANAGE ACCIDENTALLY HETEROGENEOUS CORES**
A Biswas, Intel Corporation, US

1000 **EXHIBITION BREAK/IP2**

IP2 Interactive Presentations

Room - Salle de Reception 1000-1030

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the morning. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP2-1 **AN ENERGY-EFFICIENT 3D CMP DESIGN WITH FINE-GRAINED VOLTAGE SCALING**
J Zhao, X Dong and Y Xie, Pennsylvania State U, US

IP2-2 **OPTIMISED MODEL CHECKING OF MULTIPLE PROPERTIES**
G Cabodi and S Nocco, Politecnico di Torino, IT

IP2-3 **A NEW DISTRIBUTED EVENT-DRIVEN GATE-LEVEL HDL SIMULATION BY ACCURATE PREDICTION**
D Kim and M Ciesielski, U of Massachusetts Amherst, US
S Yang, Pusan National U, KR

IP2-4 **CIRCUIT AND DFT TECHNIQUES FOR ROBUST AND LOW COST QUALIFICATION OF A MIXED-SIGNAL SOC WITH INTEGRATED POWER MANAGEMENT SYSTEM**
L Balasubramanian, P Sabbarwal, R K Mittal, P Narayanan, R K Dash, A D Kudari, S Manian, S Polarouthu, H Parthasarathy, R C Vijayaraghavanj and S Turkewadikar,
Texas Instruments (India) Private Limited, Bangalore, IN

IP2-5 **A 3D RECONFIGURABLE PLATFORM FOR 4G TELECOM APPLICATIONS**
W Lafi, D Lattard and A Jerraya, CEA-LETI, FR

IP2-6 **AN LOCV-BASED STATIC TIMING ANALYSIS CONSIDERING SPATIAL CORRELATIONS OF POWER SUPPLY VARIATIONS**
S Kobayashi and K Horiuchi,
Renesas Electronics Corporation, JP

IP2-7 **COMPILING SYNCCHARTS TO SYNCHRONOUS C**
C Traulsen, T Amende and R Von Hanxleden,
Christian-Albrechts U zu Kiel, DE

IP2-8 **OPTIMISATION OF STATEFUL HARDWARE ACCELERATION IN HYBRID ARCHITECTURES**
X Chang, K Wang and R Hou, IBM Research, PRC
Y Ma, Chinese Academy of Sciences, PRC
H Franke and H Yu, IBM Research, Watson, US
T Nelms, IBM SWG

IP2-9 **FORMAL RESET RECOVERY SLACK CALCULATION AT THE REGISTER TRANSFER LEVEL**
C-N Chung and S-Y Kuo, National Taiwan U, ROC
C-W Chang, National Central U, Jhongli, Taiwan, ROC
K-H Chang, Avery Design System Inc, US

IP2-10 **MULTI-GRANULARITY THERMAL EVALUATION OF 3D MPSoC ARCHITECTURES**
A Fourmigue, G Beltrame, G Nicolescu and E M Aboulhamid, Ecole Polytechnique Montreal, CA
I O'Connor, Ecole Centrale Lyon, FR

IP2-11 **TWO METHODS FOR 24 GBPS TEST SIGNAL SYNTHESIS**
D C Keezer and C E Gray,
Georgia Institute of Technology, US

IP2-12 **3D-ICML: A 3D BIPOLAR RERAM DESIGN WITH INTERLEAVED COMPLEMENTARY MEMORY LAYERS**
Y-C Chen and H Li, Polytechnic Institute of NYU, US
Y Chen, Pittsburgh U, US
R Pino, AFRL, US

IP2-13 **ARCHITECTURAL EXPLORATION OF 3D FPGAS TOWARDS A BETTER BALANCE BETWEEN AREA AND DELAY**
C-I Chen, B-C Lee and J-D Huang,
National Chiao Tung U, ROC

IP2-14 **NoC-MPU: A SECURE ARCHITECTURE FOR FLEXIBLE CO-HOSTING ON SHARED MEMORY MPSoCs**
J Porquet and A Grenier, UPMC, F
C Schwarz, Nagravision, CH

6.1.1 SMART DEVICES HOT TOPIC/EMBEDDED TUTORIAL – Ultra Low Power Smart Devices

Room – Oisans 1100-1230

Organisers/Moderators:
J Goodacre, ARM, UK
A Jerraya, CEA-LETI MINATEC, FR

Low power is considered the key enabling technology for future smart systems. For most applications stringent requirements on power consumption has to be satisfied. This session presents power issues in different application domains and how specific requirements are addressed. This is illustrated with hardware/software design techniques for concrete products.

1100 **LOW POWER SMART INDUSTRIAL CONTROL AND INSTRUMENTATION**
M A Bilgic and M Gerding, KHRONE Messtechnik GmbH, DE

1130 **ULTRA LOW POWER PROCESSOR ARCHITECTURES FOR SMART MICROCONTROLLERS**
S Sadasivan, ARM, UK

1200 **LOW POWER INTERCONNECTS FOR SIMD COMPUTERS**
M Who, S Satpathy, R Dreslinsky, D Blaauw and T Mudge, U of Michigan, US

1230 **LUNCH BREAK**

6.2 Placement and Floorplanning

Room – Meije 1100-1230

Organisers/Moderators:
R Otten, TU Eindhoven, NL
A Davoodi, Wisconsin U, US

The first paper develops a network-flow based algorithm for large-scale placement with region constraints. Subsequent papers propose techniques for I/O buffer placement, temperature-driven whitespace allocation in floorplanning, as well as physical planning for on-chip networks.

1100 **FLOW-BASED PARTITIONING AND POSITION CONSTRAINTS IN VLSI PLACEMENT**
M Struzyna, Bonn U, DE

1130 **INTEGRATED CIRCUIT WHITE SPACE REDISTRIBUTION FOR TEMPERATURE OPTIMISATION**
Y Chen and H Zhou, Northwestern U, US
R P Dick, U of Michigan, US

1200 **TIMING-CONSTRAINED I/O BUFFER PLACEMENT FOR FLIP-CHIP DESIGNS**
Z-W Chen and J-T Yan, Chung-Hua U, Taiwan, ROC

1215 **FLOORPLANNING EXPLORATION AND PERFORMANCE EVALUATION OF A NEW NETWORK-ON-CHIP**
L Xue and W Ji, Beijing Institute of Technology, PRC
H-U-R Khan, Pakistan Institute of Engineering and Applied Sciences, Islamabad, PK

IP **IP3-1**

1230 **LUNCH BREAK**

6.3 Power Modelling, Analysis and Optimisation

Room – Belle-Etoile **1100-1230**

Moderators:
J Henkel, Karlsruhe Institute of Technology, DE
M Poncino, Politecnico di Torino, IT

This session presents five papers dealing with various aspects of power modelling, analysis, and optimisation. The topics include thermal analysis and leakage modelling, optimised clock gating structures, low-power design of multimedia building blocks, and energy-efficient cache architectures.

1100 **WORST-CASE TEMPERATURE ANALYSIS FOR REAL-TIME SYSTEMS**
D Rai, H Yang, I Bacivarov and L Thiele ETH Zurich, CH
J-J Chen, KIT, DE

1130 **BLACK-BOX LEAKAGE POWER MODELING FOR CELL LIBRARY AND SRAM COMPILER**
C-K Tseng, C-C Weng and S-Y Huang
National Tsing Hua U, Taiwan, ROC
S-C Fang, Tinnotek Inc, Taiwan, ROC
J-J Chen, Industrial Technology Research Institute (ITRI), Taiwan, ROC

1145 **CLOCK GATING OPTIMISATION WITH DELAY-MATCHING**
S-J Hsu and R-B Lin, Yuan Ze U, Taiwan, ROC

1200 **A LOW COMPLEXITY STOPPING CRITERION FOR REDUCING POWER CONSUMPTION IN TURBO DECODERS**
P Reddy, CEA-LETI and Telecom Bretagne, FR
F Clermidy, CEA-LETI, FR
A Baghdadi and M Jezequel, Telecom Bretagne, FR

1215 **A NOVEL TAG ACCESS SCHEME FOR LOW POWER L2 CACHE**
H Park, S Yoo and S Lee, POSTECH, KR
Y Cho, Samsung Electronics, KR

IPs **IP3-2 AND IP3-7**

1230 **LUNCH BREAK**

6.4 Design and Test of Fault Resilient NoC Architectures

Room – Stendhal **1100-1230**

Moderators:
M Coppola, ST Microelectronics, FR
K Goossens, TU Eindhoven, NL

Due to their role of distributed backbone of Systems-on-Chip, NoCs must be capable of tolerating faults and carrying fault notifications of other components in the system. The first paper in this session describes an efficient methodology to diagnose faults in the NoC via BIST techniques. The second leverages physical channel redundancy to tolerate runtime NoC failures while still enabling QoS support. The third paper deals with fault-tolerant application mapping onto a NoC-based platform, with the goal of optimising performance and interconnect power consumption.

1100 **EXPLOITING NETWORK-ON-CHIP STRUCTURAL REDUNDANCY FOR A COOPERATIVE AND SCALABLE BUILT-IN-SELF-TEST ARCHITECTURE**
A Strano, M Favalli and D Bertozzi, ENDIF – Ferrara U, IT
C Gomez and M E Gomez, UP de Valencia, ES
D Ludovici, TU Delft, NL

1130 **A RELIABLE NETWORK FOR PRIORITY-BASED ON-CHIP COMMUNICATION**
M R Kakoee and L Benini, Bologna U, IT
V Bertacco, U of Michigan, Ann Arbor, US

1200 **FARM: FAULT-AWARE RESOURCE MANAGEMENT FOR NOC-BASED MULTIPROCESSOR PLATFORMS**
C-L Chou and R Marculescu, Carnegie Mellon U, US

IP **IP3-12**

1230 **LUNCH BREAK**

6.5 New Techniques for Diagnosis and Debug

Room – Chartreuse **1100-1230**

Moderators:
S Reddy, Iowa U, US
B Vermeulen, NXP Semiconductors, NL

This session covers advances in diagnosis and debug, ranging from diagnosis using compressed responses, to capturing traced data during circuit execution, and concluding with a technique that ensures valid state dumps in the presence of clock domain crossings.

1100 **ON DIAGNOSIS OF MULTIPLE FAULTS USING COMPRESSED RESPONSES**
J Ye, Y Hu and X Li, Chinese Academy of Sciences, PRC

1130 **ON MULTIPLEXED SIGNAL TRACING FOR POST-SILICON DEBUG**
X Liu and Q Xu, The Chinese U of Hong Kong, HK

1200 **ELIMINATING DATA INVALIDATION IN DEBUGGING MULTIPLE-CLOCK CHIPS**
J Gao, Y Han and X Li, Chinese Academy of Sciences, PRC

1230 **LUNCH BREAK**

6.6 Embedded Software for Parallel Architectures

Room – Bayard **1100-1230**

Moderators:
O Bringmann, FZI Karlsruhe, DE
F Slomka, Ulm U, DE

This session presents automation approaches for programming parallel architectures. Two papers deal with software parallelisation applied to nested loop programs and to matrix operations using OpenCL. The third paper evaluates the implementation of HPC benchmarks on a GPU.

1100 **PARALLELISATION OF WHILE LOOPS IN NESTED LOOP PROGRAMS FOR SHARED-MEMORY MULTIPROCESSOR SYSTEMS**
S J Geuns, T Bijlsma and H Corporaal, TU Eindhoven, NL
M J G Bekooij, NXP Semiconductors, NL

1130 **GEMMA IN APRIL: A MATRIX-LIKE PARALLEL PROGRAMMING ARCHITECTURE ON OPENCL**
T Wu, D Wu, Y Wang, X Zhang, H Luo, N Xu, Tsinghua U, Tsinghua U, PRC

1100 **EVALUATING THE POTENTIAL OF GRAPHICS PROCESSORS FOR HIGH PERFORMANCE EMBEDDED COMPUTING**
Si Mu, C Wang, M Liu, D Li, M Zhu, X Xie and Y Deng, Tsinghua U, PRC
X Chen, Chinese Academy of Sciences, PRC

IPs **IP3-3 and IP3-8**

1230 **LUNCH BREAK**

6.7 HOT TOPIC – Virtual Manycore Platforms: Moving Towards 100+ Processor Cores

Room – Les Bans **1100-1230**

Organisers:
R Leupers, RWTH Aachen U, DE
G Martin, Tensilica, US

Moderator:
F Ghenassia, STMicroelectronics, FR

The evolution to manycore platforms is real, both in the High-Performance Computing domain and in embedded systems. If we start with ten or more cores, we can see the evolution to many tens of cores and to platforms with 100 or more occurring in the next few years.

These platforms are heterogeneous, homogeneous, or a mixture of subsystems of both types, both relatively generic and quite application-specific. They are applied to many different application areas. When we consider the design, verification, software development and debugging requirements for applications on these platforms, the need for virtual platform technologies for manycore systems grows quickly as the systems evolve. As we move to manycore, the key issue is simulation speed, and trying to keep pace with the target complexity using host-based simulation is a major challenge. New Instruction Set Simulation technologies, such as compiled, JIT, DBT, sampling, abstract, hybrid and parallel have all emerged in the last few years to match the growth in complexity and requirements. At the same time, we have seen consolidation in the virtual platform industrial sector, leading to some concerns about whether the market can support the required continued development of innovations to give the needed performance. This special session will deal with manycore virtual platforms from several different perspectives, highlighting new research approaches for high speed simulation, tool and IP marketing opportunities, as well as real life virtual platform needs of industrial end users.

1100 **HYBRID PROCESSOR SIMULATION FOR VIRTUAL PLATFORMS**
R Leupers, RWTH Aachen U, DE

1115 **THE VIRTUAL DESIGN REQUIREMENTS OF CONFIGURABLE MANYCORE BASEBAND PLATFORMS**
G Martin, Tensilica, US

1130 **ULTRA-FAST PARALLEL SIMULATION IN THE MANY-CORE ERA**
N Topham, Edinburgh U, UK

1145 **TOWARDS SCALABLE AND ACCURATE ARCHITECTURAL SIMULATION OF 100+ CORE SYSTEMS**
L Eeckhout, Ghent U, BE

1200 **ENABLING PRODUCTIVE MANYCORE SOFTWARE DEVELOPMENT USING VIRTUAL PROTOTYPES**
F Schirrmeister, Synopsys, US

1215 **A GENERIC MANYCORE SOC VIRTUAL PLATFORM**
S Chen, Huawei Technologies, US

1230 **LUNCH BREAK**

6.8 PANEL SESSION – Embedded Software Debug and Test

Room – Exhibition Theatre **1100-1230**

Organiser/Moderator:
M Winterholer, Cadence, DE

Panellists:
F Cerisier, EASii-IC, FR
S Davidmann, Imperas, UK
L Ducuosso, STMicroelectronics, FR
J Engblom, Simics Wind River, SE
A Mayer, Infineon, DE

Today's complexity of embedded software is steadily increasing. The growing number of processors in a system and the increased communication and synchronisation of all components requires scalable debug and test methods for each component as well as the system as a whole. Considering today's cost and time to market sensitivity it is important to find and debug errors as early as possible and to increase the degree of test and debug automation to avoid quality losses. These challenges are not only requiring new tools and methodologies but also organisational changes since hardware and software developer have to work closer together to achieve the necessary productivity and quality gain. The panel will discuss new strategies in hardware and software development to make embedded software more reliable and easy to debug.

1230 **LUNCH BREAK**

6.1.2 SPECIAL DAY KEYNOTE AND AWARDS

Room – Oisans - 1340-1400 Awards and 1400-1430 Keynote

1340 **Awards Moderator: Z Peng,** Linkoping U, SE

Awards: Presentation of the DATE 10 Best Paper Awards

TRACK D - PROPERTIES OF AND IMPROVEMENTS TO TIME-DOMAIN DYNAMIC THERMAL ANALYSIS ALGORITHMS
X Chen and R P Dick, U of Michigan, US
L Shang, U of Colorado at Boulder, US

TRACK E - SKEWED PIPELINING FOR PARALLEL SIMULINK SIMULATIONS
A Canedo, T Yoshizawa and H Komatsu, IBM Research, JP

BEST IP - TOWARDS A CHIP LEVEL RELIABILITY SIMULATOR FOR COPPER/LOW-K BACKEND PROCESSES
M Bashir and L Milor, Georgia Institute of Technology, US

Presentation of the EDAA Outstanding Dissertation Awards

1400

Organiser/Moderator:
A Jerraya, CEA-LETI MINATEC, FR

Keynote Speaker:
Hannu Kauppinen, Director, Head of Radio Systems Laboratory, Nokia Research Center, FI

WIRELESS INNOVATIONS FOR SMARTPHONES

Abstract: The ever increasing demand for fast mobile internet connectivity continues to set challenges for research in radio communications. On one hand the capacity demand can be served by offloading data traffic to local networks. On the other hand using more bandwidth, and possibly dynamically allocating spectrum in a flexible way, will improve the usage of the available spectrum. The future of wireless access continues to be defined by the 3GPP and IEEE standards setting bodies. Radios can also provide innovative features that offer new functionalities for consumers, such as ultra fast local connectivity, sensing and positioning.

This talk will present examples of various radio innovations and the challenges related to commercialising them.

1430 **END OF SESSION**

7.1 SMART DEVICES HOT TOPIC – Smart Medical Implants

Room – Oisans **1430-1600**

Organisers:
A Jerraya, CEA-LETI MINATEC, FR
J Goodacre, ARM, UK

Moderator:
S Yoo, POSTECH, KR

Medical implants integrate a large number of heterogeneous components (computing, sensors, actuators, antenna, RF) to implement sophisticated functions. Unlike classic devices, the design of medical implants includes the building of application specific architecture and specific interfaces and other kinds of packaging required to efficiently interface with human body. This session introduces the key technologies for the design of such complex devices.

1430 **POWERING AND COMMUNICATING WITH MM-SIZE IMPLANTS**
J Rabaey, M Mark, D Chen, C Sutardja, C Tang, S Gowda, M Wagner and D Werthimer, UC Berkeley, US

1500 **HETEROGENEOUS INTEGRATION FOR SMART SYSTEM DESIGN**
P Ancey, STMicroelectronics, FR

1530 **AN ANTENNA-FILTER CO-DESIGN FOR CARDIAC IMPLANTS**
E de Foucauld, J-B David and C Delaveaud, CEA-LETI, FR

1600 **BREAK/IP3**

7.2 Emerging Memory Technologies

Room – Meije **1430-1600**

Moderators:
H Li, New York U, US
Y Chen, Pittsburgh U, US

This session includes three papers on emerging memory technologies. The first paper discusses design issues on memristor-based RRAM; the second paper presents SRAM design using emerging tunnelling transistors; the last paper presents a novel scratch pad memory architecture using PCRAM.

1430 **DESIGN IMPLICATIONS OF MEMRISTOR-BASED RRAM CROSS-POINT STRUCTURES**
C Xu, X Dong and Y Xie, Pennsylvania State U, US
N P Jouppi, Hewlett-Packard Labs, US

1500 **ROBUST 6T SI TUNNELING TRANSISTOR SRAM DESIGN**
Xi Yang and K Mohanram, Rice University, US

1530 **TOWARDS ENERGY EFFICIENT HYBRID ON-CHIP SCRATCH PAD MEMORY WITH NON-VOLATILE MEMORY**
J Hu and W-C Tseng, U of Texas at Dallas, US
C J Xue, City U of Hong Kong, PRC
Q Zhuge, Jiangnan U, PRC
E H-M. Sha, U of Texas at Dallas, US and Hunan U, PRC

1600 **BREAK/IP3**

7.3 Architectural Optimisation for Low Power Systems

Room – Belle-Etoile **1430-1600**

Moderators:
A Nannarelli, TU Denmark, DK
W Nebel, Oldenburg U and OFFIS, DE

In this session new contributions are presented for optimisation of lower power system at architectural level ranging from clock gating techniques for FPGAs, trading off quality vs. energy for DSP applications, and finally, optimising switched capacitor DC/DC converters.

1430 **A NEW RECONFIGURABLE CLOCK-GATING TECHNIQUE FOR LOW POWER SRAM-BASED FPGAS**
L Sterpone, Politecnico di Torino, IT
D Matos and L Carro, UFRGS, BR
S Wong and F Anjam, TU Delft, NL

1500 **CONTROLLED TIMING-ERROR ACEPTANCE FOR LOW ENERGY IDCT DESIGN**
K He, A Gerstlauer and M Orshansky,
U of Texas at Austin, US

1530 **ENERGY PARSIMONIOUS CIRCUIT DESIGN THROUGH PROBABILISTIC PRUNING**
A Lingamneni and K Palem, Rice U and NTU-Rice Inst of Sustainable and Applied Infodynamics (ISAID), US
C Enz, J-L Nagel and C Piguet, CSEM, CH

1545 **STAGE NUMBER OPTIMISATION FOR SWITCHED CAPACITOR POWER CONVERTERS IN MICRO-SCALE ENERGY HARVESTING**
C Lu, S P Park, V Raghunathan and K Roy, Purdue U, US

IP **IP3-4**

1600 **BREAK/IP3**

7.4 Advanced Technologies for NoC Implementation

Room - Stendhal **1430-1600**

Moderators:
D Bertozzi, Ferrara U, IT
P Vivet, CEA-LETI, FR

Constraints of nanoscale manufacturing are pushing the development of new technologies for NoC implementation. The scope of this session ranges from asynchronous links to optical interconnects for chip networking. The first paper is about new fault tolerant mechanisms for NoC asynchronous links. The second paper presents a tool for optical NoC specification, while the last one improves upon optical ring architectures.

1430 **INTERCONNECT-FAULT-RESILIENT DELAY-INSENSITIVE ASYNCHRONOUS COMMUNICATION LINK BASED ON CURRENT-FLOW MONITORING**
N Onizawa, A Matsumoto and T Hanyu, Tohoku U, JP

1500 **VANDAL: A TOOL FOR THE DESIGN SPECIFICATION OF NANOPHOTONIC NETWORKS**
G Hendry, J Chan, L Carloni and K Bergman, Columbia U, US

1530 **OPTICAL RING NETWORK-ON-CHIP (ORNOC). ARCHITECTURE AND DESIGN METHODOLOGY**
S Le Beux, Ecole Polytechnique de Montreal, CA and Ecole Centrale de Lyon, FR
J Trajkovic, G Nicolescu and G Bois, Ecole Polytechnique de Montreal, CA
P Paulin, STMicroelectronics, CA
I O'Connor, Ecole Centrale de Lyon, FR

1600 **BREAK/IP3**

7.5 Emerging Test Solutions for Advanced Technologies, RF and MEMS Devices

Room – Chartreuse **1430-1600**

Moderators:
S Khursheed, Southampton U, UK
J Machado da Silva, INESC Porto, PT

Papers in this session address test challenges in RF, MEMS and advanced technology nodes. The proposed solutions address either to reduce conventional specification tests or show how to improve limit setting for parametric tests. One paper covers test structures which identify lithographic deviations.

1430 **MULTIDIMENSIONAL PARAMETRIC TEST SET OPTIMISATION OF WAFER PROBE DATA FOR PREDICTING IN FIELD FAILURES AND SETTING TIGHTER TEST LIMITS**
D Drmanac, N Sumikawa and L-C Wang, UC Santa Barbara, US
L Winemberg and M S Abadir, Freescale Semiconductor Inc, US

1500 **ON DESIGN OF TEST STRUCTURES FOR LITHOGRAPHIC PROCESS CORNER IDENTIFICATION**
A Sreedhar and S Kundu, U of Massachusetts at Amherst, US

1515 **AN ELECTRICAL TEST METHOD FOR MEMS CONVECTIVE ACCELEROMETERS: DEVELOPMENT AND EVALUATION**
A A Rekik, LIRMM, FR and Sfax U, TN
F Azais, N Dumas, F Mailly and P Nouet, LIRMM, FR

1545 **CORRELATING INLINE DATA WITH MODULE FINAL TEST OUTCOMES IN ANALOG/RF DEVICES**
N Kupp and Y Makris, Yale U, US
M Slamani, IBM, US

IPs **IP3-5 AND IP3-9**

1600 **BREAK/IP3**

7.6 Innovative Power-Aware Systems for a Green and Healthy Society

Room – Bayard **1430-1600**

Moderators:
W Eberle, IMEC, BE
E Popovici, National U of Ireland, IE

A green and healthy society demands innovative systems relying on a joint effort from the technology, the signal processing and energy management point of view. Healthcare applications address brain computer interfacing, ECG monitoring and digital hearing aids based on bioelectronics interfaces, wearable and implantable systems. Optimised circuits that collect energy from the environment and power management controllers are presented for integrated, wearable and embedded systems.

1430 **SYSTEMATIC DESIGN OF A PROGRAMMABLE LOW-NOISE CMOS NEURAL INTERFACE FOR CELL ACTIVITY RECORDING**
C M Lopez, S Musa, C Bartic and W Eberle, IMEC, BE
R Puers and G Gielen, KU Leuven, BE

1500 **A REAL-TIME COMPRESSED SENSING-BASED PERSONAL ELECTROCARDIOGRAM MONITORING SYSTEM**
K Kanoun, H Mamaghanian, N Khaled and D Atienza, EPF Lausanne, CH

1515 **A DISTRIBUTED AND SELF-CALIBRATING MODEL-PREDICTIVE CONTROLLER FOR ENERGY AND THERMAL MANAGEMENT OF HIGH-PERFORMANCE MULTICORES**
A Bartolini, M Cacciari, A Tilli and L Benini, DEIS – Bologna U, IT

1545 **AN EFFECTIVE MULTI-SOURCE ENERGY HARVESTER FOR LOW POWER APPLICATIONS**
D Carli, En-DIF - Ferrara U, IT
D Brunelli, DISI – Trento U, IT
L Benini, DEIS – Bologna U, IT
M Ruggeri, IMAMOTER, National Research Council, IT

IPs **IP3-6, IP3-10 AND IP3-11**

1600 **BREAK/IP3**

7.7 HOT TOPIC – Foundations of Component-Based Design for Embedded Systems

Room – Les Bans **1430-1600**

Moderators:
A Sangiovanni-Vincentelli, UC Berkeley, US and Trento U, IT
J Sifakis, VERIMAG, FR

Component-based validation techniques for parallel and distributed embedded systems should be able to deal with heterogeneous components, interactions, and specification mechanisms. This special session describes a unified composition paradigm that allows the composition of subsystems with different execution and interaction semantics, combining computational and analytic models. This paradigm focuses on constructivity, which is reasoning about global system properties based on properties of its individual components.

1430 **COMPOSING HETEROGENEOUS COMPONENTS FOR SYSTEM-WISE PERFORMANCE ANALYSIS**
L Thiele, ETH Zurich, CH

1500 **FORMAL METHODS FOR COMPOSING COMPONENTS**
T Henzinger,
Institute of Science and Technology, Vienna, AT

1500 **REQUIREMENT ENGINEERING FOR COMPOSITION**
A Benveniste, INRIA, FR

1600 **BREAK/IP3**

7.8 EMBEDDED TUTORIAL – Predictable System Integration

Room – Exhibition Theatre **1430-1600**

Organiser/Moderator:
W Kruijtzer, Synopsys, NL

Starting from the application side, we present system functions and their implementations on CPUs and function-specific hardware using concrete examples from the video processing domain. This includes quantitative data on bandwidth and latency requirements and an overview of challenges developers face if the SoC infrastructure lacks basic provisions for Quality-of-Service. We then present how these challenges can be addressed by a combination of architectural principles and associated analysis techniques, based on network calculus. Finally we show how these techniques can be applied in building real-life SoCs. Key benefits of the presented techniques are predictable performance and improved time-to-market, while avoiding costly over-dimensioning to guarantee real-time behaviour.

1430 **BUILDING REAL TIME HDTV APPLICATIONS IN FPGAS USING PROCESSORS, AXI INTERFACES AND HIGH LEVEL SYNTHESIS TOOLS**
S Neuendorffer, J Noguera and K Vissers, Xilinx, US

1500 **ARCHITECTURES AND MODELLING OF PREDICTABLE MEMORY CONTROLLERS FOR IMPROVED SYSTEM INTEGRATION**
B Akesson and K Goossens, TU Eindhoven, NL

1530 **SOC INFRASTRUCTURES FOR PREDICTABLE SYSTEM INTEGRATION**
P van der Wolf and J Geuzebroek, Synopsys, NL

1600 **BREAK/IP3**

IP3 Interactive Presentations

Room - Salle de Reception 1600-1630

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP3-1 **EARLY CHIP PLANNING COCKPIT**
J Shin, J A Darringer, G Luo, A J Weger and C L Johnson, IBM Research, US

IP3-2 **POWER REDUCTION VIA NEAR-OPTIMAL LIBRARY-BASED CELL-SIZE SELECTION**
M Rahman, H Tennakoon and C Sechen, U of Texas at Dallas, US

IP3-3 **SCALABLE PACKET CLASSIFICATION VIA GPU METAPROGRAMMING**
K Kang and Y S Deng, Tsinghua U, PRC

IP3-4 **BATTERY-SUPERCAPACITOR HYBRID SYSTEM FOR HIGH-RATE PULSED LOAD APPLICATIONS**
D Shin, Y Kim, J Seo and N Chang, Seoul National U, KR
Y Wang and M Pedram, U of Southern California, US

IP3-5 **FEEDBACK BASED DROOP MITIGATION**
S Pontarelli, M Ottavi and A Salsano, Rome U, IT
K Zarrineh, Advanced Micro Devices Boxborough, US

IP3-6 **A 0.964MW DIGITAL HEARING AID SYSTEM**
P Qiao and H Corporaal, TU Eindhoven, NL
M Lindwer, Silicon Hive B.V., NL

IP3-7 **HYPOENERGY: HYBRID SUPERCAPACITOR-BATTERY POWER-SUPPLY OPTIMIZATION FOR ENERGY EFFICIENCY**
A Mirhoseini and F Koushanfar, Rice U, US

IP3-8 **FINE-GRAIN OPENMP RUNTIME SUPPORT WITH EXPLICIT COMMUNICATION HARDWARE PRIMITIVES**
P Tendulkar, V Papaefstathiou, G Nikiforos, S Kavadias and D Nikolopoulos, FORTH-ICS, GR

IP3-9 **TRANSITION-TIME-RELATION BASED CAPTURE-SAFETY CHECKING FOR AT-SPEED SCAN TEST GENERATION**
K Miyase, X Wen and S Kajihara, Kyushu Institute of Technology, JP
M Aso and Furukawa, Renesas Micro Systems Co Ltd, JP
Y Yamato, The Fukuoka Industry, Science and Technology Foundation, JP

IP3-10 **2D AND 3D INTEGRATION WITH ORGANIC AND SILICON ELECTRONICS**
C K Landrock, B Omrane, B Kaminska, Y Chuo and J Aristizabal, Simon Fraser U, CA

IP3-11 **ULTRA LOW-POWER PHOTOVOLTAIC MPPT TECHNIQUE FOR INDOOR AND OUTDOOR WIRELESS SENSOR NODES**
A S Weddell, G V Merrett and B M Al-Hashimi, Southampton U, UK

IP3-12 **A FAULT-TOLERANT DEADLOCK-FREE ADAPTIVE ROUTING FOR ON CHIP INTERCONNECTS**
F Chaix, N E Zergainoh and M Nicolaidis, TIMA Laboratory, FR
D R Avresky, IRIANC, FR

8.1 SMART DEVICES PANEL SESSION – Integrating the Real World Interfaces

Room – Oisans **1700-1830**

Organisers/Moderators:
A Jerraya, CEA-LETI MINATEC, FR
J Goodacre, ARM, UK

Panellists:
P Urard, STMicroelectronics, FR
J Rabaey, UC Berkeley, US
R Bramley, STEricsson, FR
A King-Smith, IMGTEC, UK
W Burleson, Massachusetts U, US
F Perruchot, CEA-LETI, FR

Smart systems require interfacing more of the world in an integrated solution (Camera, gyroscope, compass, temp, direction…). This is imposed by social evolution and enabled by new integration technologies. So far, many products featuring a variety of hardware and software have been developed and many more seems to be coming in a fast growing market. The panel will present the most promising products and solutions and discuss the innovations enabling future smart systems.

1830 **CLOSE**

8.2 System-Level Design Techniques for Automotive Systems

Room – Meije **1700-1830**

Moderators:
J Teich, Erlangen-Nuremberg U, DE
L Lavagno, Politecnico di Torino, IT

This session is on different aspects of system and software design for automotive platforms. The first paper describes techniques for control software design for architectures with hybrid communication protocols like FlexRay. The second paper is on accurate worst-case execution time analysis of software with an emphasis on the automotive domain. Finally, the third paper is on schedule synthesis for a switched FlexRay bus.

1700 **RE-ENGINEERING CYBER-PHYSICAL CONTROL APPLICATIONS FOR HYBRID COMMUNICATION PROTOCOLS**
D Goswami, R Schneider and S Chakraborty, TU Munich, DE

1730 **PRECISE WCET CALCULATION IN HIGHLY VARIANT REAL-TIME SYSTEMS**
P Montag, Daimler AG, DE
S Altmeyer, Saarland U, DE

1800 **OPTIMAL SCHEDULING OF SWITCHED FLEXRAY NETWORKS**
T Schenkelaars and K Goossens, TU Eindhoven, NL
B Vermeulen, NXP Semiconductors, NL

1830 **CLOSE**

8.3 Power/Error Tradeoffs

Room – Belle-Etoile **1700-1830**

Moderators:
L Bai, U of Michigan, US
J Chen, Karlsruhe Institute of Technology, DE

This session features four papers addressing the interaction of power consumption and error-related metrics. The first two papers discuss how power optimisation can be actually leveraged to reduce errors due to device aging in circuits and memory structures. The other two papers deal with the issue of how power can be saved by tolerating errors in the computation.

1700 **ON THE EFFICACY OF NBTI MITIGATION TECHNIQUES**
T-B Chan and P Gupta, UCLA, US
J M Sartori and R Kumar, U of Illinois at Urbana-Champaign, US

1730 **PARTITIONED CACHE ARCHITECTURES FOR REDUCED NBTI-INDUCED AGING**
M Loghi, Udine U, IT
A Calimera and M Poncino, Politecnico di Torino, IT

1800 **ADAPTIVE VOLTAGE OVER-SCALING FOR RESILIENT APPLICATIONS**
P-K Krause, Frankfurt U, DE
I Polian, Passau U, DE

1815 **DESIGN OF VOLTAGE-SCALABLE META FUNCTIONS FOR APPROXIMATE COMPUTING**
D Mohapatra,V K Chippa, K Roy and A Raghunathan, Purdue U, US

IPs **IP4-1, IP4-9 AND IP4-14**

1830 **CLOSE**

8.4 Memory System Architectures

Room – Stendhal **1700-1830**

Moderators:
T Austin, U of Michigan, US
G Gaydadjiev, TU Delft, NL

This session features six papers focused on the design of efficient and robust memory systems. The techniques to be presented include novel heterogeneous memory architectures, scratchpad memory optimisations, and support for vectorised loops. In addition, detailed system analysis is utilised to improve the design of MPSoC transactional memory and wear-prone storage.

1700 (A) **MLP AWARE HETEROGENEOUS MEMORY SYSTEM**
S Phadke and S Narayanasamy, U of Michigan, US

1730 **IMPACT OF PROCESS VARIATION ON ENDURANCE ALGORITHMS FOR WEAR-PRONE MEMORIES**
A Peixoto Ferreira, S Bock, B Childers, R Melhem and D Mosse, Pittsburgh U, US

1800 **FLEXMEMORY: EXPLOITING AND MANAGING ABUNDANT OFF-CHIP OPTICAL BANDWIDTH**
Y Wang, L Zhang, Y Han, H Li and X Li, Chinese Academy of Science, PRC

1815 **SCRATCHPAD MEMORY OPTIMISATIONS FOR DIGITAL SIGNAL PROCESSING APPLICATIONS**
S Z Gilani and N S Kim, U of Wisconsin-Madison, US
M Schulte, Advanced Micro Devices

IPs **IP4-2 AND IP4-10**

1830 **CLOSE**

8.5 Testing and Designing SRAM Memories

Room – Chartreuse 1700-1830

Moderators:
S Nassif, IBM, US
X Wen, Kyushu Institute of Technology, JP

Papers in this session describe the challenges of testing and designing SRAM memories in advanced technology nodes. Topics covered are improved robustness, models for gate-oxide shorts and how to counteract BTI reliability issues

1700 **ROBUSTNESS ANALYSIS OF A 6T SRAM IN MEMORY RETENTION MODE UNDER PVT VARIATION**
E I Vatajelu and J Figueras, UP Catalunya, ES

1730 **OPTIMISATION OF EMBEDDED 8T SRAMS USING WORD-LINE VOLTAGE MODULATION**
B Alorda, G Torrens, S Bota and J Segura, Illes Balears U, ES

1800 **PROACTIVE RECOVERY FOR BTI IN HIGH-K SRAM CELLS**
L Li, Y Zhang and J Yang, Pittsburgh U, US

IP **IP4-3**

1830 **CLOSE**

8.6 Cryptoanalysis, Attacks and Countermeasures

Room – Bayard 1700-1830

Moderators:
K Sakiyama, U of Electro-Communications, Tokyo, JP
L Torres, LIRMM, FR

The focus of this session is on the threats and the protection of the implementation of cryptographic algorithms. The presentations cover a cryptanalytic attack on FPGA clusters, electromagnetic attacks, insertion of hardware trojans and fault attack countermeasures for elliptic curve cryptosystems.

1700 **THE POTENTIAL OF RECONFIGURABLE TECHNOLOGIES FOR HPC CRYPTANALYTIC APPLICATIONS**
A Cilardo, U of Naples Federico II, IT

1730 **ENHANCEMENT OF SIMPLE ELECTRO-MAGNETIC ATTACKS BY PRE-CHARACTERISATION IN FREQUENCY DOMAIN AND DEMODULATION TECHNIQUES**
O Meynard,
Institut TELECOM, TELECOM ParisTech and DGA/MI, FR
D Real, DGA/MI, FR
S Guilley and J-L Danger,
Institut TELECOM, TELECOM ParisTech, FR
N Homma, Tohoku U, JP

1800 **LOEDAR: A LOW COST ERROR DETECTION AND RECOVERY SCHEME FOR ECC**
K Ma and K Wu, U of Illinois at Chicago, US

1815 **LIGHTWEIGHT COUNTERMEASURE AGAINST FAULT ATTACKS ON ELLIPTIC CURVE CRYPTOGRAPHY**
D Karaklajic, J Fan and I Verbauwhede, KU Leuven, BE
J-M Schmidt, TU Graz, AT

IP **IP4-4**

1830 **CLOSE**

8.7 HOT TOPIC – Flows, Application and Future of Component-based Design for Embedded Systems

Room – Les Bans **1700-1830**

Organisers:
A Sangiovanni-Vincentelli, UC Berkeley, US and Trento U, IT
J Sifakis, VERIMAG, FR

Moderator:
A Sangiovanni-Vincentelli, UC Berkeley, US and Trento U, IT

It is essential that theoretical results developed by the community of researchers in the domain of compositionality be integrated in coherent component-based design flows that must validated in comparison with existing industrial practices. Furthermore, compositionality results should be implemented in scalable supporting methods and tools. The special session presents a component-based design flow, its application to specific industrial domains and to diverse areas of design endeavors such as energy efficient buildings and synthetic biology.

1700 **METHODS AND TOOLS FOR COMPONENT-BASED DESIGN**
J Sifakis, VERIMAG, FR

1730 **USING CONTRACT-BASED COMPONENT SPECIFICATIONS FOR VIRTUAL INTEGRATION AND ARCHITECTURE DESIGN**
W Damm, E Thaden, I Stierand, T Peikenkamp and H Hungar, OFFIS, DE

1800 **COMPONENT-BASED DESIGN FOR THE FUTURE**
A Sangiovanni-Vincentelli,
UC Berkeley, US and Trento U, IT

1830 **CLOSE**

8.8 EMBEDDED TUTORIAL – Communication Networks in Next Generation Automobiles

Room – Exhibition Theatre **1700-1830**

Organisers:
T Kazmierski, Southampton U, UK
C Grimm, TU Vienna, AT

Moderator:
C Grimm, TU Vienna, AT

The tutorial addresses upcoming technologies aimed at communication networks for automotive applications. The first presentation will discuss applications of networked or even autonomous sensors in a car. The second presentation will emphasise novel, cross-industry communication technologies that enhance the standard IEEE 802.3 switched Ethernet.

The third and fourth presentations will introduce applications and methods for the design of wireless communication in a car, including methods for wireless energy supply of sensor nodes in cars as well as design tools and methods for design of wireless sensor nodes.

1700 **SENSOR NETWORKS ON THE CAR: STATE OF THE ART AND FUTURE CHALLENGES**
L D'Orazio, Centro Ricerche FIAT (Trento Branch), IT

1730 **TIME-TRIGGERED ETHERNET FOR AUTOMOTIVE APPLICATIONS**
M Schwarz, TTTech Computertechnik AG, AT

1800 **REAL-TIME WIRELESS COMMUNICATION IN AUTOMOTIVE APPLICATIONS**
R Matischek and T Herndl,
Infineon Technologies Austria AG, AT
C Grimm and J Haase, TU Vienna, AT

1815 **WIRELESS COMMUNICATION AND ENERGY HARVESTING IN AUTOMOBILES**
T Kazmierski, Southampton U, UK
S Mahlknecht and C Grimm, TU Vienna, AT

1830 **CLOSE**

Intelligent Energy Management - Supply and Utilisation Special Day

THURSDAY 17 MARCH, 2011

0730 REGISTRATION and SPEAKERS' BREAKFAST

9.1 INTELLIGENT ENERGY MANAGEMENT TUTORIAL – Energy Transfer, Generation and Power Electronics

Room – Oisans 0830-1000

Organisers:
P Mitcheson, Imperial College, UK
P K Wright, UC Berkeley, US

Moderator:
P Mitcheson, Imperial College, UK

Issues relating to energy resources are set to play an increasing role in all of our futures. This special day at DATE is intended to further involve the EDA community in energy related matters at all scales. This session covers setting the scene for the day on energy, covering topics from levels of micro Watts to Giga Watts.

0830 **ENERGY HARVESTING FROM MOTION: FUNDAMENTALS AND FUTURE CHALLENGES**
E Halvorsen, Vestfold U College, NO

0900 **POWER MANAGEMENT TRENDS IN PORTABLE CONSUMER APPLICATIONS**
J Brown, Wolfson Microelectronics, UK

0930 **WHY THE LIGHTS DON'T GO OUT MORE OFTEN, WHY THEY MIGHT IN FUTURE AND HOW A 'SMARTER GRID' CAN HELP**
K Bell, Strathclyde U, UK

1000 **EXHIBITION BREAK/IP4**

9.2 Design Automation Methodologies for Emerging Technologies

Room – Meije 0830-1000

Moderators:
K Mohanram, Rice U, US
S Bhanja, South Florida U, US

The first paper presents a mask optimisation method; the second paper shows techniques for digital microfluidic biochps; the third paper presents the design of FPGA using NEMS; and the last paper shows a case study to improve chip reliability with CNT thermal

0830 **AN EFFICIENT MASK OPTIMISATION METHOD BASED ON HOMOTOPY CONTINUATION TECHNIQUE**
F Liu, IBM Austin Research Lab, US
X Shi, Intel Corp, US

0900 **WASTE-AWARE DILUTION AND MIXING OF BIOCHEMICAL SAMPLES WITH DIGITAL MICROFLUIDIC BIOCHIPS**
S Roy, Indian Institute of Technology Kharagpur, IN
B B Bhattacharya, Indian Statistical Institute Kolkata, IN
K Chakrabarty, Duke U, US

0930 **HIGH-TEMPERATURE (>500°C) FPGA USING SIC NANO-ELECTRO-MECHANICAL SYSTEM SWITCHES**
X Wang, S Narasimhan, A Krishna, F Wolff, T-H Lee, S Rajagopal, M Mehregany and S Bhunia,
Case Western Reserve U, US

0945 **CASE STUDY: LEVERAGING HOTSPOTS AND IMPROVING CHIP RELIABILITY VIA CARBON NANOTUBE THERMAL INTERFACE**
W Zhang, Nanyang Technological U, SG
J Huang and S Yang, Shanghai U, PRC
P Gupta, Intel Corp, US

IPs **IP4-5, IP4-11 AND IP4-15**

1000 **EXHIBITION BREAK/IP4**

9.3 System Modelling

Room – Belle-Etoile **0830-1000**

Moderators:
J Haase, TU Vienna, AT
D Borrione, TIMA Laboratory, FR

The first paper applies the SMT technology to find if a given behaviour can be exercised in a UML model. The second paper describes an automated technique for generating a performance model for a wireless sensor network. The third paper presents an efficient transaction-level model for a specific NoC router. Finally, the fourth paper proposes a high-level analytical model for chip multiprocessing systems.

0830 **VERIFYING DYNAMIC ASPECTS OF UML MODELS**
M Soeken, R Wille and R Drechsler, Bremen U, DE

0900 **AUTOMATED CONSTRUCTION OF FAST AND ACCURATE SYSTEM-LEVEL MODELS FOR WIRELESS SENSOR NETWORKS**
L Bai and R P Dick, U of Michigan, US
P A Dinda, Northwestern U, US
P Chou, UC Irvine, US

0930 **FAST AND ACCURATE TRANSACTION-LEVEL MODEL OF A WORMHOLE NETWORK-ON-CHIP WITH PRIORITY PREEMPTIVE VIRTUAL CHANNEL ARBITRATION**
L S Indrusiak and O M Dos Santos, York U, UK

0945 **A HIGH-LEVEL ANALYTICAL MODEL FOR APPLICATION SPECIFIC CMP DESIGN EXPLORATION**
A Cassidy, H Zhou and A G Andreou, Johns Hopkins U, US
K Yu, Carnegie Mellon U, US

IPs **IP4-6 AND IP4-12**

1000 **EXHIBITION BREAK/IP4**

9.4 Modelling and Verification of Analogue and RF Circuits

Room – Stendhal **0830-1000**

Moderators:
L Hedrich, Frankfurt U, DE
M Olbrich, Hannover U, DE

The session includes modelling and optimisation of leading edge circuit structures applied to an SRAM cell and a 60 GHz inductor loop. An abstract theory for entrainment and an advanced jitter tolerance analysis improves the automatic design and analysis of PLLs and oscillators. Novel methods for symbolic classification and stochastic process variation analysis are presented as interactive presentations.

0830 **GLOBAL OPTIMISATION OF INTEGRATED TRANSFORMERS FOR HIGH FREQUENCY MICROWAVE CIRCUITS USING A GAUSSIAN PROCESS BASED SURROGATE MODEL**
B Liu, P Reynaert and G Gielen, KU Leuven, BE

0900 **A METHOD FOR FAST JITTER TOLERANCE ANALYSIS OF HIGH-SPEED PLLS**
S Erb, W Pribyl, TU Graz, AT

0930 **ENTRAINMENT - THEORY AND APPLICATIONS**
H G Brachtendorf,
U of Applied Science of Upper Austria, AT
R Laur, Bremen U, DE

0945 **SAMURAI: AN ACCURATE METHOD FOR MODELLING AND SIMULATING NON-STATIONARY RANDOM TELEGRAPH NOISE IN SRAMS**
K V Aadithya, S Venugopalan and J Roychowdhury, UC Berkeley, US
A Demir, Koc U, TK

IPs **IP4-7 AND IP4-13**

1000 **EXHIBITION BREAK/IP4**

9.5 INDUSTRIAL 2

Room – Chartreuse 0830-1000

Moderators:
D Sciuto, Politecnico di Milano, IT
L Anghel, TIMA Laboratory, FR

This session is dedicated to presentations in which industry points out to the community real-life design and technology challenges that should be addressed in the short-to-medium term. Further details about the topics presented in this session can be found in the 2-page industrial papers included in the conference proceedings.

0830 **CHARACTERISATION OF AN INTELLIGENT POWER SWITCH FOR LED DRIVING WITH CONTROL OF WIRING PARASITICS EFFECTS**
G Pasetti, F Tinfena, R Serventi and P D'Abramo, Austriamicrosystems, IT
N Constantino, S Saponara and L Fanucci, Pisa U, IT

0845 **ENERGY ANALYSIS METHODS AND TOOLS FOR MODELING AND OPTIMISING TYRE SYSTEMS**
M Sabatini, Pirelli Tyre S.p.A, IT
A Bonanno and A Bocca, Politecnico di Torino, IT

0900 **SYSTEM LEVEL TECHNIQUES TO IMPROVE RELIABILITY IN HIGH POWER MICROCONTROLLERS FOR AUTOMOTIVE APPLICATIONS**
M Ottella and M Sciolla, Centro Ricerche Fiat, Orbassano, IT
A Acquaviva and M Poncino, Politecnico di Torino, IT

0915 **SYSTEM-LEVEL POWER ESTIMATION METHODOLOGY USING CYCLE- AND BIT-ACCURATE TLM**
M D Grammatikakis, E Politis and C Papadas, ISD S.A., GR
J-P Schoellkopf, ASTUS-SA, FR

0930 **ECO PASSIVE INTELLIGENT BUILDING**
C Sapienza, Foster Marketing, IT

0945 **MOVING TO GREEN ICT: FROM STAND-ALONE POWER-AWARE IC DESIGN TO AN INTEGRATED APPROACH TO ENERGY EFFICIENT DESIGN OF HETEROGENEOUS ELECTRONIC SYSTEMS**
S Rinaudo and G Gangemi, STMicroelectronics, IT
A Calimera, A Macii and M Poncino, Politecnico di Torino, IT

1000 **EXHIBITION BREAK/IP4**

9.6 Embedded System Resource Allocation and Management

Room – Bayard **0830-1000**

Moderators:
S Chakraborty, TU Munich, DE
A Girault, INRIA, Rhone-Alpes, FR

This session features papers on real-time scheduling and allocation problems, with specific focus on multicore and low-power embedded systems. The first paper addresses the important problem of how to assign resources to concurrent real-time applications in a heterogeneous multicore Network on a Chip, in order to optimise a user defined goal. The proposed procedure (workflow) is performed on-line and is based on an heuristic that tries to balance often contrasting requirements on three different types of resources, namely computational resources, memory consumption and communication bandwidth. The second paper addresses the problem of minimising energy on modern multicore systems, where different cores may be grouped into islands that share the same clock source. The authors propose a methodology for frequency scaling that directly takes into account the multicore scheduling problem. The third paper addresses the problem of improving the reliability of modern scratchpad memories by applying techniques similar to the RAID system used mass-storage, with the objective of minimising power and performance overhead. The authors show that their proposed methodology has less overhead than traditional parity-check and cyclic redundancy techniques.

0830 **A WORKFLOW FOR RUNTIME ADAPTIVE TASK ALLOCATION ON HETEROGENEOUS MPSOCS**
J Huang, A Raabe, C Buckl, Fortiss GmbH, DE
A Knoll, TU Munich, DE

0900 **ENERGY-EFFICIENT SCHEDULING OF REAL-TIME TASKS ON CLUSTER-BASED MULTICORES**
F Kong and Q Deng, Northeastern U, PRC
W Yi, Uppsala U, SE

0930 **E-ROC: EMBEDDED RAIDS-ON-CHIP FOR LOW POWER DISTRIBUTED DYNAMICALLY MANAGED RELIABLE MEMORIES**
L A D Bathen and N D Dutt, UC Irvine, US

IP **IP4-8**

1000 **EXHIBITION BREAK/IP4**

9.7 EMBEDDED TUTORIAL – Sub-Wave Length Lithography and Variability Aware Test and Characterisation Methods

Room – Les Bans 0830-1000

Organiser:
S Kundu, U of Massachusetts Amherst, US

Moderator:
R Galivanche, Intel Corporation, US

Manufacturing small MOSFET devices and interconnect wires today requires printing of polygons that can have feature widths below quarter wavelength of the light source used in photolithography. Parametric control in photolithography steps such as resist coating, exposure, etch, doping, oxide deposition and surface planarisation contribute to process variation. Process variation leads to changes in circuit parameters such as Leff and VT that lead to problems in design centering, yield, time to market and ultimately cost. Variability aware solutions may involve variation tolerant design methods that span across multiple levels of design. Solutions at the system level may include clock tuning, adaptive body bias, adaptive voltage control. At the circuit level, they include sizing and self-compensation methods. At the layout level, it encompasses layout hardening techniques. At the test level, the road takes two forks: one for modeling and characterisation and the other for manufacturing test. At the characterisation level, special structures and tests are needed to expose the extent of variation and models to support variability aware test development. This session features an overview presentation from Sandip Kundu followed by a talk by Miguel Miranda covering variability aware modelling for SRAM memories. The final presenter in this session is Rob Aitken who will speak on the problem of correlating models and silicon for improving parametric yield.

0830 **MODELLING MANUFACTURING PROCESS VARIATION FOR DESIGN AND TEST**
S Kundu and A Sreedhar, U of Massachusetts Amherst, US

0900 **VARIABILITY AWARE MODELLING FOR YIELD PREDICTION & ENHANCEMENT OF SRAM AND LOGIC**
M Miranda, P Zuber, P Dobrovolny and P Roussel, IMEC, BE

0930 **CORRELATING MODELS AND SILICON FOR IMPROVED PARAMETRIC YIELD**
R Aitken, ARM, US

1000 **EXHIBITION BREAK/IP4**

IP4 Interactive Presentations

Room - Salle de Reception 1000-1030

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the morning. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP4-1 **EVALUATING ENERGY CONSUMPTION OF HOMOGENEOUS NOC-BASED MPSoCs USING SPARE TILES**
A M Amory, L C Ost, C A M Marcon and F G Moraes, PUCRS, BR
M Lubaszewski, UFRGS, BR

IP4-2 **IMPROVING THE EFFICIENCY OF A HARDWARE TRANSACTIONAL MEMORY ON AN NoC-BASED MPSoC**
L Kunz, G Girao and F R Wagner, UFRGS, BR

IP4-3 **ANALYTICAL MODEL FOR SRAM DYNAMIC WRITE-ABILITY DEGRADATION DUE TO GATE OXIDE BREAKDOWN**
V Chandra and R Aitken, ARM, US

IP4-4 **MULTI-LEVEL ATTACK: AN EMERGING THREAT MODEL FOR CRYPTOGRAPHIC HARDWARE**
S S Ali, R S Chakraborty and D Mukhopadhyay, Indian Institute of Technology Kharagpur, IN
S Bhunia, Case Western Reserve U, US

IP4-5 **NEW REVERSIBLE DESIGN OF BCD ADDER**
H Thapliyal and N Ranganathan, South Florida U, US

IP4-6 **JTLM: AN EXPERIMENTATION FRAMEWORK FOR THE SIMULATION OF TRANSACTION-LEVEL MODELS OF SYSTEMS-ON-CHIP**
G Funchal, STMicroelectronics and Verimag, FR
M Moy, Verimag, FR

IP4-7 **ENSURING CORRECTNESS OF ANALOG CIRCUITS IN PRESENCE OF NOISE AND PROCESS VARIATIONS USING PATTERN MATCHING**
R Narayanan and S Tahar, Concordia U, CA
M H Zaki, U of British Columbia, CA

IP4-8 **A MULTI-OBJECTIVE DECISION-THEORETIC EXPLORATION ALGORITHM FOR PLATFORM BASED DESIGN**
G Beltrame and G Nicolescu, Ecole Polytechnique de Montreal, CA

IP4-9 **PREDICTING BUS CONTENTION EFFECTS ON ENERGY AND PERFORMANCE IN MULTI-PROCESSOR SoCo**
S Penolazzi, I Sander and A Hemani, Royal Institute of Technology, SE

IP4-10 **SPECIALISED LOW-COST VECTORISED LOOP BUFFER FOR EMBEDDED PROCESSORS**
L Huang and Z Wang, National U of Defense Technology, PRC

IP4-11 **DETERMINING THE MINIMAL NUMBER OF LINES FOR LARGE REVERSIBLE CIRCUITS**
R Wille, O Keszoecze and R Drechsler, Bremen U, DE

IP4-12 **DYNAMIC APPLICATIONS ON RECONFIGURABLE SYSTEMS: FROM UML MODEL DESIGN TO FPGAS IMPLEMENTATION**
J Vidal, F De Lamotte, G Gogniat, J-P Diguet and S Guillet, European U of Brittany - UBS – CNRS, FR

IP4-13 **A SYMBOLIC TECHNIQUE FOR AUTOMATED CHARACTERISATION OF THE UNIQUENESS AND SIMILARITY OF ANALOG CIRCUIT DESIGN FEATURES**
C Ferent and A Doboli,
State U of New York at Stony Brook, US

IP4-14 **COORDINATE STRIP-MINING AND KERNEL FUSION TO LOWER POWER CONSUMPTION ON GPU**
G Wang, National U of Defense Technology, PRC

IP4-15 **AN EFFICIENT QUANTUM-DOT CELLULAR AUTOMATA ADDER**
F Bruschi, F Perini, V Rana and D Sciuto,
Politecnico di Milano, IT

10.1.1 INTELLIGENT ENERGY MANAGEMENT – Smart Energy Generation: Design Automation and the Smart-Grid

Room – Oisans **1100-1230**

Organisers:
P Mitcheson, Imperial College, UK
P K Wright, UC Berkeley, US

Moderator:
P K Wright, UC Berkeley, US

This session will look at issues relating to the supply side of the electrical grid, including smart grids and the role of electric vehicles in future supply infrastructure and includes talks from both industry and academia.

1100 **UNDERSTANDING THE ROLE OF BUILDINGS IN A SMART MICROGRID**
Y Agarwal, T Weng and R K Gupta, UC San Diego, US

1130 **THE SMART-GRID: A DATA-CRUNCHING PERSPECTIVE**
P Feldmann, IBM T J Watson Research Centre, US

1200 **eCAR IN ITS SMART-GRID INFRASTRUCTURE – HOLISTIC APPROACH OF SIEMENS**
G Spiegelberg, Siemens Corporate Technology, DE

1230 **LUNCH BREAK**

10.2 Advanced Algorithms and Applications for Reconfigurable Computing

Room – Meije 1100-1230

Moderator:
M Huebner, Karlsruhe Institute of Technology (KIT), DE
C Passerone, Politecnico di Torino, IT

This session presents three papers which describe advanced algorithms to accelerate complex applications on FPGAs in the domains of cryptography, image processing and satisfiability analysis.

1100 **THEORETICAL MODELING OF THE ITOH-TSUJII INVERSION ALGORITHM FOR ENHANCED PERFORMANCE ON K-LUT BASED FPGAS**
S S Roy, C Rebeiro and D Mukhopadhyay, Indian Institute of Technology Kharagpur, IN

1130 **A STREAMING MODEL FOR FPGA ACCELERATORS AND ITS APPLICATION TO REAL-TIME SALIENCY DETECTION**
S Kestur, D Dantara and V Narayanan, The Pennsylvania State U, US

1200 **A RECONFIGURABLE, PIPELINED, CONFLICT DIRECTED JUMPING SEARCH SAT SOLVER**
M Safar and M Watheq ElKharashi, Ain Shams U, EY
M Shalan, American U in Cairo, EY
A Salem, Mentor Graphics, EY

1230 **LUNCH BREAK**

10.3 System Optimisations and Adaptivity

Room – Belle-Etoile 1100-1230

Moderators:
M Berekovic, TU Braunschweig, DE
S Yehia, Thales Research and Technology, FR

This session features five papers focused on system optimisation and adaptivity. Techniques are presented to improve system robustness, reduce the cost of MP interconnect, increase system performance, and demonstrate adaptivity.

1100 **REDUCING THE COST OF REDUNDANT EXECUTION IN SAFETY-CRITICAL SYSTEMS USING RELAXED DEDICATION**
B H Meyer, N George, J Lach, B Calhoun and K Skadron, Virginia U, US

1130 **FRUGAL FIXED SILICON BUT FLEXIBLE TOPOLOGIES FOR MULTICORE PLATFORMS IN SUPPORT OF RESOURCE VARIATION-DRIVEN ADAPTIVITY**
C Yang, Delaware U, US
A Orailoglu, UC San Diego, US

1200 **MINORITY-GAME-BASED RECONFIGURABLE FABRIC RESOURCE ALLOCATION FOR RUN-TIME RECONFIGURABLE MULTI-CORE PROCESSORS**
M Shafique, L Bauer, W Ahmed and J Henkel, Karlsruhe Institute of Technology (KIT), DE

IPs **IP5-1, IP5-5 AND IP5-11**

1230 **LUNCH BREAK**

10.4 Design and Simulation of Mixed-Signal Systems

Room – Stendhal **1100-1230**

Moderators:
M Louerat, UPMC Paris, FR
I O'Connor, EC Lyon, FR

Raising the level of abstraction of design and simulation of mixed signal and mixed technology systems is an essential step towards accelerating the design of complex heterogeneous systems. The first paper in this session proposes an approach to solve the issue of long simulation times in energy harvesting systems. In the second paper, tight links are set up between system and transistor levels to adjust specifications early in the design cycle. The third paper describes an extension of a high level design language to handle distributed components modelled with partial differential equations. The impact of ageing on the reliability of analogue circuits is discussed in the fourth paper through the application of an analysis framework on a current steering DAC. Finally an IP discusses the use of the AMS extension of SystemC on a wireless sensor network.

1100 (A) **ACCELERATED SIMULATION OF TUNABLE KINETIC ENERGY HARVESTING SYSTEMS USING STATE-SPACE TECHNIQUE**
L Wang, T J Kazmierski, B M Al-Hashimi, A S Weddell, G V Merrett and I N Ayala, Southampton U, UK

1130 **SIMULATION BASED TUNING OF SYSTEM SPECIFICATION**
Y Zaidi, C Grimm and J Haase, TU Vienna, AT

1200 **AN EXTENSION TO SYSTEMC-A TO SUPPORT MIXED-TECHNOLOGY SYSTEMS WITH DISTRIBUTED COMPONENTS**
C Zhao and T J Kazmierski, Southampton U, UK

1215 **STOCHASTIC CIRCUIT RELIABILITY ANALYSIS**
E Maricau and G Gielen, KU Leuven, BE

IP **IP5-2**

1230 **LUNCH BREAK**

10.5 Advances in Test Generation and Fault Simulation

Room – Chartreuse 1100-1230

Moderators:
I Polian, Passau U, DE
A Virazel, LIRMM, FR

This session addresses the challenges of both offline and online test generation for delay faults, as well as fault coverage evaluation in the presence of unknowns.

1100 **AS-ROBUST-AS-POSSIBLE TEST GENERATION IN THE PRESENCE OF SMALL DELAY DEFECTS USING PSEUDO-BOOLEAN OPTIMISATION**
S Eggersgluess and R Drechsler, Bremen U, DE

1130 **BUILT-IN GENERATION OF FUNCTIONAL BROADSIDE TESTS**
I Pomeranz, Purdue U, US

1200 **SAT-BASED FAULT COVERAGE EVALUATION IN THE PRESENCE OF UNKNOWN VALUES**
M A Kochte and H-J Wunderlich, Stuttgart, DE

1230 **LUNCH BREAK**

10.6 Model Based Verification and Synthesis of Embedded Systems

Room – Bayard 1100-1230

Moderators:
R Majumdar, Max Planck Institute for Software Systems, DE
P Pop, TU Denmark, DK

The first paper suggests an algorithm that minimises the overall cost of producing an embedded system, including the cost of testing the system and expected losses from an incompletely tested design. The approach is based on a Bayesian model for probabilistic system testing. The following two presentations address the issue of synchronisation and scheduling on multiprocessor systems. The second paper proposes an approach to determine the amount of resynchronisation while preventing deadlock and satisfying the throughput constraint of an application. The last presentation proposes a method for pipelined schedule synthesis of streaming applications running on heterogeneous multicore platforms.

1100 **WHEN TO STOP VERIFICATION? STATISTICAL TRADE-OFF BETWEEN EXPECTED LOSS AND SIMULATION COST**
S K Jha, U of Central Florida, US
C J Langmead, Carnegie Mellon U, US
S Ramesh and S Mohalik, General Motors, US

1130 **RESYNCHRONISATION OF CYCLO-STATIC DATAFLOW GRAPHS**
J P H M Hausmans and H Corporaal, TU Eindhoven, NL
M J G Bekooij, NXP Semiconductors, NL

1200 **PIPELINE SCHEDULE SYNTHESIS FOR REAL-TIME STREAMING TASKS WITH INTER/INTRA-INSTANCE PRECEDENCE CONSTRAINTS**
Y-S Chiu and C-S Shih, National Taiwan U, ROC

IPs **IP5-3 AND IP5-9**

1230 **LUNCH BREAK**

10.7 EMBEDDED TUTORIAL – Die Stacking Goes Mobile and Embedded

Room – Les Bans 1100-1230

Organiser:
A Jerraya, CEA-LETI MINATEC, FR

Moderator:
Y Xie, Penn State U, US

The focus of this session is in-depth investigations on the application of 3D die stacking to mobile and embedded devices. 3D die stacking is expected to go for mass production in near future in some markets, e.g., imagers. Industrial high-end mobile SoCs as well as CMPs are being actively redesigned to exploit the increased bandwidth of 3D stacked memories. 3D die stacking is expected to tip in very near future in both markets of mobile/embedded and high-end devices. In this embedded tutorial, recent technical achievements and future projections on 3D die stacking technology and its applications are presented. Especially, the feasibility and impact of 3D die stacking on mobile and embedded systems are stressed.

1100 **FROM ACTIVE INTERPOSER TO ADVANCED CMOS STACK: OVERVIEW OF 3D DIE STACKING TECHNOLOGY AND RELATED KEY ISSUES**
N Sillon, D Henry, S Cheramy, P Leduc, G Simon and J Charbonnier, CEA-LETI MINATEC, FR

1130 **3D EMBEDDED MULTI-CORE: SOME PERSPECTIVES**
F Clermidy, F Darve, D Dutoit and P Vivet, CEA-LETI MINATEC, FR

1145 **3D DIE STACKING'S IMPACT ON MOBILE SOC DESIGN AND MOBILE PRODUCT MARKET**
P Boulet, STEricsson, FR

1200 **A QUANTITATIVE ANALYSIS OF PERFORMANCE BENEFITS OF 3D DIE STACKING ON MOBILE AND EMBEDDED SOC**
S Yoo, D Kim and S Lee, POSTECH, KR
J H Ahn, Seoul National U, KR
H Jung, Samsung Electronics, KR

1230 **LUNCH BREAK**

10.8 PANEL SESSION – State of the Art Verification Methodologies in 2015

Room – Exhibition Theatre **1100-1230**

Organiser:
T Fitzpatrick, Mentor Graphics, US

Moderator:
A Crone, Mentor Graphics, SE

Panellists:
C Chevallaz, STMicroelectronics, FR
B Dickman, ARM, UK
V Esen, Infineon Technologies, DE
O Bringmann, FZI, DE
M Rohleder, Freescale, DE

In the last few years, the industry has seen acceleration in the evolution of verification methodologies. While the industry focus has been on enabling a standard based approach to help today's challenges, one can wonder what is needed to prepare us self for the further verification challenges. The expert panellists will discuss the many aspects of verification methodologies, the requirements and predictions for verification methodologies needed 4-5 years from now on.

1230 **LUNCH BREAK**

10.1.2 SPECIAL DAY KEYNOTE

Room – Oisans **1330-1400**

Organiser/Moderator:
P K Wright, UC Berkeley, US

Keynote Speaker:
Carmelo Papa, Executive VP Industrial and Multisegment, STMicroelectronics, IT

SMART ENERGY AT ST

Abstract: The exponential increase of world energy demand, with a forecasted raise of 45%[1] between 2010 and 2030, makes energy management one of the most urgent topics of the century and a key driver for semiconductors and electronics products evolution. The main solutions for world energy demand and global warming issues have been individuated in two main streams: an increasing offer from alternative energy sources and their integration into the new Smart Grid and a reduction of the demand through an increase of systems efficiency.

In energy supply and distribution, the Smart Grid is in fact impacting for an estimated 14% of CO2[2] emissions reduction in the global energy system by 2020. In addition it makes it possible to generate high cost savings for industrial and economic system (188 Billion$ per year estimated only for U.S.[2])

New measures for Energy Efficiency will contribute up to 8 Giga-Tons of CO2 reduction (54% of total with the application of policy 450[1]) by 2020, mostly thanks to power electronics applications.

Along these two areas of intervention, ST is investing to provide both effective power semiconductor technologies and ICs for new topologies for power conversion, but not only. New materials (SiC) for power transistors, innovative solutions for power management and digital control, wired and wireless ICs are some examples of ST offer that apply to energy related applications like PV converters, Smart Metering, Connectivity, Building Automation, Electrical Traction and Motor Control.

Along the energy theme, though at different orders of magnitude, innovation for portable systems is tackled at ST R&D: extremely low consuming CMOS technology for digital ICs, low power RF transceivers, milliWatt capable super thin batteries and 3D integration techniques are the base for miniaturised, long lasting battery based systems, that enable new scenarios especially in portable Healthcare and Wireless Autonomous Sensors Networks.

[1] Source: International Energy Agency
[2] Source: The Climate Group
[3] Source: Grid 2030 A National Vision for Electricity s Second 100 Years, United States Department of Energy, Office of Electric Transmission and Distribution

1400 **END OF SESSION**

11.1 INTELLIGENT ENERGY MANAGEMENT – Smart Energy Utilisation: From Circuits to Consumer Products

Room – Oisans **1400-1530**

Organisers:
P Mitcheson, Imperial College, UK
P K Wright, UC Berkeley, US

Moderator:
P Mitcheson, Imperial College, UK

This session concentrates on smart use of energy at the demand side - from energy issues at the circuit level to larger scale issues with consumer products and use of energy in the home.

1400 **ENERGY-MODULATED COMPUTING**
A Yakovlev, Newcastle U, UK

1430 **ENHANCED WIRELESS ENERGY TRANSFER USING STRONGLY-COUPLED MAGNETIC RESONANCE**
M Kesler, Witricity, US

1500 **DIGITAL SERVICES AND SMART ENERGY NETWORKS**
M Perry, BRE, UK

1530 **BREAK/IP5**

11.2 Architectural Innovations for Reconfigurable Computing

Room – Meije 1400-1530

Moderators:
D Goehringer, Fraunhofer Institute, DE
K Bertels, TU Delft, NL

This session describes advances in novel cache controllers for adaptive computing systems, specialised interconnect topologies for coarse grained computing arrays and adaptive VLIW and SIMD processor architectures.

1400 **I2CRF: INCREMENTAL INTERCONNECT CUSTOMISATION FOR EMBEDDED RECONFIGURABLE FABRICS**
J W Yoon, J Jung, S Park, Y Kim and Y Paek, Seoul National U, KR
J Lee, Ulsan National Institute of Science and Technology, KR

1430 **MARC II: A PARAMETRISED SPECULATIVE MULTI-PORTED MEMORY SUBSYSTEM FOR RECONFIGURABLE COMPUTERS**
H Lange, LOEWE Research Center AdRIA, Darmstadt, DE
T Wink and A Koch, TU Darmstadt, DE

1500 **TARGETING CODE DIVERSITY WITH RUN-TIME ADJUSTABLE ISSUE-SLOTS IN A CHIP MULTIPROCESSOR**
F Anjam, TU Delft, NL

1530 **BREAK/IP5**

11.3 Asynchronous Circuits and Advanced Timing Issues in Logic Synthesis

Room – Belle-Etoile 1400-1530

Moderators:
T Villa, Verona U, IT
P Vivet, CEA-LETI, FR

This session features papers on clock skew scheduling, bus encoding and timing issues in asynchronous logic.

1400 **AN EFFICIENT ALGORITHM FOR MULTI-DOMAIN CLOCK SKEW SCHEDULING**
Y Zhi, W-S Luk, X Zeng and H Zhu, Fudan U, PRC
H Zhou, Northwestern U, US

1430 **A DELAY-INSENSITIVE BUS-INVERT CODE AND HARDWARE SUPPORT FOR ROBUST ASYNCHRONOUS GLOBAL COMMUNICATION**
M Y Agyekum and S M Nowick, Columbia U, US

1500 **REDRESSING TIMING ISSUES FOR SPEED-INDEPENDENT CIRCUITS IN DEEP SUBMICRON AGE**
Y Li, T Mak and A Yakovlev, Newcastle U, UK

IPs **IP5-4, IP5-6 AND IP5-7**

1530 **BREAK/IP5**

11.4 High Level Synthesis

Room – Stendhal 1400-1530

Moderators:
S Singh, Microsoft Research, Cambridge, UK
P Brisk, UC Riverside, US

This session presents latest advances in High Level Synthesis, ranging from theoretical contributions to realistic applications, from models and representations to synthesis of efficient arithmetic circuits, and from optimisation of silicon estate and delay to minimisation of power consumption.

1400 **REALISTIC PERFORMANCE-CONSTRAINED PIPELINING IN HIGH-LEVEL SYNTHESIS**
A Kondratyev, L Lavagno, M Meyer and Y Watanabe, Cadence Design Systems, US

1430 **OPTIMISATION OF MUTUALLY EXCLUSIVE SUM-OF-PRODUCT DATAPATH**
T Drane and G Constantinides, Imperial College London, UK

1445 **INTERMEDIATE REPRESENTATIONS FOR CONTROLLERS IN CHIP GENERATORS**
K Kelley, A Danowitz, M Horowitz, S Richardson, P Stevenson and M Wachs, Stanford U, US

1500 **POWER OPTIMISATION IN HETEROGENOUS DATAPATHS**
A A Del Barrio, M C Molina, J M Mendias and R Hermida, Madrid Complutense U, ES
S O Memik, Northwestern U, US

1515 **ABSTRACT STATE MACHINES AS AN INTERMEDIATE REPRESENTATION FOR HIGH-LEVEL SYNTHESIS**
H D Patel and R Sinha, Waterloo U, CA

IPs **IP5-8 AND IP5-10**

1530 **BREAK/IP5**

11.5 New Directions in Testing

Room – Chartreuse 1400-1530

Moderators:
J Schloeffel, Mentor Graphics, DE
J Tyszer, TU Poznan, PL

This session deals with issues in standardising test and debug access, testing 3D IC stacks and adaptive testing. The first paper presents a method to construct and optimise IEEE P1687 instrumented networks. The next two papers focus on prebond testing of dies for 3D stacks. While the second paper shows how to generate test and scan clocks in 3D ICs using DLLs, the third paper proposes an algorithm for circuit partitioning to facilitate efficient prebond testing. Finally, the fourth paper presents a method to optimise manufacturing test by adaptive test pattern reordering.

1400 **DESIGN AUTOMATION FOR IEEE P1687**
F G Zadegan, U Ingelsson and E Larsson, Linkoping U, SE
G Carlsson, Ericsson AB, SE

1430 **ON TESTING PREBOND DIES WITH INCOMPLETE CLOCK NETWORKS IN A 3D IC USING DLLS**
M Buttrick and S Kundu, U of Massachusetts Amherst, US

1500 **HYPER-GRAPH BASED PARTITIONING TO REDUCE DFT COST FOR PRE-BOND 3D-IC TESTING**
A Kumar and S M Reddy, Iowa U, US
I Pomeranz, Purdue U, US
B Becker, Albert-Ludwigs-U of Freiburg, DE

1515 **ADAPTIVE TEST OPTIMISATION THROUGH REAL TIME LEARNING OF TEST EFFECTIVENESS**
B Arslan and A Orailoglu, UC San Diego, US

1530 **BREAK/IP5**

11.6 Hardware Design for Multimedia Applications

Room – Bayard **1400-1530**

Moderators:
F Clermidy, CEA-LETI, FR
A Baghdadi, Telecom Bretagne, FR

This session on Multimedia includes three papers. The first one proposes a new hardware design and FPGA implementation of the Chambolle algorithm for optical flow estimation. The second paper, describes a novel approach for face detection, which exploits depth information to improve energy efficiency and performance. The third paper addresses the motion and disparity estimation problem using multi-view video encoding proposing a pipelined hardware design.

1400 **A HIGH-PERFORMANCE PARALLEL IMPLEMENTATION OF THE CHAMBOLLE ALGORITHM**
A Akin, I Beretta, V Rana and D Atienza, EPF Lausanne, CH
A Nacci and M D Santambrogio, Politecnico di Milano, IT

1430 **DEPTH-DIRECTED HARDWARE OBJECT DETECTION**
C Kyrkou, C Ttofis and T Theocharides, Cyprus U, CY

1500 **MULTI-LEVEL PIPELINED PARALLEL HARDWARE ARCHITECTURE FOR HIGH THROUGHPUT MOTION AND DISPARITY ESTIMATION IN MULTIVIEW VIDEO CODING**
B Zatt and S Bampi, UFRGS, BR
M Shafique and J Henkel, Karlsruhe Institute of Technology (KIT), DE

1530 **BREAK/IP5**

11.7 HOT TOPIC – New Frontiers in Embedded Systems Design: Technology and Applications

Room – Les Bans **1400-1530**

Organiser:
G De Micheli, EPF Lausanne, CH

Moderators:
H Meyr, RWTH Aachen U, DE

This session reports on work addressing the design of distributed embedded systems.

The first two presentations address two application areas. The former deals with subcutaneous smart implants that can communicate with patient monitoring systems. The latter deals with environmental systems to monitor glaciers, in view of the effects of global warming

The remaining two presentations address the two technological sides of the spectrum of computational units: high-performance and ultra-low-power processing respectively. The first paper addresses issues related to 3-dimensional integration and ways and means to control temperature in 3D structures, including the use of micro-cooling. The second paper addresses the underlying technologies for distributed embedded systems where power consumption has to be carefully monitored.

These four contributions are related to projects developed within the nano-tera.ch program for researching distributed embedded systems for health and the environment.

1400 **A PLATFORM FOR INTEGRATED SENSING FOR REMOTE MONITORING OF HUMAN METABOLISM**
G De Micheli, C Boero, S Carrara and S Ghoreishizadeh, EPF Lausanne, CH
F Valgimigli, Menarini, IT

1430 **X-SENSE: SENSING IN EXTREME ENVIRONMENT**
J Beutel, L Thiele, M Keller, B Buchli, M Zimmerling and F Ferrari, ETH Zurich, CH

1500 **TOWARDS THERMAL-AWARE DESIGN OF 3D MPSoCs WITH INTERLAYER COOLING**
D Atienza, M Sabry, A Sridhar, Y Temiz, Y Leblebici and J R Thome, EPF Lausanne, CH
T Brunschwiler and B Michel, IBM, CH

1515 **A CIRCUIT TECHNOLOGY PLATFORM FOR MEDICAL DATA ACQUISITION AND COMMUNICATION**
Q Huang and T Burger, ETH Zurich, CH
C Enz, CSEM, CH
C Dehollain, EPF Lausanne, CH

1530 **BREAK/IP5**

11.8 HOT TOPIC – Stochastic Circuit Reliability Analysis in Nanometer CMOS

Room – Exhibition Theatre **1400-1530**

Organiser/Moderator:
G Gielen, KU Leuven, BE

Process variability causes statistical spread on the performance of ICs, eventually limiting circuit yield. In addition, aging effects in nanometer CMOS technologies cause a shift in transistor parameters over time, possibly causing circuit malfunction within the lifetime of the circuit. Some of these wear-out phenomena are stochastic in nature, introducing asymmetry in circuits. To guarantee a reliable product over the entire lifetime, fast and efficient design tools can help a designer to estimate the impact of various reliability threats on his/her circuit, at design time. The stochastic nature of the phenomena requires techniques well beyond current commercial tools. This hot topic session addresses both accurate stochastic transistor compact models that include reliability effects, as well as efficient stochastic CAD solutions to evaluate the reliability of an IC at circuit level and at system level. In addition, alternative novel system approaches are presented that exploit the stochasticity.

1400 **ANALOG CIRCUIT RELIABILITY IN SUB 32 NANOMETER CMOS: ANALYSIS AND MITIGATION**
E Maricau, G Gielen and P De Wit, KU Leuven, BE

1430 **STATISTICAL ASPECTS OF NBTI/PBTI AND IMPACT ON SRAM YIELD**
A Asenov, A Brown and B Cheng, Glasgow U, UK

1445 **PROCESS VARIABILITY ANALYSIS: FROM PROCESS TO SYSTEM**
E Remond and E Nercessian, STMicroelectronics FR

1500 **SYSTEM-ASSISTED MIXED-SIGNAL DESIGN**
N Shanbhag and A Singer,
U of Illinois, Urbana-Champaign, US

1530 **BREAK/IP5**

IP5 Interactive Presentations

Room - Salle de Reception **1530-1600**

Each Interactive Presentation will run in a 30 minute presentation slot and will additionally be supported by a poster which will be on display throughout the afternoon. Additionally, each IP will be briefly introduced in a one-minute presentation in the relevant regular session.

IP5-1 **PRIORITY DIVISION: A HIGH-SPEED SHARED-MEMORY BUS ARBITRATION WITH BOUNDED LATENCY**
H Shah and A Raabe, ForTISS GmbH, DE
A Knoll, TU Munich, DE

IP5-2 **SYSTEM-LEVEL MODELING OF A MIXED-SIGNAL SYSTEM ON CHIP FOR WIRELESS SENSOR NETWORKS**
G S Beserra, J E Guimaraes De Medeiros, A M Sampaio, J Camargo Da Costa, U De Brasilia, BR

IP5-3 **A UML 2-BASED HW/SW CO-DESIGN FRAMEWORK FOR BODY SENSOR NETWORK APPLICATIONS**
Z Sun and W-F Wong, National U of Singapore, SG
C T Yeh, Shih Chien U, PRC

IP5-4 **AREA-EFFICIENT MULTI-LEVEL SINGLE-TRACK PIPELINE TEMPLATE**
P Golani and P A Beerel, U of Southern California, US

IP5-5 **SLACK-AWARE SCHEDULING ON COARSE GRAINED RECONFIGURABLE ARRAYS**
G Ansaloni and L Pozzi, Lugano U, CH
K Tanimura and N Dutt, UC Irvine, US

IP5-6 **TIMING VARIATION-AWARE CUSTOM INSTRUCTION EXTENSION TECHNIQUE**
M Kamal and A Afzali-Kusha, Tehran U, IR
M Pedram, U of Southern California, US

IP5-7 **PSEUDO CIRCUIT MODEL FOR REPRESENTING UNCERTAINTY IN WAVEFORMS**
A Nigam, M Berkelaar, Q Tang, A Zjajo and N Van Der Meijs, TU Delft, NL

IP5-8 **A GLOBAL POSTSYNTHESIS OPTIMISATION METHOD FOR COMBINATIONAL CIRCUITS**
Z Vasicek and L Sekanina, TU Brno, CZ

IP5-9 **AN ALGORITHM TO IMPROVE ACCURACY OF CRITICALITY IN STATISTICAL STATIC TIMING ANALYSIS**
S Tsukiyama, Chuo U, JP
M Fukui, Ritsumeikan U, JP

IP5-10 **AN APPROACH FOR DYNAMIC SELECTION OF SYNTHESIS TRANSFORMATIONS BASED ON MARKOV DECISION PROCESSES**
T Welp, UC Berkeley, US
A Kuehlmann, Cadence Research Labs, US

IP5-11 **MODELLING CIRCUIT PERFORMANCE VARIATIONS DUE TO STATISTICAL VARIABILITY: MONTE CARLO STATIC TIMING ANALYSIS**
M Merrett, Y Wang and M Zwolinski, Southampton U, UK
P Asenov, D Reid, S Roy, C Millar and A Asenov, Glasgow U, UK
S Furber and Z Liu, Manchester U, UK

12.1 INTELLIGENT ENERGY MANAGEMENT PANEL SESSION – The Role of the EDA Community in the Future of World Energy Supply and Conservation?

Room – Oisans **1600-1730**

Organiser/Moderator:
P K Wright, UC Berkeley, US
P Mitcheson, Imperial College, UK

Panellists:
L Bomhold, Synopsys, US
T Green, Imperial College, UK
A Ephrimides, Maryland U, US
C Blumstein, California Institute for Energy and Environment, US
S Henry, RTE, FR

Until recently the electrical power industry has relied solely on traditional technologies - copper and iron as cables, transformers and machines as the mainstream solution for the generation, transmission and distribution of power. Whilst use of these materials and technologies is here to stay, improvements in power semiconductor technology mean that the industry is moving into a position where more and faster control of power systems can be achieved. This high level control requires a sensing and communication infrastructure to be put in place across the network. At the same time, the use of electricity in the home, through the potential of real time consumer pricing requires new technologies.

This panel session aims to pull together heavy current electrical power engineers and light current electronic engineers to form a discussion and debate about the future role of EDA in applications which are being brought about by changes in the functioning of the power industry. Power engineers from both industry and academia will stimulate the discussion with requirements both from a system perspective and consumer perspective. The representatives from the EDA side will respond with what contributions they believe EDA can make, what already exists or is a simple development problem and what research issues remain in achieving these goals. In summary, this panel aims to provide motivation for the EDA industry to work on useful technology that can be applied to heavy power systems with a view to improving global energy efficiency.

1730 **CLOSE**

12.2 Design and Run-Time Support for Dynamic Reconfigurability

Room – Meije **1600-1730**

Moderators:
P Lysaght, Xilinx, US
F Ferrandi, Politecnico di Milano, IT

This session presents techniques for optimising FPGA configuration times, compiler enhancements for improved acceleration performance of critical code kernels and a run-time management system for heterogeneous systems consisting of fine and coarse-grained architectures.

1600 **FAST STARTUP FOR SPARTAN-6 FPGAS USING DYNAMIC PARTIAL RECONFIGURATION**
J Meyer, M Huebner, L Braun, O Sander and J Becker, Karlsruhe Institute of Technology (KIT), DE
J Noguera and R Stewart, Xilinx, US
R M Gil, UAH, ES

1630 **LOOP DISTRIBUTION FOR K-LOOPS ON RECONFIGURABLE ARCHITECTURES**
O S Dragomir and K Bertels, TU Delft, NL

1700 **MRTS: RUN-TIME SYSTEM FOR RECONFIGURABLE PROCESSORS WITH MULTI-GRAINED INSTRUCTION-SET EXTENSIONS**
W Ahmed, M Shafique, L Bauer and J Henkel, Karlsruhe Institute of Technology (KIT), DE

1730 **CLOSE**

12.3 Reliability and Error Tolerance in Logic Synthesis

Room – Belle-Etoile **1600-1730**

Moderators:
S Nowick, Columbia U, US
A Yakovlev, Newcastle U, UK

This session features papers which show how to improve reliability of logic, use error tolerance to optimise a circuit, and how to prevent NBTI aging from making your logic fail timing.

1600 **RELIABILITY-DRIVEN DON'T CARE ASSIGNMENT FOR LOGIC SYNTHESIS**
A Zukoski, M Choudhury and K Mohanram, Rice U, US

1630 **A NEW CIRCUIT SIMPLIFICATION METHOD FOR ERROR TOLERANT APPLICATIONS**
D Shin and S K Gupta, U of Southern California, US

1700 **AGING-AWARE TIMING ANALYSIS AND OPTIMISATION CONSIDERING PATH SENSITISATION**
K-C Wu and D Marculescu, Carnegie Mellon U, US

1730 **CLOSE**

12.4 Multilevel Simulation and Validation

Room – Stendhal **1600-1730**

Moderators:
A Acquaviva, Politecnico di Torino, IT
E Aboulhamid, Montreal U, CA

This session deals with validation and simulation techniques at different levels of abstraction. The first two papers address the problem of simulation of high level models. The following two papers focus on generating high quality validation suites. The last work presents a STA tool that efficiently determines the critical path list to speed-up delay computation.

1600 **EFFICIENT PARAMETER VARIATION SAMPLING FOR ARCHITECTURE SIMULATIONS**
F Lu, R Joseph, G Trajcevski, S Liu, Northwestern U, US

1630 **TEMPORAL PARALLEL SIMULATION: A FAST GATE-LEVEL HDL SIMULATION USING HIGHER LEVEL MODELS**
D Kim and M Ciesielski, U of Massachusetts Amherst, US
K Shim and S Yang, Pusan National U, KR

1645 **A UNIFIED METHODOLOGY FOR PRE-SILICON VERIFICATION AND POST-SILICON VALIDATION**
A Adir, A Ziv, S Landa, G Shurek, S Copty and A Nahir, IBM, IL

1700 **EFFICIENT VALIDATION INPUT GENERATION IN RTL BY HYBRIDISED SOURCE CODE ANALYSIS**
L Liu and S Vasudevan,
U of Illinois at Urbana-Champaign, US

1715 **AN EFFICIENT AND SCALABLE STA TOOL WITH DIRECT PATH ESTIMATION AND EXHAUSTIVE SENSITISATION VECTOR EXPLORATION FOR OPTIMAL DELAY COMPUTATION**
S Barcelo, X Gili, S Bota and J Segura,
Balearic Islands U (UIB), ES

1730 **CLOSE**

12.5 Error Correction and Resilience

Room – Chartreuse **1600-1730**

Moderators:
J Abella, Barcelona Supercomputing Center, ES
D Gizopoulos, Piraeus U, GR

Innovative approaches to analyse and implement error correction and resilience in memory and logic design are proposed.

1600 **A CONFIDENCE-DRIVEN MODEL FOR ERROR-RESILIENT COMPUTING**
C-H Chen, Y Kim, Z Zhang, D Blaauw and D Sylvester,
U of Michigan, Ann Arbor , US
H Naeimi and S Sandhu, Intel, US

1630 **ELIMINATING SPEED PENALTY IN ECC PROTECTED MEMORIES**
M Nicolaidis, T Bonnoit and N-E Zergainoh,
TIMA Laboratory, FR

1700 **ERROR CORRECTING CODE ANALYSIS FOR MEMORY HIGH RELIABILITY AND PERFORMANCE**
D Rossi, N Timoncini and C Metra, DEIS - Bologna U, IT
M Spica, Cypress Semiconductor, US

1715 **ERROR PREDICTION BASED ON CONCURRENT SELF-TEST AND REDUCED SLACK TIME**
V Gherman, J Massas, S Evain, S Chevobbe and Y Bonhomme, CEA LIST, FR

1730 **CLOSE**

12.6 Security Modules from Layout to Network-on-Chip

Room – Bayard **1600-1730**

Moderators:
L Fesquet, TIMA Laboratory, FR
V Fischer, St. Etienne U, FR

Physically uncloneable functions, Trojan and error detection cipher processors, are particularly important to ensure security into systems. All these mechanisms, inserted at design time, have to be robust and efficient against a large panel of side-channel and fault attacks. This session will give an overview of these techniques, starting from the layout to the network-on-chip level.

1600 **PHYSICALLY UNCLONABLE FUNCTIONS FOR EMBEDDED SECURITY USING LITHOGRAPHIC VARIATION**
A Sreedhar and S Kundu,
U of Massachusetts at Amherst, US

1630 **RON: AN ON-CHIP RING OSCILLATOR NETWORK FOR HARDWARE TROJAN DETECTION**
X Zhang and M Tehranipoor, Connecticut U, US

1700 **ARITHMETIC LOGIC UNITS WITH HIGH ERROR DETECTION RATES TO COUNTERACT FAULT ATTACKS**
M Medwed, TU Graz, AT
S Mangard, Infineon Technologies, DE

1715 **DATA-ORIENTED PERFORMANCE ANALYSIS OF SHA-3 CANDIDATES ON FPGA ACCELERATED COMPUTERS**
Z Chen, X Guo, A Sinha and P Schaumont,
Virginia Tech, US

1730 **CLOSE**

12.7 HOT TOPIC – Sustainability through Massively Integrated Computing: Are We Ready to Break the Energy Efficiency Wall for Single-Chip Platforms?

Room – Les Bans 1600-1730

Organiser:
R Marculescu, Carnegie Mellon U, US

Moderator:
N Nicolici, McMaster U, CA

In this hot topic session we intend to elaborate on new, far-reaching, design methodologies and run-time optimisation techniques that can help breaking the energy efficiency wall in massively integrated single-chip computing platforms. Specifically, there are three nature-inspired approaches we want to discuss: *Small-world networks, game-theoretic and consensus optimisation,* and *multiscale and multifractal network behaviour.* We hope that our talks will stir an engaging discussion among the participants on a few major challenges and appropriate design solutions that will enable multicore-based single chip systems to be energy efficient and sustainable when solving various real life problems.

1600 **SUSTAINABILITY THROUGH SMALL WORLD NETWORKS: REVISING THE MULTI-CORE CHIP DESIGN**
P Pande, Washington State U, US

1630 **RUNTIME AND DISTRIBUTED OPTIMISATION IN MASSIVE MULTI-CORE: GAME THEORETIC AND CONSENSUS APPROACHES FOR ENERGY EFFICIENCY**
F Clermidy, CEA-LETI, FR

1700 **UNDERSTANDING THE MULTISCALE BEHAVIOR OF NETWORKED SYSTEMS: FROM APPLICATION SOFTWARE TO MULTICORE PLATFORMS**
R Marculescu, Carnegie Mellon U, US

1730 **CLOSE**

12.8 HOT TOPIC – Synthesis Supported Increase of Efficiency in Analogue Design

Room – Exhibition Theatre 1600-1730

Organiser:
J Nowak, IMMS GmbH, DE

Moderator:
R Sommer, TU Ilmenau, DE

Analogue design still is the bottleneck in the development of mixed-signal ICs.

This is due to the fact that the three steps in analogue circuit design – topology generation or modification, sizing and layout generation – are mainly carried out by hand. In this special session four methods will be presented which allow a semi-automated design process. These approaches include a fully automated hierarchical topology generation for analogue circuits, a generation of a compensation network by automated topology modification, a methodology for sizing based on a combination of analytic and numerical techniques and a method for modular layout generation. The methods and the resulting tools relieve the designer from routine tasks, allow more space for creativity and enable re-use.

1600 **AUTOMATED EXPLORATIVE TOPOLOGY SYNTHESIS FOR ANALOG CIRCUITS**
O Mitea, M Meissner and L Hedrich, Frankfurt U, DE
P Jores, Robert Bosch GmbH, DE

1630 **A NEW METHOD FOR AUTOMATED GENERATION OF COMPENSATION NETWORKS – THE 'EDA DESIGNER FINGER'**
E Hennig, IMMS GmbH, DE
D Krausse and R Sommer, TU Ilmenau, DE
C Sporrer, Infineon Technologies AG, DE

1645 **STRATEGIES FOR INITIAL SIZING AND OPERATING POINT ANALYSIS OF ANALOG CIRCUITS**
V Boos and J Nowak, IMMS GmbH, DE
S Henker and S Hoeppner TU Dresden, DE
M Sylvester, MunEDA, DE
H Grimm, Melexis GmbH, DE

1715 **GENERATOR BASED APPROACH FOR ANALOG CIRCUIT AND LAYOUT DESIGN AND OPTIMISATION**
A Graupner, ZMDI, DE
R Jancke, Fraunhofer IIS/EAS, DE
R Wittmann, IP-GEN, DE

1730 **CLOSE**

friday workshops

Chair:
Nicola Nicolici, McMaster U, Hamilton, CA

The DATE Friday Workshops initiative was first introduced in 2003 and, since then, the workshops topics and participation have increased to some 230 researchers and designers attending six workshops at DATE 10. This initiative has now become an integral part of the conference, offering workshops on current and emerging important issues in design, test, EDA and software to complement the regular conference programme running throughout the week. They provide an unique opportunity for the various research and design communities to spend a day discussing the latest and the best, sharing their experiences and visions.

This year's programme includes eight workshop themes ranging from embedded systems and SOC design to 3D integration, FPGA-based acceleration and processor emulation. The embedded systems field, of growing interest to the DATE community, is covered by three workshops focused on embedded parallel computing platforms, predictability and performance in embedded systems, and model based engineering methods. The SOC workshops explore hardware dependent software solutions and micro power management for macro SOCs. Building on the success from the previous two years, the 3D integration workshop covers a broad spectrum of topics from technology to commercialisation. Two new DATE workshops on FPGA-based acceleration and processor emulation respectively wrap up the large variety of themes from the Friday's programme.

Friday Workshop attendees should choose in advance one of W1, W2, W3, W4, W5, W6, W7 or W8. The Friday Workshops run from 0830 in the morning until 1700 in the afternoon. The individual timetables for each Friday Workshop vary and are as listed below. For the detailed version of the programme, visit - www.date-conference.com

W1 Workshop on Micro Power Management for Macro Systems on Chip (uPM²SoC)

Room – Les Bans **0845 - 1630**

Organisers:
Diana Marculescu, Carnegie Mellon U, US
Suzanne Lesecq, CEA-LETI Minatec, FR
Diego Puschini, CEA-LETI Minatec, FR
Radu Marculescu, Carnegie Mellon U, US

Description: Increased integration of hundreds of processing cores on the same silicon substrate has allowed the concurrent execution of multiple applications on a chip, but at the cost of significant increase in on-chip power consumption. On-chip power management has therefore become a critical component of every step in the many-core design flow, from physical design all the way up to micro-architecture and system-level design.

While dynamic power management has been extensively studied for the case of single-core systems, many-core systems present additional challenges that require maintaining appropriate performance levels for applications running on the system both in the context of turning on/off cores and using selectively power states, or in the context of using Dynamic Voltage Frequency Scaling (DVFS) for enabling a certain performance level at a minimum power. Furthermore, enabling power management at macroscale – for hundreds or thousands of on-chip resources – while relying on capabilities developed at microscale – specifically, technology and device-level knobs – becomes an essential for effective power control.

This workshop addresses this need by targeting emerging topics in power management and control of large scale many-core systems, such as scalability, distributed vs. centralised vs. hybrid approaches, as well as technology-driven challenges that need to be considered for providing a truly power-aware solution, such as static and dynamic variations and reliability, as well as limits for control strategies for technologies 22nm and beyond. Further details can be found at http://www.ece.cmu.edu/~dianam/uPM2SoC10/.

0845 **Introduction to the Workshop**
Diana Marculescu, Suzanne Lesecq

0900 **Keynote 1: Technology at the design and system levels for making fine-grain dynamic power management a reality**
Fabien Clermidy, CEA-LETI, FR

0945 **Keynote 2: Fine-grained Power management for heterogeneous many-core architectures in 32nm and beyond**
Luca Benini, Bologna U and STMicroelectronics, IT

1030 **BREAK**

1100 **Power Modelling and Optimisation**

Regular papers:

An Energy Scalability Model for Efficient Resource Allocation on Manycore Architectures
Joosung Kim, Hakbong Kim, Hyunhee Kim and Jihong Kim, School of Computer Science and Engineering, Seoul National U, KR

Task scheduling based on energy token model
Danil Sokolov and Alex Yakovlev, Newcastle U, UK

Exploiting the Correlation Between Leakage and Frequency for Speed-binning
Siddharth Garg, Waterloo U, CA

Poster highlights:

Improving Automated Stress Pattern Generation For Increasing SoC Dynamic Power Consumption
Mauricio De Carvalho, Paolo Bernardi, Ernesto Sanchez and Giovanni Squillero, Politecnico di Torino, IT

Enabling Timing and Power Aware Virtual Prototyping of HW/SW Systems
Kim Gruettner, Kai Hylla, Sven Rosinger, OFFIS, DE
Philipp A Hartmann and Wolfgang Nebel,
Carl von Ossietzky U Oldenburg, DE

GPGPU-Accelerated Instruction Accurate and Fast Simulation of Thousand-core Platforms
Shivani Raghav, Martino Ruggiero and
David Atienza, EPF Lausanne, CH
Christian Pinto, Andrea Marongiu and Luca Benini,
Bologna U - DEIS, IT

1205 **LUNCH BREAK**

1325 **Thermal and Power Management**

Regular papers:

Fault Tolerant Thermal Management for High-Performance Multicores
Andrea Bartolini, Matteo Cacciari, Alessio Cellai,
Manuel Morelli, Andrea Tilli and Luca Benini,
Bologna U – DEIS, IT

System Level Power Management for Many-Core Systems
Simon Holmbacka, Jens Smeds, Sébastien Lafond
and Johan Lilius, Åbo Akademi U,
Department of Information Technologies, FI

Game Theoretic Power Management Techniques for Real-Time Scheduling
James Docherty and Alex Yakovlev, Newcastle U, UK

Poster Highlights:

DVFS applied to a Homogeneous MPSoC for Power-Efficient Algorithms Implementations
Roberto Airoldi, Fabio Garzia and Jari Nurmi,
Tampere U of Technology , FI

Energy-Aware Simultaneous Architecture Exploration and Task Scheduling for MPSoCs under Process Variation
Mahboobeh Ghorbani, Mahmoud Momtazpour and
Maziar Goudarzi, Sharif U of Technology, IR

1430 **BREAK AND POSTER SESSION**
(includes all regular papers and posters above)

1500 **POSTER SESSION**
(cont'd – includes all regular papers and posters above)

1530 **Panel Session (Organiser: Radu Marculescu) – Cutting the Gordian Knot: Power management for extreme scale computing under extreme scale constraints**

Panellists:
Kees Goosens, TU Eindhoven, NL
Robert Dick, U of Michigan, Ann Arbor, US
Norbert Wehn, Kaiserslautern U, DE
Peter Feldmann, IBM TJ Watson, US

W2 Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing

Room – Meije 0800 -1645

Organisers:
George A Constantinides, Imperial College, UK
Brent Nelson, Brigham Young U, US
Satnam Singh, Microsoft Research, UK

Description: Field-Programmable Gate Arrays (FPGAs) have been considered as possible implementation platforms for computation since the early 1990s. Over the technology generations, the regularity of FPGA designs has allowed them to stay at the leading edge of each new technology node, with architectural innovations enabling their widespread adoption for embedded applications. The potential of FPGAs for scientific computation is well understood today; nonetheless, long implementation cycles have hindered their faster adoption for numerically intensive scientific applications. We currently stand on a threshold, where various key research contributions and initiatives have the potential to propel FPGA-based computation from the embedded space into scientific computing. At the same time, other "accelerator technologies" such as GPGPU are beginning to make deep inroads into traditional HPC, with the potential for common design capture languages such as OpenCL.

This workshop will critically examine the state of the art in this community, and will include a panel discussion of whether FPGAs will ever make a significant breakthrough into scientific computation, and the challenges – technological and otherwise – that will need to be surmounted for them to do so. We aim to bring together the leading researchers in the field to help converge on a collaborative research programme enabling this vision.

The workshop programme contains the following elements.

- Six sessions with in total four regular presentations
- Two poster sessions
- A panel session

For the detailed version of the programme, please check http://www.date-conference.com/conference/date11-workshop-W2

0800 **SESSION 1: OPENING AND PAPER**
Moderator: Satnam Singh, Microsoft Research, UK

0900 **Higher Level Programming Abstractions for FPGAs using OpenCL**
Desh Singh, Altera, CA

1000 **SESSION 2: COFFEE AND POSTERS**

1045 **SESSION 3: PANEL: DISCUSSION**

"FPGA-based Scientific Computing: A Bright Future?"
Moderator: George A Constantinides, Imperial College, UK

Panellists:
Brent Nelson, Brigham Young U, US
Satnam Singh, Microsoft Research, UK
Greg Stitt, U of Florida, US
David Thomas, Imperial College, UK

1200 **LUNCH BREAK**

1300 **SESSION 4: PAPERS**
Moderator: Brent Nelson, Brigham Young U, US

1300 **Execution of a Computational Fluid Dynamics application on FLOPS-2D, a multi-FPGA platform**
Hideharu Amano, Keio U, JP

1400 **Exploiting spatial parallelism to improve both speed and accuracy in financial computing**
David Thomas, Imperial College, UK

1500 **SESSION 5: COFFEE AND POSTERS**

1545 **SESSION 6: PAPER**
Moderator: David Thomas, Imperial College, UK

1545 **Floating Point Vector Processing on an FPGA**
Miriam Leeser, Northeastern U, US

1645 **CLOSE**

W3

Third Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications

Room – Bayard 0830 -1645

Organisers:
Cristina Silvano, Politecnico di Milano, IT – General Co-Chair
Giovanni Agosta, Politecnico di Milano, IT – General Co-Chair
Maurizio Palesi, Kore U, IT – Architectures Session Chair
Chantal Ykman-Couvreur, IMEC, BE – Design Tools Session Chair
Diana Goehringer, Fraunhofer IOSB, DE – Applications Session Chair
Michael Huebner,
Karlsruhe Institute of Technology, DE – Poster Session Chair
Juergen Becker,
Karlsruhe Inst. of Technology, DE – Panel Session Co-Chair
Michael Huebner,
Karlsruhe Inst. of Technology, DE – Panel Session Co-Chair
Fabrizio Castro,
Politecnico di Milano, IT – Web and Posters Submission Chair

Description: The future of embedded computing is shifting to multi/many-core designs to boost performance due to the unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence embedded system designers are increasingly faced with the following new big challenges: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant issues:

- How can we write applications that exploit the underlying (parallel) architecture, without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the process should be automated?
- How should we design the underlying architectures?

This workshop brings together researchers actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

The workshop will have three main sessions:

- Architectures: on the most relevant problems arising during the design exploration and optimisation of many/multi core architectures.
- Design tools: on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- Applications: on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

FRIDAY

For the detailed version of the program, please check the Workshop web site:

http://conferenze.dei.polimi.it/depcp/

The Call for Posters is already available at the Workshop web site.

- Posters submission deadline: January 15, 2011
- Notification of acceptance: February 5, 2011
- Posters programme will be posted online by February 10, 2011

PRELIMINARY PROGRAMME

0830	**Opening Session:** Cristina Silvano and Giovanni Agosta, Politecnico di Milano, IT
0845	**Introduction to Poster Sessions:** Michael Huebner, Karlsruhe Institute of Technology, DE
0900	**Architectures Session -** Organiser: Maurizio Palesi, Kore University, IT
	Invited Speaker: Diego Melpignano, STMicroelectronics, Grenoble, FR
0945	**Invited Speaker:** Radu Marculescu, Carnegie Mellon University, US
1030	**BREAK & POSTER SESSION** (Posters programme will be posted online)
1100	**Panel on: "Embedded Multi-core Computing: Challenges and Trends"** Panel Organisers and Moderators: Juergen Becker and Michael Huebner, Karlsruhe Institute of Technology, DE
1200	**LUNCH BREAK**
1300	**Design Tools Session -** Organiser: Chantal Ykman-Couvreur, IMEC, BE
	Invited Speaker: Gert Goossens, Target Compiler Technologies, BE
1345	**Invited Speaker:** Iole Moccagatta, NVIDIA, US
1430	**BREAK & POSTER SESSION** (Posters programme will be posted online)
1500	**Applications Session -** Organiser: Diana Goehringer, Fraunhofer IOSB, DE
	Invited Speaker: Benno Stabernack, Fraunhofer HHI, Berlin, DE
1545	**Invited Speaker:** Michael Riepen, Intel Labs Braunschweig, DE
1630	**Final Wrap-up**
1645	**CLOSE**

W4 Bringing Theory to Practice: Predictability and Performance in Embedded Systems

Room – Berlioz **0830 - 1600**

Organisers:
Philipp Lucas, Saarland U, DE
Lothar Thiele, ETH Zurich, CH
Benoit Triquet, Airbus, FR
Theo Ungerer, Augsburg U, DE
(Chair) **Reinhard Wilhelm,** Saarland U, DE

Description: The PPES workshop is concerned with critical hard real-time systems that have to satisfy both efficiency and predictability requirements. For example, an electronic controller for a safety-critical system in an automobile needs to react not only correctly to external inputs such as rapid deceleration or loss of grip, but also provably within a given time-span. Although there exist techniques to accurately predict the worst-case execution time of critical embedded systems for complex microprocessors, the current approaches will not scale to future systems. The trend of integrating multiple functions on a single control unit or to use multi-core systems with shared resources saves costs, but introduces lots of interferences between tasks and components.

A unified approach which focuses on performance and predictability of Embedded Systems is needed to permit analysability of future systems. The workshop will discuss approaches to achieve improvements of worst-case predictability and of average-case performance on all system layers, including hardware architecture, operating systems, code generation, software architecture and program analysis. It will also discuss the problems arising in industrial practice in trying to achieve one or both of these goals and address proposed tools or standardisation efforts.

For more information about the workshop, see:
http://ppes2011.cs.uni-saarland.de

PROGRAMME

0830

Invited Talk:
Predictability and Performance Requirements in Avionics Systems
Ottmar Bender, Cassidian Electronics, DE

0930

Papers:
Software Structure and WCET Predictability
Gernot Gebhard, Christoph Cullmann and Reinhold Heckmann, AbsInt, DE

Towards a Time-predictable Dual-Issue Microprocessor: The Patmos Approach
Martin Schoeberl and Pascal Schleuniger, DTU, DK
Wolfgang Puffitsch, TU Vienna, AT
Florian Brandner, ENS Lyon, FR
Christian W Probst and Sven Karlsson, DTU, DK
Tommy Thorn, Unaffiliated, US

1030 **BREAK**

1100

Papers:
A Template for Predictability Definitions with Supporting Evidence
Daniel Grund, Saarland U, DE
Jan Reineke, UC Berkeley, US
Reinhard Wilhelm, Saarland U, DE

An Overview of Approaches Towards the Timing Analysability of Parallel Architectures
Christine Rochange, Toulouse U, FR

1200 **LUNCH BREAK**

1300

Papers:
Implementation and Empirical Evaluation of Partioning-Based Multi-Core Scheduling
Yi Zhang, Northeastern U, CN
Nan Guan and Wang Yi, Uppsala U, SE

An Automated Flow to Map Throughput Constrained Applications to a MPSoC
Roel Jordans, Firew Siyoum and Sander Stuijk, TU Eindhoven, NL
Akash Kumar, TU Eindhoven, NL / National U, SG
Henk Corporaal, TU Eindhoven, NL

Towards Formally Verified Optimising Compilation in Flight Control Software
Ricardo Bedin-Franca, Airbus / ENSEEIHT, FR
Denis Favre-Felix, Airbus, FR
Xavier Leroy, INRIA Rocquencourt, FR
Marc Pantel, ENSEEIHT, FR
Jean Souyris, Airbus, FR

1430 **BREAK**

1500

Panel Discussion:
Predictability and Industrial Reality
Moderator:
Lothar Thiele, ETH Zurich, CH
Participants:
Ottmar Bender, Cassidian Electronics, DE
Benoit Triquet, Airbus, FR
Theo Ungerer, Augsburg U, DE
Reinhard Wilhelm, Saarland U, DE
Rafael Zalman, Infineon, DE

1600 **CLOSE**

W5 3D Integration – Applications, Technology, Architecture, Design, Automation, and Test

Room – Stendhal **0830 - 1600**

Organisers:
Yuan Xie, Pennsylvania State U, US
Damien Riquet , STMicroelectronics SA, FR
Nikolaos Minas, IMEC, BE

Description: 3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. But in order to produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the art, exchange ideas, and discuss future challenges. The first and second edition of this workshop took place in conjunction with DATE 2009 and DATE 2010 (see http://www.date-conference.com/date09/conference/date09-workshop-W5 and http://www.date-conference.com/date10/conference/date10-workshop-W5)

The workshop program contains the following elements.

- Two invited keynote addresses
- Two sessions with in total six regular presentations
- Two poster sessions
- A panel session

For the detailed version of the program, please check http://www.dateconference.com/conference/date11-workshop-W5

0830 **SESSION 1: OPENING**

Welcome Address and Introduction to the Workshop
Yuan Xie and Damien Riquet

0850 **Keynote Address**

Architecture and Design of 3DICs
Dr. Tanay Karnik, Intel, USA

0925 **Keynote Address**

Lower Cost Alternative to TSV Using ThruChip Interface (TCI)
Prof. Tadahiro Kuroda, Keio University, Japan

1000 **SESSION 2: BREAK & POSTER SESSION (see list on web)**

1030 **SESSION 3: PAPERS**

Electrical Performances of 3D TSV Channel and 3D Stacked PDN based on Hierarchical Models
Jun So Pak, Joohee Kim, Jonghyun Cho, Heegon Kim, Kiyeong Kim and Joungho Kim, KAIST, KR

Thermal Gradient Effects on Inductively Coupled 3-D ICs,
Somayyeh Rahimian Omam, Vasilis F. Pavlidis and Giovanni De Micheli, EPF Lausanne, CH

Thermal-aware Bus Architecture Flow for Three-Dimensional Microprocessors
Eren Kursun, IBM, US

1200 **LUNCH BREAK**

1300 **SESSION 4: PAPERS**

Variation-Aware Die-to-Die Bonding in Circuit-Partitioned 3D Integrated Circuits
Lei Zhang, Jie Wang and Yinhe Han, Chinese Academy of Sciences, CN
Qiang Xu, The Chinese University of Hong Kong, HK

Early Chip Planning Cockpit
Jeonghee Shin, IBM, US

3D integration with TSV interconnects: Technology Trends & Market Analysis
Jerome Baron, Yole Developpement, FR

1430 **SESSION 5: BREAK & POSTER SESSION (see list on web)**

1500 **SESSION 6: PANEL DISCUSSION**

"Commercialisation of 3D Technology: How far are we?"

1600 **CLOSE**

W6

M-BED'2011, the 2nd Workshop on Model Based Engineering for Embedded Systems Design

Room – 7 Laux 4 0830 - 1630

Organisers:
Pierre Boulet, Lille 1 U, LIFL, FR
Daniela Cancila, Atego, FR
Sebastien Gerard, CEA-LIST, FR
Adam Morawiec, ECSI, FR
Chokri Mraihda, CEA-LIST, FR
Laurent Rioux, Thales RT, FR
Bran Selic, Malina Software Corp, CA

Description: The application of model-based engineering (MBE) methods for software and systems development in industry is increasing. Moreover, the integration of component-based approaches with MBE has further accelerated its adoption along is also providing a basis for a sounder theoretical underpinning.

The focus of this workshop is on the use of MBE for embedded systems development (e.g. in the industrial transport sector for applications such as railway systems, automotive, aerospace, and related domains). In this context, special focus is given to MARTE, the UML profile for Modeling and Analysis of Real-Time and Embedded systems, which has proven successful in a number of projects. In particular, the program concentrates on the following topics:

• The infrastructure that supports MBE, that is, the requisite languages, tools, and standards, as well as the combination of design and V&V activities, and the diverse engineering disciplines involved in embedded system design.

• Process and methodology related issues, such as guidelines for deciding when and how to use domain-specific languages, appropriate integration of tools, and advanced methods to assist on architecture exploration subjected to multiple non functional constraints. Experience with applying MARTE and suggestions of improvements to this standard.

The aim of the workshop is to bring together researchers as well as system designers and tool developers from both industry and academia to discuss applications of model-based engineering in general and MARTE usage in particular. A significant portion of time will be reserved for discussion. Complementing the accepted paper presentations will be several invited presentations by members of the MARTE standardisation task force, specialists participating in relevant European projects, and representatives of MBE tool vendors. The one-day workshop is organised in multiple sessions, each focusing on a particular topic. Rather than have questions at the end of each presentation, all discussion will be conducted at the end of the session, with all presenters in the session responding as a group to questions of the session moderator as well as other attendees.

0830 **OPENING SESSION**

Welcome Address

0845 **Keynote Address: Using Metaheuristic Search for the Analysis and Verification UML Models**
Lionel Briand, Oslo U, NO

0945 **SESSION 1: Model Driven Methodologies**

Model-based development of embedded systems - the MADES approach
Neil Audsley, Ian Gray, Leandro Indrusiak, Dimitrios Kolovos, Nicholas Drivalos and Richard Paige, York U, UK

1000 **Methodological Guidelines on the Usage of MARTE VSL for Specification of Time Constraints**
Arnaud Cuccuru, Chokri Mraidha, Ansgar Radermacher and Sebastien Gerard, CEA LIST, FR
Laurent Rioux, Thales RT, FR
Thomas Vergnaud and Olivier Hachet, Thales Communications, FR

1015 **Verification of ArchMDE Software Architecture Using UPPAAL Based On Model Transformation: From TURTLE Profile to Blackboard Style**
Nourchene Elleuch, Adel Khalfallah and Samir Ben Ahmed, U of Sciences, Tunis, TN

1030 **Discussion**

1045 **BREAK**

1100 **SESSION 2: MARTE Use Cases**

Experiencing the UML profile for MARTE in the generation of schedulability analysis models for MAST
Julio Medina and Alvaro Garcia Cuesta, Cantabria U, ES

1115 **Safe design of dynamically reconfigurable embedded systems**
Xin An and Eric Rutten, INRIA Rhones-Alpes, FR
Abdoulaye Gamatie, CNRS, LIFL, FR

1130 **Programming Massively Parallel Architectures using MARTE: a case study**
Antonio Wendell de Oliveira Rodrigues, Frederic Guyomarch and Jean-Luc Dekeyser, Lille 1 U, LIFL, FR

1145 **Discussion**

1200 **LUNCH BREAK**

1300 **SESSION 3: Invited Talks**

Towards MARTE 1.2 and its SysML relationships
Laurent Rioux, Thales RT, FR

1330 **Presentation of the RTSimex project**
Laurent Rioux, Thales RT, FR

1400 **SESSION 4: Electronic System Level Modelling**

A Retargetable SysML-based Front-End for High-Level Synthesis
Fabian Mischkalla and Wolfgang Mueller, Paderborn U, DE

1415 **Towards SystemC Code Generation from UML/MARTE Concurrent System-Level Models**
Pablo Penil, Fernando Herrera and Eugenio Villar, Cantabria U, ES

1430 **Generation of Abstract IP/XACT Platform Descriptions from UML/MARTE for System-Level Performance Estimation**
Fernando Herrera and Eugenio Villar, Cantabria U, ES

1445 **Combining SystemC, IP-XACT and UML-MARTE in model-based SoC design**
Jean-François Le Tallec, Julien DeAntoni and Frederic Mallet, Nice Sophia-Antipolis U, FR
Robert de Simone and Benoit Ferrero, INRIA Sophia-Antipolis, FR
Laurent Maillet-Contoz, STMicroelectronics, Crolles, FR

1500 **Discussion**

1515 **BREAK**

1530 **SESSION 5: MARTE Extensions**

Modelling Networks-on-Chip at System Level with the MARTE UML profile
Majdi Elhaji, Adbelkrim Zitouni and Rached Tourki, LAB-IT06, Monastir, TN
Pierre Boulet, Samy Meftali and Jean-Luc Dekeyser, Lille 1 U, LIFL, FR

1545 **Modelling of Legacy Communication in Distributed Embedded Systems**
Saad Mubeen, Jukka Maki-Turja and Mikael Sjodin, Malardalen U, SE

1600 **Extending MARTE with Security Concepts**
Mehrdad Saadatmand, Antonio Cicchetti and Mikael Sjodin, Malardalen U, SE

1615 **Discussion**

1630 **CLOSE**

W7 Hardware Dependent Software Solutions for SoC Design

Room – Belle-Etoile **0830 - 1630**

Organisers:
Ruud Derwig, Synopsys, NL
Christian Fabre, CEA, FR
Anne-Marie Fouilliart, THALES, FR
Erwin de Kock, NXP Semiconductors, NL
Frederic Petrot, TIMA, FR
Patrick Pirat, Thomson Grass Valley, FR
Simon Thabuteau, THALES, FR
Emmanuel Vaumorin, Magillem Design Services, FR

Description: Integration of HW and SW has become the major productivity bottleneck in SoC design. In this workshop, we introduce the integration challenges and discuss innovations that tackle this bottleneck. Past two years, a number of companies and knowledge institutes have come up with innovative solutions as the result of the Catrene SoftSoC project. The integration bottleneck is remedied by systematic and highly-automated approaches to combine HW IP with their associated Hardware Dependent Software (HDS) in efficient design packages. The packages support efficient and automated integration of HW and SW IPs into SoCs.

Nowadays, all advanced electronic products are based on SoC solutions consisting of a highly integrated chip and associated software. 95% of SoCs combine fixed function HW IP and programmable computing cores. The integration of the HW IP requires complementary software for controlling the HW IP. We refer to this software as HDS. Designing, building, configuring, integrating and testing of HDS for SoCs has grown to become a huge task. SoftSoc addresses Hardware Dependant Software (HDS) solutions to be used by SoC designers to improve design process quality and productivity for ever highly integrated SoCs.

The SoftSoC solutions are based on industrial standards, e.g, IP-XACT and TLM. Extensions to those standards are proposed when needed to integrate “software IP” within the currently full-hardware design and exploration flows. Our proposed IP-XACT extensions for SW break new grounds in term of HW/SW design integration and design flow automation opportunities.

For the detailed version of the program, please check http://www.date-conference.com/date11-workshop-W7

0830	**Welcome and introduction** Anne-Marie Fouilliart, Thales, FR
0900	**Keynote: DDGEN: An Automated Device Driver Generation Tool for Embedded Systems** Sandeep Pendharkar, Vayavya Labs, IN
1000	**BREAK**

1030 **A layered approach to hardware dependent software**
Ruud Derwig, Synopsys, NL

1100 **IP-XACT-based register abstraction and software test generation**
Gino van Hauwermeiren, Erwin de Kock and Jos Verhaegh, NXP Semiconductors, NL

1130 **Automatic Generation of HdS System Models for System Simulation using IP-XACT**
Daniel Calvo, Patricia Botella, Hector Posadas, Pablo Sanchez and Eugenio Villar, Cantabria U, ES

1200 **LUNCH BREAK**

1300 **Demonstrations (in parallel)**

Hardware dependent software generation for OMAP
Simon Thabuteau, Thales, FR

H264 video encoder mapping
Patrick Pirat, Thomson Grass Valley, FR

A device driver generation workflow
Guillaume Godet-Bar, TIMA-SLS, FR

1330 **An HdS Meta-Model Case Study: Integrating Orthogonal Computation Models**
R Nane, K Bertels, TU Delft, NL
S van Haastregt, T Stefanov and B Kienhuis, Leiden U, NL

1400 **comC: a NoC Communication Compiler**
Ivan Llopard, Jerome Martin, CEA-LETI, FR
Frederic Rousseau, TIMA-SLS, FR

1430 **BREAK**

1500 **A Model Driven Engineering approach for the automatic generation of device driver code**
Guillaume Godet-Bar and Frederic Petrot, TIMA-SLS, FR

1530 **IP-XACT extensions for hardware dependent software**
Emmanuel Vaumorin, Magillem Design Services, FR

1600 **Conclusions and wrap-up**
Anne-Marie Fouilliart, Thales, FR

1630 **CLOSE**

W8 1st International QEMU Users Forum (QUF)

Room – Chartreuse 0900 - 1715

Organisers:
Wolfgang Mueller, Paderborn U, DE
Frederic Petrot, TIMA, Grenoble, FR

More Information: http://adt.cs.upb.de/quf

Meanwhile, QEMU as Open Source Software received wide acceptance by multiple research groups. The Workshop addresses all aspects QEMU for CPU and device emulation. It will provide QEMU users from industry and academia with a discussion forum to exchange ideas and to join forces.

0900 **Opening Session**

Workshop Organisers - Welcome Address

0905 **QEMU - Project Objectives and Technical Overview**
N Froyd, Code Sourcery, Granite Bay, CA, US
A Graf, SUSE, Nuernberg, DE

0945 **Invited Presentations (1)**

QEMU and SystemC
M Monton, GreenSocs, UK and CEPHIS-UAB, Barcelona, ES
M Burton, GreenSocs, UK

1015 **Combined Use of Dynamic Binary Translation and SystemC for Fast and Accurate MPSoC Simulation**
M Gligor, TIMA, Grenoble, FR

1045 **BREAK**

1100 **Invited Presentations (2)**

QEMU/SystemC Cosimulation at Different Abstractions Levels
M Becker, Paderborn U/C-LAB, DE

1130 **Timing Aspects in QEMU/ SystemC Synchronisation**
D Quaglia, F Fummi, M Macrina and S Saggin, Verona U/EDALab s.r.l., IT

1200 **LUNCH BREAK**

1315 **Software Runtime Analysis**

Program Instrumentation with QEMU
C Guillon, STMicroelectronics, Grenoble, FR

1335 **Using QEMU in Timing Estimation for Mobile Software Development**
A P Miettinen, Nokia, Helsinki, FI
V Hirvisalo and J Knuttila, Aalto U, Espoo, FI

1355 **Embedded Processing Issues**

QEMU - A Crucial Building Block in Digital Preservation Strategies
D von Suchodoletz, K Rechert and A Nana, Freiburg U, DE

1415 **Easy Embedded Development with QEMU**
T Monjalon, Open Wide, Paris, FR

1435 **BREAK & POSTER SESSION**

Advanced Usage

1515 **MARSS-x86: A QEMU-Based Micro-Architectural and Systems Simulator for x86 Multicore Processors**
A Patel, F Afram and K Ghose, State U of New York at Binghampton, US

1535 **Showing and Debugging Haiku with QEMU**
F Revol, IMAG, Grenoble, FR

1555 **Simulation Acceleration**

PQEMU: A Parallel System Emulator Based on QEMU
J-H Ding and Y-C Chung, National Tsing Hua U, Hsinchu, Taiwan, ROC
P-C Chang and W-C Hsu, National Chiao Tung U, Hsinchu, Taiwan, ROC

1615 **QEMU TCG Enhancements for Speeding-up the Emulation of SIMD instructions**
L Michel, N Fournel and F Petrot, TIMA, Grenoble, FR

1635 **Tools**

PRoot: A Step Forward for QEMU User-Mode
C Vincent and Y Janin, STMicroelectronics, Grenoble, FR

1655 **A SysML-based Framework with QEMU-SystemC Code Generation**
D He, F Mischkalla and W Mueller, Paderborn U/C-LAB Paderborn, DE

1715 **Wrap-up and Closing**

fringe technical meetings

A number of specialist interest groups will be holding their meetings at DATE. Currently, the following meetings are scheduled but a full list of fringe meetings with description of content will be found on the DATE web portal – **www.date-conference.com**

Day	Time	Meeting & Contact	Room	Type
Mon	1900-2100	**EDAA/ACM PhD Forum** Peter Marwedel <peter.marwedel@tu-dortmund.de>	Salle de Reception	Open
Tues	1830-1930	**EDAA General Assembly** Norbert Wehn <wehn@eit.uni-kl.de>	7 Laux 4	Open
Tues	1830-2030	**ETTTC Meeting** Matteo Sonza Reorda <matteo.sonzareorda@polito.it>	Bayard	Open
Tues	1830-2130	**European SystemC Users Group Meeting** Axel Braun <abraun@informatik.uni-tuebingen.de>	Meije	Open
Thu	1730-2030	**DIAMOND Tutorial: Handling the Challenges of Debug and Reliability** Maksim Jenihhin maksim@pld.ttu.ee	Les Bans	Open

PhD forum

Monday: Room – Salle de Reception – 1900-2100

Organiser:
Peter Marwedel, TU Dortmund, DE

The EDAA/ACM PhD Forum at the Design, Automation and Test in Europe (DATE) Conference is a poster session and a buffet dinner organised and hosted by ACM SIGDA and the European Design and Automation Association (EDAA). The EDAA Best Dissertation Awards will be presented during the Wednesday lunch-time keynote session.

The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work. More information is available on the web – **www.date-conference.com**

Tool Seminars

Room - Berlioz

Once again during DATE 11 there will be Tool Seminars presented by leading tool vendors. Cadence, Cadence/EUROPRACTICE and CMP are among the vendors who will be giving a seminar. These are open to all attendees and exhibition visitors. As places are limited they will be available on a first-come, first-served basis and entrance vouchers will be available from the Conference Registration Desk located adjacent to the main entrance to Alpes Congres.

Please see <www.date-conference.com> for details of the programme as it develops.

If your company is interested in booking a Tool Seminar please contact Claire Cartwright <claire.cartwright@ec.u-net.com>

This is a programme of free events open to all attendees at DATE 11 in the Exhibition Theatre

exhibition theatre

Chair:
Juergen Haase, edacentrum, DE

In addition to the conference programme during DATE 11, there will be a presentation theatre from Tuesday 15 March to Thursday 17 March 2011. Attendees will profit from having an industry forum in the midst of of Europe's leading electronic systems design event. The theatre is located in Room Lesdiguieres which is within the exhibition hall and affords easy access for conference delegates during the morning, lunchtime and afternoon exhibition breaks.

For the third time, open Special Conference Sessions from Track 8 (full details are contained in the main conference programme pages) will take place in the Exhibition Theatre. These sessions are open to conference delegates as well as to exhibition visitors and are as follows:

2.8	**Embedded Tutorial** Addressing Critical Power Management Verification Issues in Low Power Designs	**Tuesday 1130-1300**
3.8	**Panel; Session** Power Formats: Beyond UPF and CPF	**Tuesday 1430-1600**
6.8	**Panel Session** Embedded Software Debug and Test	**Wednesday 1100-1230**
7.8	**Embedded Tutorial** Predictable System Integration	**Wednesday 1430-1600**
8.8	**Embedded Tutorial** Communication Networks in Next Generation Automobiles	**Wednesday 1700-1830**
10.8	**Panel Session** State of the Art Verification Methodologies in 201	**Thursday 1100-1230**
11.8	**Hot Topic** Stochastic Circuit Reliability Analysis in Nanometer CMOS	**Thursday 1400-1530**
12.8	**Hot Topic** Synthesis Supported Increase of Efficiency in Analogue Design	**Thursday 1600-1730**

Additionally there will be many testimonials providing valuable experience on recent results of leading companies in application of advanced design methodologies and of new tools.

The Exhibition Theatre will present in detail the two European key semi-conductor sites, Grenoble and Dresden. Grenoble is the home of worldwide market leaders, more than 100 start-up companies in addition to 117 companies, 81% of which are SME's and top research institutes. In panel discussions, testimonials, embedded tutorials and special sessions on research work they will present and discuss their latest innovations and strategies. The intensive co-operation between the sites in Grenoble and Dresden, on industrial level as well as in research programmes, will also be highlighted by the Exhibition Theatre programme.

Please see the online programme and the Event Guide for full details.

university booth demonstrations

DATE 11 will feature the University Booth where system and VLSI CAD tools developed in Universities and Research Institutes are demonstrated as well as circuits in their working environment. This provides an alternative and more direct way of communicating CAD research results and displaying working silicon to the interested specialists. The University Booth will be located in the Exhibition Hall and will be furnished with popular workstations. A rotating schedule will operate throughout the three days.

Contacts: Lorena Anghel <lorena.anghel@imag.fr>
Volker Schoeber <schoeber@edacentrum.de>

vendor exhibition

DATE 11 Exhibitors and Sponsors include:

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Embedded Software Architectures and Principles; Software for MPSoC, Multi/Many-Core and GPU-Based Systems

Oliver Bringmann
FZI, DE
Gabriela Nicolescu
Polytechnique Montreal, CA

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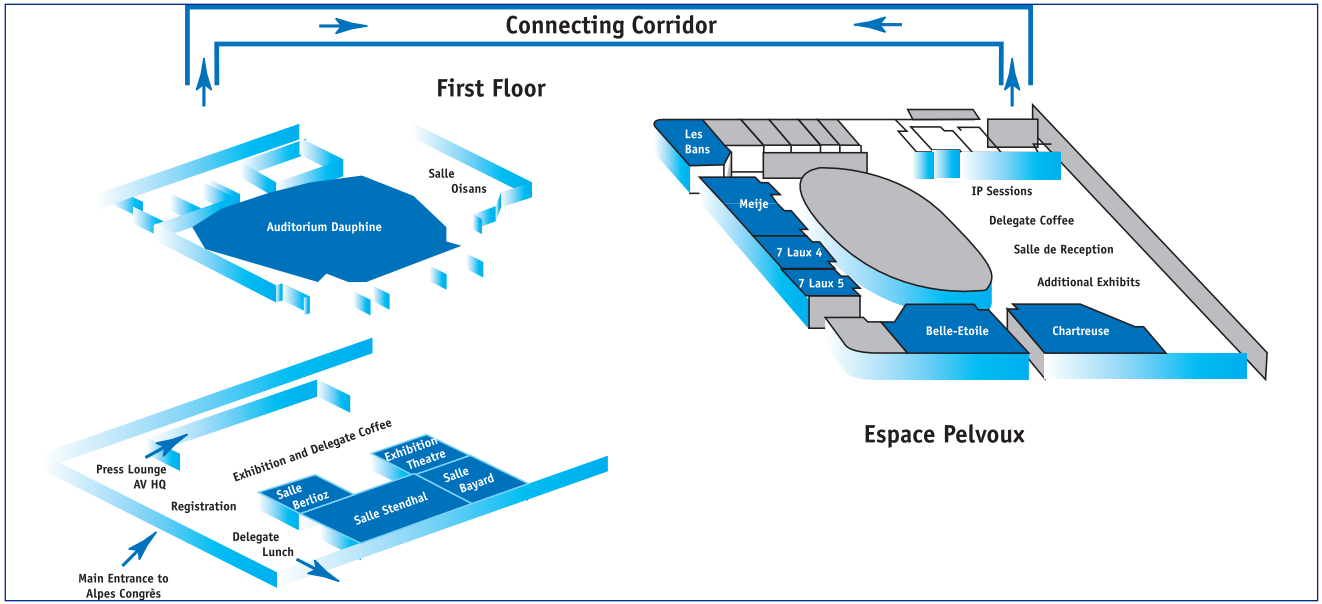
IET
SAME


Connecting Corridor
First Floor
Auditorium Dauphine
Salle Oisans
Les Bans
Meije
7 Laux 4
7 Laux 5
IP Sessions
Delegate Coffee
Salle de Reception
Additional Exhibits
Belle-Etoile
Chartreuse
Espace Pelvoux
Press Lounge AV HQ
Exhibition and Delegate Coffee
Exhibition Theatre
Salle Bayard
Salle Berlioz
Salle Stendhal
Registration
Delegate Lunch
Main Entrance to Alpes Congrès